Operational Amplifiers and Comparators Data Book

Volume B

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INTRODUCTION

Texas Instruments (TI) offers an extensive line of industry-standard and leadership products dedicated to operational amplifier and comparator functions. The technologies represented in this book include traditional bipolar through BIDFET, BIFET, IMPACT™, LinCMOS™, Advanced LinCMOS™, and Excalibur processes. The IMPACT, Advanced LinCMOS, and Excalibur technologies feature a step-function improvement in impedance, speed, power requirements, and threshold stability.

The Operational Amplifier/Comparator Data Books (volumes A and B) provide information on an extensive listing of TI operational amplifier and comparator products:

- Commercial, Industrial, Automotive, Military, and Extended Temperature Ranges
- Noncompensated, Single, Dual
- Internally Compensated, Single, Dual, Quad
- Precision, Copper Stabilized
- Excalibur: High Speed, Low Power, Precision, JFET Input, High Output, Low Noise

EXCALIBUR PROCESS DISCUSSION

Excalibur is a 44-V n-epi bipolar process that includes isolated high-speed PNPs, metal-nitride-poly capacitors, p-channel JFETs, as well as the common bipolar devices. In other bipolar processes, the capacitors have one plate made from silicon substrate (bottom) and the other from metal. At low levels of operating current, the leakage current from the silicon bottom plate can significantly impact the dc performance of the circuits. The ac performance is also affected by the parasitic substrate capacitance. Use of the metal-nitride-poly capacitor significantly reduces these effects, yielding higher ac performance and stable bias currents.

FEATURES IN THIS BOOK

- Excalibur-process devices
- Selected Macromodels (Level I)
- Expanded product characterization over supply voltage and temperature
- Extensive graphs showing the characterizations
- New 3-V devices that are specifically designed, characterized, and tested for operation at 3.3 V or less

The first section of each volume contains an alphanumeric listing, a selection guide, and a cross reference for each type of device. The alphanumeric listing in the book includes all the devices contained in volumes A and B of the Operational Amplifier/Comparator Data Book. The sections in each book are numbered consecutively across volumes (sections 1, 2, and 3 are in volume A and sections 4, 5, 6, 7 are in volume B). Thus, the reader can easily find the particular volume for a given device.

Because of the great number of devices available from TI, the selection guide for the operational amplifiers is broken down into eight primary categories with an complete alphanumeric listing at the end. The comparator selection guide is a complete alphanumeric listing. The cross references in section one help to identify devices that are comparable to other manufacturers and older TI parts.

The last section in each volume contains ordering information and mechanical data for the devices in that particular volume.

While these volumes offer information only on the operational amplifier and comparator devices available now from TI, complete technical data for upcoming analog or any other TI semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
Literature Response Center
P.O. Box 809066
Dallas, Texas 75380-9066

We feel that the Operational Amplifier/Comparator Data Book (volumes A and B) will be significant additions to your library of technical literature from Texas Instruments.

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INTRODUCTION

This selection guide is designed to help you quickly identify which operational amplifiers best suit your needs. This section includes specification tables for each operational amplifier, sorted by the primary performance category; this permits a quick comparison of key specifications, enabling a final decision on which amplifier is best for you. Also included in this section is a complete alphanumerically sorted list of all Texas Instruments advanced linear amplifiers with key specifications.

DEFINITION OF TERMS

This selection guide is broken into eight primary-selection categories:

- DC precision
- Single supply
- Noise
- Low voltage
- High speed
- Low power
- Rail to rail
- High temperature

These categories are then subdivided into secondary and tertiary groups combining performance indices. An understanding of what is meant by each term is helpful when choosing the right amplifier for your application.

DC Precision

Precision refers to an amplifier's inherent dc errors, the input offset voltage (V_{IO}), its temperature coefficient (α_{VIO}), and long-term drift (ΔV_{IO}). In direct-coupled applications, these errors are amplified by the amplifier and carried through the system. The magnitude of the input offset voltage limits the minimum signal level that can be accurately measured. This document defines precision operational amplifiers as those having $V_{IO} \leq 1$ mV. In the precision-operational-amplifiers specification table, these operational amplifiers are sorted in ascending order of V_{IO}max at 25°C; the α_{VIO} specification is also provided for comparison.

Single Supply

Single-supply operational amplifiers are those that are designed to operate well with only one power-supply rail, typically 5 V. They are generally characterized as having a common-mode input voltage range (V_{ICR}) that includes ground and outputs that can swing to or very near ground ($V_{OL} \approx 0$ V). Most single-supply operational amplifiers are manufactured using CMOS technology, although some bipolar single-supply amplifiers are available. Single-supply operational amplifiers can be used in systems with split supplies (e.g., ±5 V), but care must be taken not to exceed the maximum supply voltage across the device. For example, V_{DD}max for CMOS operational amplifiers is 16 V. No more than ±8 V should be applied to these devices in a split-supply system. Also, some single-supply operational amplifier output stages are not designed to both source and sink current; when used with split supplies, they may exhibit some crossover distortion as the signal passes through midsupply.

Rail to Rail

Rail-to-rail operational amplifiers feature outputs that swing close to both the positive and negative supply rails. To achieve expected results, maintain loading conditions within the specified drive capability of the amplifier; output swing decreases as load increases.

Noise

Noise in operational amplifiers typically has two components: voltage noise and current noise. Current noise is primarily a function of input bias currents (I_{IB}) and is negligible in JFET-input (BiFET) and CMOS amplifiers. Voltage noise (V_n) is noise generated by the amplifier due to the thermal noise of the channel resistance in JFET and CMOS amplifiers or the emitter resistance in bipolar amplifiers. Bipolar technology offers the lowest voltage noise and offers the greatest advantage when interfacing to low-impedance sources. As source impedance increases to about 10 kΩ, system noise is dominated by the thermal noise of the source and feedback resistances and selection of an amplifier is usually driven by other characteristics. At higher source impedances, the noise contribution due to the high-input currents of bipolar amplifiers becomes prohibitive and either a CMOS or BiFET amplifier should be chosen. Amplifiers in the low-noise operational amplifier sections have $V_n \leq 15\ nV/\sqrt{Hz}$. Current noise, though not specified, can be approximated by:

$$I_n \approx \sqrt{(2 \times q \times I_{IB})}, \text{ where } q = 1.6 \times 10^{-19}$$

Low Voltage

Low-voltage amplifiers operate with V_{CC} or $V_{DD} \leq 3$ V. Some CMOS amplifiers operate with $V_{DD} = 1.4$ V. When using any supply voltage, you must ensure that input signals are within the common-mode input voltage range (V_{ICR}) of the device. To address the emerging 3-V device market, Texas Instruments has introduced a full line of 3-V operational amplifiers, the TLV series of devices.

High Speed

Speed refers to an operational amplifier's slew rate (SR) and its bandwidth. Slew rate describes the ability of the amplifier's output to follow a large rapidly changing signal at its input, expressed in V/μs. Slew rate is a function of and inversely proportional to supply current (I_{CC} or I_{DD}); increased power consumption must often be traded for faster output response. BiFET amplifiers have traditionally offered the best speed performance, although new complementary bipolar technologies are gaining ground. The high-speed operational amplifiers in this selection guide have a bandwidth ≥ 6 MHz; the amplifiers' slew rate is included in the specification tables for reference.

Low Power

Low power in this document refers to amplifiers whose quiescent currents are less than 500 μA. This category is further broken down to delineate micropower amplifiers, or those with I_{CC} or $I_{DD} \leq 250$ μA. The supply current is specified under no-load conditions; the outputs neither sink nor source current. To minimize power consumption, unused amplifiers should be connected as unity-gain followers with their inputs grounded.

High Temperature

High-temperature operational amplifiers are those manufactured using Texas Instruments patent-pending high temperature and high-reliability process. These operational amplifiers perform reliably at temperatures up to 150°C and are well suited for automotive and geophysical (down-hole) applications where temperatures often exceed the industrial or military temperature ranges.

TEXAS INSTRUMENTS
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PRECISION OPERATIONAL AMPLIFIERS
V_{IO}max ≤ 1 mV

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC2652A	0.001	0.03	2.4	0.004	140	23	2.8	1.9	C, I, M	Single, chopper stabilized	2–993
TLC2652	0.003	0.03	2.4	0.004	140	23	2.8	1.9	C, I, M	Single, chopper stabilized	2–993
TLC2654A	0.01	0.3	2.4	0.05	125	13	2	1.9	C, I, M	Single, chopper stabilized	2–1017
TLC2654	0.02	0.3	2.4	0.05	125	13	2	1.9	C, I, M	Single, chopper stabilized	2–1017
TLE2027A	0.025	0.6	4.7	15	131	3.3	2.8	13	C, I, M	Single, low noise, high speed	5–83
TLE2037A	0.025	0.2	4.7	15	131	3.3	2.8	76	C, I, M	Single, low noise, high speed, decompensated	5–109
TLE2027	0.1	1	5.3	15	131	3.3	2.8	13	C, I, M	Single, low noise, high speed	5–83
TLE2037	0.1	0.4	5.3	15	131	3.3	2.8	76	C, I, M	Single, low noise, high speed, decompensated	5–109
OP07C	0.15	0.5	—	1.8	120	9.8	0.3	—	C	Single, ultra-low offset voltage	2–95
OP07D	0.15	0.5	—	2	110	9.8	0.3	—	C	Single, ultra-low offset voltage	2–95
LT1013A	0.15	0.4	0.5	12	117	22	0.4	—	C, I, M	Dual, precision	2–51
TLE2022B	0.15	0.3	0.35	25	105	15	0.65	2.8	C, I, M	Dual, low power, high speed	5–29
TLC2201A	0.2	0.5	1.5	0.001	110	8	2.5	1.8	C, I, M	Single, low noise, rail-to-rail output	2–795
TLE2021A	0.2	2	0.3	25	115	15	0.65	2	C, I, M	Single, low noise, high speed	5–3
LT1013	0.3	0.4	0.55	15	117	22	0.4	—	C, I, M	Dual, precision	2–51
TLE2022A	0.3	2	0.35	25	102	15	0.65	2.8	C, I, M	Dual, low power, high speed	5–29
TLE2227	0.35	0.4	5.3	15	115	2.5	2.5	13	C	Dual, low noise, high speed	5–547
TLE2237	0.35	0.4	5.3	15	115	2.5	5	50	C	Dual, low noise, high speed, decompensated	5–569
TLC1078	0.45	1.1	0.017	0.0006	95	68	0.032	0.085	C, I, M	Dual, low voltage, micropower	2–763
TLC277	0.5	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, single supply, low power	2–537
TLC27L7	0.5	1.1	0.017	0.0006	94	68	0.03	0.085	C, I, M	Dual, single supply, micropower	2–625
TLC27M7	0.5	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Dual, single supply, low power	2–693
TLC2201	0.5	0.5	1.5	0.001	110	8	2.5	1.8	C, I, M	Single, low noise, rail-to-rail output	2–795
TLC2202A	0.5	0.5	1.2	0.001	110	8	2.5	1.8	C, I, M	Single, low noise, rail-to-rail output	2–825
TLE2021	0.5	2	0.3	25	115	15	0.65	2	C, I, M	Single, low power, high speed	5–3
TLE2022	0.5	2	0.35	25	100	15	0.65	2.8	C, I, M	Dual, low power, high speed	5–29
TLE2024B	0.5	2	0.35	40	108	15	0.7	2.8	C, I, M	Quad, low power, high speed	5–57
TLE2141A	0.5	1.7	4.5	–700	108	10.5	45	6	C, I, M	Single, high speed, high output drive, low noise	5–435
TLE2024A	0.75	2	0.35	45	105	15	0.7	2.8	C, I, M	Quad, low power, high speed	5–57
TLE2142A	0.75	1.7	4.5	–700	108	10.5	45	6	C, I, M	Dual, high speed, high output drive, low noise	5–463

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

PRECISION OPERATIONAL AMPLIFIERS (Continued)
V_{IO}max ≤ 1 mV

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
LT1013D	0.8	0.7	0.55	15	114	22	0.4	—	C, I, M	Dual, precision	2–51
TL031A	0.8	5.9	0.28	0.2	94	41	5.1	1.1	C, I, M	Single, JFET input, low power	2–115
TL032A	0.8	10.8	0.28	0.2	94	41	5.1	1.1	C, I, M	Dual, JFET input, low power	2–143
TL051A	0.75	8	3.2	0.2	93	18	23.7	3.1	C, I, M	Single, JFET input, high speed, precision	2–199
TL052A	0.8	8	2.8	0.2	93	19	20.7	3	C, I, M	Dual, JFET input, high speed, precision	2–229
TLC1079	0.85	1.1	0.017	0.0006	95	68	0.032	0.085	C, I, M	Quad, precision, low voltage, micropower	2–779
TLC279	0.9	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Quad, precision, single supply, low power	2–573
TLC27L9	0.9	1.1	0.017	0.0006	94	70	0.03	0.085	C, I, M	Quad, precision, low voltage, micropower	2–657
TLC27M9	0.9	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, precision, single supply, low power	2–727
TLE2141	0.9	1.7	4.5	–700	108	10.5	45	6	C, I, M	Single, high speed, high output drive, low noise	5–435
TLC2262A	0.95	2	0.25	0.001	80	12	0.55	0.82	I	Dual, precision, low power, rail-to-rail output, low noise	2–855
TLC2264A	0.95	2	0.25	0.001	83	12	0.55	0.82	I	Quad, low power, rail-to-rail output, low noise	2–889
TLC2272A	0.95	2	3	0.001	75	9	3.6	2.18	C, I, M	Dual, rail-to-rail output, precision	2–923
TLC2274A	0.95	2	3	0.001	75	9	3.6	2.18	C, M	Dual, rail-to-rail output, precision	2–957
TLV2262A	0.95	2	0.25	0.001	77	12	0.55	0.82	I	Dual, low voltage, rail-to-rail output, low noise	5–695
TLV2264A	0.95	2	0.25	0.001	80	12	0.55	0.82	I	Quad, low voltage, rail-to-rail output, low noise	5–725
TLC2202	1	0.5	1.2	0.001	110	8	2.5	1.9	C, I, M	Dual, precision, low noise, rail-to-rail output	2–825
TLE2024	1	2	0.35	50	102	15	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

DEVICE	V_{CC} V (min–max)	V_{IO} mV (max)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC251 (high bias)	1.4 – 16	10	1.6	0.0006	80	25	3.6	1.7	C	Single, low voltage, programmable power	2–411
TLC251A (high bias)	1.4 – 16	5	1.6	0.0006	80	25	3.6	1.7	C	Single, low voltage, programmable power	2–411
TLC251B (high bias)	1.4 – 16	2	1.6	0.0006	80	25	3.6	1.7	C	Single, low offset, programmable power	2–411
TLC251 (medium bias)	1.4 – 16	10	0.28	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251A (medium bias)	1.4 – 16	5	0.28	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251B (medium bias)	1.4 – 16	2	0.28	0.0006	91	32	0.43	0.525	C	Single, low offset, programmable power	2–411
TLC251 (low bias)	1.4 – 16	10	0.017	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251A (low bias)	1.4 – 16	10	0.017	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251B (low bias)	1.4 – 16	2	0.017	0.0006	94	68	0.03	0.085	C	Single, low offset, programmable power	2–411
TLC252	1.4 – 16	10	1.6	0.0006	80	25	3.6	1.7	C	Dual, low voltage	2–429
TLC252A	1.4 – 16	5	1.6	0.0006	80	25	3.6	1.7	C	Dual, low voltage	2–429
TLC252B	1.4 – 16	2	1.6	0.0006	80	25	3.6	1.7	C	Dual, low voltage, low offset	2–429
TLC25L2	1.4 – 16	10	0.017	0.0006	94	68	0.03	0.085	C	Dual, low voltage, micropower	2–429
TLC25L2A	1.4 – 16	5	0.017	0.0006	80	25	3.6	1.7	C	Dual, low voltage, micropower	2–429
TLC25L2B	1.4 – 16	2	0.017	0.0006	94	68	0.03	0.085	C	Dual, low voltage, low offset, micropower	2–429
TLC25M2	1.4 – 16	10	0.28	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low power	2–429
TLC25M2A	1.4 – 16	5	0.017	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset, low power	2–429
TLC25M2B	1.4 – 16	2	0.28	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset, low power	2–429
TLC254	1.4 – 16	10	1.6	0.0006	80	25	3.6	1.7	C	Quad, low voltage	2–449
TLC254A	1.4 – 16	5	1.6	0.0006	80	25	3.6	1.7	C	Quad, low voltage	2–449
TLC254B	1.4 – 16	2	1.6	0.0006	80	25	3.6	1.7	C	Quad, low voltage, low offset	2–449
TLC25L4	1.4 – 16	10	0.017	0.0006	94	70	0.03	0.085	C	Quad, low voltage, micropower	2–449
TLC25L4A	1.4 – 16	5	0.017	0.0006	94	70	0.03	0.085	C	Quad, low voltage, micropower	2–449
TLC25L4B	1.4 – 16	2	0.017	0.0006	94	70	0.03	0.085	C	Quad, low voltage, low offset, micropower	2–449
TLC25M4	1.4 – 16	10	0.28	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low power	2–449
TLC25M4A	1.4 – 16	5	0.28	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low power	2–449
TLC25M4B	1.4 – 16	2	0.28	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low offset, micropower	2–449
TLC1078	1.4 – 16	0.45	0.017	0.0006	95	68	0.032	0.085	C, I, M	Dual, precision, low voltage, micropower	2–763
TLC1079	1.4 – 16	0.85	0.017	0.0006	95	68	0.032	0.085	C. I, M	Quad, precision, low voltage, micropower	2–779
TLV2362	2 – 5	6	2.5	20	85	8	3	7	I	Dual, low voltage, low noise, high speed	5–949

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

SINGLE-SUPPLY OPERATIONAL AMPLIFIERS (Continued)

DEVICE	V_{CC} V (min–max)	V_{IO} mV (max)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLV2322	2 – 8	9	0.017	0.0006	94	68	0.03	0.085	I	Dual, low voltage, micropower	5–755
TLV2332	2 – 8	9	0.28	0.0006	91	32	0.43	0.525	I	Dual, low voltage, low power	5–803
TLV2342	2 – 8	9	1.6	0.0006	80	25	3.6	1.7	I	Dual, low voltage	5–901
TLV2324	2 – 8	10	0.017	0.0006	94	68	0.03	0.085	I	Quad, low voltage, micropower	5–779
TLV2334	2 – 8	10	0.28	0.0006	91	32	0.43	0.525	I	Quad, low voltage, low power	5–763
TLV2344	2 – 8	10	1.6	0.0006	80	25	3.6	1.7	I	Quad, low voltage	5–925
TLV2341 (high bias)	2 – 8	8	1.6	0.0006	80	25	3.6	1.7	I	Single, low voltage, programmable power	5–851
TLV2341 (medium bias)	2 – 8	8	0.28	0.0006	91	32	0.43	0.525	I	Single, low voltage, programmable power	5–851
TLV2341 (low bias)	2 – 8	8	0.017	0.0006	94	68	0.03	0.085	I	Single, low voltage, programmable power	5–851
TLV2262	2.7 – 8	2.5	0.25	0.001	80	12	0.55	0.82	C, I	Dual, low voltage, low noise, rail to rail	5–695
TLV2262A	2.7 – 8	0.95	0.25	0.001	80	12	0.55	0.82	C, I	Dual, precision, low noise, rail to rail	5–695
TLV2264	2.7 – 8	2.5	0.25	0.001	80	12	0.55	0.82	I	Quad, low voltage, low noise, rail to rail	5–725
TLV2264A	2.7 – 8	0.95	0.25	0.001	80	12	0.55	0.82	I	Quad, precision, low noise, rail to rail	5–725
TLC2262	2.7 – 16	25	0.25	0.001	80	12	0.55	0.82	C, I	Dual, low power, low noise, rail to rail	2–855
TLC2262A	2.7 – 16	0.95	0.25	0.001	80	12	0.55	0.82	C, I	Dual, precision, low noise, rail to rail	2–855
TLC2264	2.7 – 16	25	0.25	0.001	80	12	0.55	0.82	C, I	Quad, low power, low noise, rail to rail	2–889
TLC2264A	2.7 – 16	0.95	0.25	0.001	80	12	0.55	0.82	I	Quad, precision, low noise, rail to rail	2–889
TLV2362	3 – 7	6	5	20	85	9	3	7	C, I	Dual, low voltage, high speed	5–949
TLC271 (high bias)	3 – 16	10	1.6	0.0006	80	25	3.6	1.7	C, I, M	Single, low voltage, programmable power	2–469
TLC271A (high bias)	3 – 16	5	1.6	0.0006	80	25	3.6	1.7	C, I, M	Single, low voltage, programmable power	2–469
TLC271B (high bias)	3 – 16	2	1.6	0.0006	80	25	3.6	1.7	C, I, M	Single, low offset, programmable power	2–469
TLC271 (medium bias)	3 – 16	10	0.28	0.0006	91	32	0.43	0.525	C, I, M	Single, low voltage, programmable power	2–469
TLC271A (medium bias)	3 – 16	5	0.28	0.0006	91	32	0.43	0.525	C, I, M	Single, low voltage, programmable power	2–469
TLC271B (medium bias)	3 – 16	2	0.28	0.0006	91	32	0.43	0.525	C, I, M	Single, low offset, programmable power	2–469
TLC271 (low bias)	3 – 16	10	0.17	0.0006	94	68	0.03	0.085	C, I, M	Single, low voltage, programmable power	2–469
TLC271A (low bias)	3 – 16	10	0.17	0.0006	94	68	0.03	0.085	C, I, M	Single, low voltage, programmable power	2–469
TLC271B (low bias)	3 – 16	2	0.17	0.0006	94	68	0.03	0.085	C, I, M	Single, low offset, programmable power	2–469
TLC272	3 – 16	10	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, low voltage	2–537
TLC272A	3 – 16	5	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, low voltage	2–537
TLC272B	3 – 16	2	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, low voltage, low offset	2–537

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SINGLE-SUPPLY OPERATIONAL AMPLIFIERS (Continued)

DEVICE	V_{CC} V (min–max)	V_{IO} mV (max)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC27L2	3 – 16	10	0.017	0.0006	94	68	0.03	0.085	C, I, M	Dual, low voltage, micropower	2–625
TLC27L2A	3 – 16	5	0.017	0.0006	80	25	3.6	1.7	C, I, M	Dual, low voltage, micropower	2–625
TLC27L2B	3 – 16	2	0.017	0.0006	94	68	0.03	0.085	C, I, M	Dual, low voltage, low offset, micropower	2–625
TLC27M2	3 – 16	10	0.28	0.0006	91	32	0.43	0.525	C, I, M	Dual, low voltage, low power	2–693
TLC27M2A	3 – 16	5	0.017	0.0006	91	32	0.43	0.525	C, I, M	Dual, low voltage, low offset, low power	2–693
TLC27M2B	3 – 16	2	0.28	0.0006	91	32	0.43	0.525	C, I, M	Dual, low voltage, low offset, low power	2–693
TLC274	3 – 16	10	1.6	0.0006	80	25	3.6	1.7	C, I, M	Quad, low voltage	2–573
TLC274A	3 – 16	5	1.6	0.0006	80	25	3.6	1.7	C, I, M	Quad, low voltage	2–573
TLC274B	3 – 16	2	1.6	0.0006	80	25	3.6	1.7	C, I, M	Quad, low voltage, low offset	2–573
TLC274x2	3 – 16	10	1.6	0.0006	80	25	3.6	1.7	C, I, M	Octal, low voltage	2–609
TLC27L4	3 – 16	10	0.017	0.0006	94	70	0.03	0.085	C, I, M	Quad, low voltage, micropower	2–657
TLC27L4A	3 – 16	5	0.017	0.0006	94	70	0.03	0.085	C, I, M	Quad, low voltage, micropower	2–657
TLC27L4B	3 – 16	2	0.017	0.0006	94	70	0.03	0.085	C, I, M	Quad, low voltage, low offset, micropower	2–657
TLC27M4	3 – 16	10	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, low voltage, low power	2–727
TLC27M4A	3 – 16	5	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, low voltage, low power	2–727
TLC27M4B	3 – 16	2	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, low voltage, low offset, micropower	2–727
TLC277	3 – 16	0.5	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, precision, single supply, low power	2–537
TLC279	3 – 16	0.9	1.6	0.0006	80	25	3.6	1.7	C, I, M	Quad, precision, single supply, low power	2–573
TLC27L7	3 – 16	0.5	0.017	0.0006	94	68	0.3	0.085	C, I, M	Dual, precision, single supply, micropower	2–625
TLC27L9	3 – 16	0.9	0.017	0.0006	94	70	0.3	0.085	C, I, M	Quad, precision, single supply, micropower	2–657
TLC27M7	3 – 16	0.5	0.28	0.0006	91	32	0.43	0.525	C, I, M	Dual, precision, single supply, low power	2–693
TLC27M9	3 – 16	0.9	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, precision, single supply, low power	2–727
LM2904	3 – 26	7	2	–20	80	—	0.2	—	Q	Dual, high gain, low power, bipolar	2–29
LM2904Q	3 – 26	7	2	–20	80	—	0.2	—	Q	Dual, high gain, low power, bipolar	2–29
LM158	3 – 30	5	2	–20	80	—	0.2	—	M	Dual, high gain, low power, bipolar	2–29
LM158A	3 – 30	2	2	–15	80	—	0.2	—	M	Dual, high gain, low power, bipolar	2–29
LM258	3 – 30	5	2	–20	80	—	0.2	—	I	Dual, high gain, low power, bipolar	2–29
LM258A	3 – 30	3	2	–15	80	—	0.2	—	I	Dual, high gain, low power, bipolar	2–29
LM358	3 – 30	7	2	–20	80	—	0.2	—	C	Dual, high gain, low power, bipolar	2–29
LM358A	3 – 30	3	2	–15	80	—	0.2	—	C	Dual, high gain, low power, bipolar	2–29

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C, Q = –40°C to 105°C

SINGLE-SUPPLY OPERATIONAL AMPLIFIERS (Continued)

DEVICE	V_{CC} V (min – max)	V_{IO} mV (max)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLE2021	4 – 40	0.5	0.3	25	115	15	0.65	2	C, I, M	Single, precision, low power, high speed	5–3
TLE2021A	4 – 40	0.2	0.3	25	115	15	0.65	2	C, I, M	Single, precision, low power, high speed	5–3
TLE2022	4 – 40	0.5	0.35	25	100	15	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2022A	4 – 40	0.3	0.35	25	102	15	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2022B	4 – 40	0.15	0.35	25	105	15	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2024	4 – 40	1	0.35	50	102	15	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2024A	4 – 40	0.75	0.35	45	105	15	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2024B	4 – 40	0.5	0.35	40	108	15	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2141	4 – 38	0.9	4.5	–700	108	10.5	45	6	C, I, M	Single, precision, high speed, high output drive, low noise	5–435
TLE2141A	4 – 38	0.5	4.5	–700	108	10.5	45	6	C, I, M	Single, precision, high speed, high output drive, low noise	5–435
TLE2142	4 – 38	1.2	4.5	–700	108	10.5	45	6	C, I, M	Dual, precision, high output drive, low noise	5–463
TLE2142A	4 – 38	0.75	4.5	–700	108	10.5	45	6	C, I, M	Dual, precision, high speed, high output drive, low noise	5–463
TLE2144	4 – 38	2.4	4.5	–700	108	10.5	45	6	C, I, M	Quad, precision, high speed, high output drive, low noise	5–491
TLE2144A	4 – 38	1.5	4.5	–700	108	10.5	45	6	C, I, M	Quad, precision, high speed, high output drive, low noise	5–491
TLC2272	4.4 – 16	2.5	1.5	0.001	75	9	3.6	2.18	C, I, M	Quad, low noise, rail to rail	2–923
TLC2272A	4.4 – 16	0.95	1.5	0.001	75	9	3.6	2.18	C, I, M	Quad, precision, low noise, rail to rail	2–923
LM2900	4.5 – 32	—	6.2	30	—	—	0.6	—	I	Quad, Norton amplifier, bipolar	2–43
LM3900	4.5 – 32	—	6.2	30	—	—	0.6	—	C	Quad, Norton amplifier, bipolar	2–43
TLC2201	4.6 – 16	0.5	1.5	0.001	110	8	2.5	1.8	C, I, M	Single, precision, low noise, rail-to-rail output	2–795
TLC2201A	4.6 – 16	0.2	1.5	0.001	110	8	2.5	1.8	C, I, M	Single, precision, low noise, rail-to-rail output	2–795
TLC2202	4.6 – 16	1	1.2	0.001	110	8	2.5	1.9	C, I, M	Dual, precision, low noise, rail-to-rail output	2–825
TLC2652	4.6 – 16	0.003	1.2	0.004	140	23	2.8	1.9	C, I, M	Single, precision, chopper stabilized	2–993
TLC2652A	4.6 – 16	0.001	2.4	0.004	140	23	2.8	1.9	C, I, M	Single, precision, chopper stabilized	2–993
TLC2654	4.6 – 16	0.02	2.4	0.05	125	13	2	1.9	C, I, M	Single, precision, chopper stabilized	2–1017
TLC2654A	4.6 – 16	0.01	2.4	0.05	125	13	2	1.9	C, I, M	Single, precision, chopper stabilized	2–1017
MC3303	5 – 30	8	7	–200	90	—	0.6	—	I	Quad, low power, bipolar	2–79
MC3403	5 – 30	10	7	–200	90	—	0.6	—	C	Quad, low power, bipolar	2–79

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

LOW-NOISE OPERATIONAL AMPLIFIERS
$V_n$typ ≤ 15 nV/√Hz

DEVICE	V_n (1 kHz) nV/√Hz (typ)	V_{IO} mV (max)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLE2027	2.5	0.1	5.3	15	131	2.8	13	C, I, M	Single, low noise, high speed, precision	5–83
TLE2027A	2.5	0.025	4.7	15	131	2.8	13	C, I, M	Single, low noise, high speed, precision	5–83
TLE2037	2.5	0.1	5.3	15	131	7.5	76	C, I, M	Single, low noise, high speed, precision, decompensated	5–109
TLE2037A	2.5	0.025	4.7	15	131	7.5	76	C, I, M	Single, low noise, high speed, precision, decompensated	5–109
TLE2227	2.5	0.35	5.3	15	115	2.5	13	C	Dual, precision, low noise, high speed	5–547
TLE2237	2.5	0.35	5.3	15	115	5	50	C	Dual, precision, low noise, high speed, decompensated	5–569
SE5534A	3.5	2	6.5	400	100	13	—	M	Single, low noise, high performance	2–89
NE5534	4	4	8	500	100	13	—	C	Single, low noise, high performance	2–89
NE5534A	4	4	8	500	100	13	—	C	Single, low noise, high performance	2–89
SE5534	4	2	6.5	400	100	13	—	M	Single, low noise, high performance	2–89
NE5532	5	4	16	200	100	9	—	C, I	Dual, low noise	2–85
NE5532A	5	4	16	200	100	9	—	C, I	Dual, low noise	2–85
RC4558	8	6	5.6	5	90	1.7	—	C	Dual, high performance	2–105
RM4558	8	6	5.6	5	90	1.7	—	M	Dual, high performance	2–105
RV4558	8	6	5.6	5	90	1.7	—	I	Dual, high performance	2–105
TLC2201	8	0.5	1.5	0.001	110	2.5	1.8	C, I, M	Single, precision, low noise, rail-to-rail output	2–795
TLC2201A	8	0.2	1.5	0.001	110	2.5	1.8	C, I, M	Single, precision, low noise, rail-to-rail output	2–795
TLC2202	8	1	1.2	0.001	110	2.5	1.9	C, I, M	Dual, precision, low noise, rail-to-rail output	2–825
TLC2202A	8	0.5	1.2	0.001	110	2.5	1.9	C, I, M	Dual, precision, low noise, rail-to-rail output	2–825
TLC2801	8	0.5	1.5	0.001	110	2.5	1.8	Z	Single, precision, low noise, rail-to-rail output, high temperature	2–1041
TLC2872	9	2.5	3	0.001	75	3.6	2.18	Z	Dual, rail-to-rail output, low noise, high temperature	2–1073
TLC2272	9	2.5	3	0.001	75	3.6	2.18	C, I, M	Dual, rail-to-rail output, low noise	2–923
TLC2272A	9	0.95	3	0.001	75	3.6	2.18	C, I, M	Dual, rail-to-rail output, precision, low noise	2–923
TLC2274	9	2.5	3	0.001	75	3.6	2.18	C, I, M	Quad, rail-to-rail output, low noise	2–957
TLC2274A	9	0.95	3	0.001	75	3.6	2.18	C, I, M	Quad, rail-to-rail output, precision, low noise	2–957
TLE2141	10.5	0.9	4.5	−700	108	45	6	C, I, M	Single, precision, high speed, high output drive, low noise	5–435
TLE2141A	10.5	0.5	4.5	−700	108	45	6	C, I, M	Single, precision, high speed, high output drive, low noise	5–435
TLE2142	10.5	1.2	4.5	−700	108	45	6	C, I, M	Dual, precision, high speed, high output drive, low noise	5–463
TLE2142A	10.5	0.75	4.5	−700	108	45	6	C, I, M	Dual, precision, high speed, high output drive, low noise	5–463
TLE2144	10.5	2.4	4.5	−700	108	45	6	C, I, M	Quad, precision, high speed, high output drive, low noise	5–491

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C, Z = −40°C to 150°C

LOW-NOISE OPERATIONAL AMPLIFIERS (Continued)
$V_n$typ ≤ 15 nV/√Hz

DEVICE	V_n (1 kHz) nV/√Hz (typ)	V_{IO} mV (max)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLE2144A	10.5	1.5	4.5	−700	108	45	6	C, I, M	Quad, precision, high speed, high output drive, low noise	5–491
TLE2071	11.6	4	2.2	0.02	98	40	10	C, I, M	Single, high speed, low noise, JFET input	5–227
TLE2071A	11.6	2	2.2	0.02	98	40	10	C, I, M	Single, high speed, low noise, JFET input	5–227
TLE2072	11.6	6	1.8	0.02	98	40	10	C, I, M	Dual, high speed, low noise, JFET input	5–263
TLE2072A	11.6	3.5	1.8	0.02	98	40	10	C, I, M	Dual, high speed, low noise, JFET input	5–263
TLE2074	11.6	5	1.875	0.025	98	40	10	C, I, M	Quad, high speed, low noise, JFET input	5–299
TLE2074A	11.6	3	1.875	0.025	98	40	10	C, I, M	Quad, high speed, low noise, JFET input	5–299
TLE2081	11.6	6	2.2	0.02	98	40	10	C, I, M	Single, high speed, JFET input	5–335
TLE2081A	11.6	3	2.2	0.02	98	40	10	C, I, M	Single, high speed, JFET input	5–335
TLE2082	11.8	7	1.8	0.02	98	40	10	C, I, M	Dual, high speed, JFET input	5–367
TLE2082A	11.8	4	1.8	0.02	98	40	10	C, I, M	Dual, high speed, JFET input	5–367
TLE2084	11.6	7	1.875	0.025	98	40	10	C, I, M	Quad, high speed, JFET input	5–403
TLE2084A	11.6	4	1.875	0.025	98	40	10	C, I, M	Quad, high speed, JFET input	5–403
TLC2654	13	0.020	2.4	0.05	125	2	1.9	C, I, M	Single, precision, chopper stabilized	2–1017
TLC2654A	13	0.010	2.4	0.05	125	2	1.9	C, I, M	Single, precision, chopper stabilized	2–1017
TLE2021	15	0.5	0.3	25	115	0.65	2	C, I, M	Single, precision, low power, high speed	5–3
TLE2021A	15	0.2	0.3	25	115	0.65	2.8	C, I, M	Single, precision, low power, high speed	5–3
TLE2022	15	0.5	0.35	25	100	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2022A	15	0.3	0.35	25	102	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2022B	15	0.15	0.35	25	105	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2024	15	1	0.35	50	102	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2024A	15	0.75	0.35	45	105	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2024B	15	0.5	0.35	40	108	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

LOW-VOLTAGE OPERATIONAL AMPLIFIERS
V_{CC}min ≤ 3 V

DEVICE	V_{CC} V (min – max)	V_{IO} mV (max)	I_{CC} mA (max)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC251 (high bias)	1.4 – 16	10	1.6	80	25	3.6	1.7	C	Single, low voltage, programmable power	2–411
TLC251A (high bias)	1.4 – 16	5	1.6	80	25	3.6	1.7	C	Single, low voltage, programmable power	2–411
TLC251B (high bias)	1.4 – 16	2	1.6	80	25	3.6	1.7	C	Single, low voltage, low offset, programmable power	2–411
TLC251 (medium bias)	1.4 – 16	10	0.28	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251A (medium bias)	1.4 – 16	5	0.28	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251B (medium bias)	1.4 – 16	2	0.28	91	32	0.43	0.525	C	Single, low voltage, low offset, programmable power	2–411
TLC251 (low bias)	1.4 – 16	10	0.017	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251A (low bias)	1.4 – 16	5	0.017	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251B (low bias)	1.4 – 16	2	0.017	94	68	0.03	0.085	C	Single, low voltage, low offset, programmable power	2–411
TLC252	1.4 – 16	10	1.6	80	25	3.6	1.7	C	Dual, low voltage	2–429
TLC252A	1.4 – 16	5	1.6	80	25	3.6	1.7	C	Dual, low voltage	2–429
TLC252B	1.4 – 16	2	1.6	80	25	3.6	1.7	C	Dual, low voltage, low offset	2–429
TLC25L2	1.4 – 16	10	0.017	94	68	0.03	0.085	C	Dual, low voltage, micropower	2–429
TLC25L2A	1.4 – 16	5	0.017	94	68	0.03	0.085	C	Dual, low voltage, micropower	2–429
TLC25L2B	1.4 – 16	2	0.017	94	68	0.03	0.085	C	Dual, low voltage, low offset, micropower	2–429
TLC25M2	1.4 – 16	10	0.28	91	32	0.43	0.525	C	Dual, low voltage, low power	2–429
TLC25M2A	1.4 – 16	5	0.28	91	32	0.43	0.525	C	Dual, low voltage, low power	2–429
TLC25M2B	1.4 – 16	2	0.28	91	32	0.43	0.525	C	Dual, low voltage, low offset, low power	2–429
TLC254	1.4 – 16	10	1.6	80	25	3.6	1.7	C	Quad, low voltage	2–449
TLC254A	1.4 – 16	5	1.6	80	25	3.6	1.7	C	Quad, low voltage	2–449
TLC254B	1.4 – 16	2	1.6	80	25	3.6	1.7	C	Quad, low voltage, low offset	2–449
TLC25L4	1.4 – 16	10	0.017	94	70	0.03	0.085	C	Quad, low voltage, micropower	2–449
TLC25L4A	1.4 – 16	5	0.017	94	70	0.03	0.085	C	Quad, low voltage, micropower	2–449
TLC25L4B	1.4 – 16	2	0.017	94	70	0.03	0.085	C	Quad, low voltage, low offset, micropower	2–449
TLC25M4	1.4 – 16	10	0.28	91	32	0.43	0.525	C	Quad, low voltage, low power	2–449
TLC25M4A	1.4 – 16	5	0.28	91	32	0.43	0.525	C	Quad, low voltage, low power	2–449
TLC25M4B	1.4 – 16	2	0.28	91	32	0.43	0.525	C	Quad, low voltage, low offset, micropower	2–449
TLC1078	1.4 – 16	0.45	0.017	95	68	0.032	0.085	C, I, M	Dual, precision, low voltage, micropower	2–763
TLC1079	1.4 – 16	0.85	0.017	95	68	0.032	0.085	C, I, M	Quad, precision, low voltage, micropower	2–779
TLV2322	2 – 8	9	0.017	94	68	0.03	0.085	I	Dual, low voltage, micropower	5–755

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

LOW-VOLTAGE OPERATIONAL AMPLIFIERS (Continued)
V_{CC}min ≤ 3 V

DEVICE	V_{CC} V (min – max)	V_{IO} mV (max)	I_{CC} mA (max)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLV2332	2 – 8	9	0.28	91	32	0.43	0.525	I	Dual, low voltage, low power	5–803
TLV2342	2 – 8	9	1.6	80	25	3.6	1.7	I	Dual, low voltage	5–901
TLV2324	2 – 8	10	0.017	94	68	0.03	0.085	I	Quad, low voltage, micropower	5–779
TLV2334	2 – 8	10	0.28	91	32	0.43	0.525	I	Quad, low voltage, low power	5–827
TLV2344	2 – 8	10	1.6	80	25	3.6	1.7	I	Quad, low voltage	5–925
TLV2341 (high bias)	2 – 8	8	1.6	80	25	3.6	1.7	I	Single, low voltage, programmable power	5–851
TLV2341 (medium bias)	2 – 8	8	0.28	91	32	0.43	0.525	I	Single, low voltage, programmable power	5–851
TLV2341 (low bias)	2 – 8	8	0.017	94	68	0.03	0.085	I	Single, low voltage, programmable power	5–851
TLV2262	2.7 – 8	25	0.250	80	12	0.55	0.82	C, I	Dual, low power	5–695
TLV2262A	2.7 – 8	0.95	0.25	80	12	0.55	0.82	C, I	Dual, low power, precision	5–695
TLV2264	2.7 – 8	25	0.250	80	12	0.55	0.82	C, I	Quad, low power	5–725
TLV2264A	2.7 – 8	0.95	0.25	80	12	0.55	0.82	C, I	Quad, low power, precision	5–725
TLV2362	3 – 7	6	5	85	9	3	7	C, I	Dual, high speed	5–949
TLC271 (high bias)	3 – 16	10	1.6	80	25	3.6	1.7	C, I, M	Single, programmable power	2–469
TLC271A (high bias)	3 – 16	5	1.6	80	25	3.6	1.7	C, I, M	Single, low voltage, programmable power	2–469
TLC271B (high bias)	3 – 16	2	1.6	80	25	3.6	1.7	C, I, M	Single, low voltage, low offset, programmable power	2–469
TLC271 (medium bias)	3 – 16	10	0.28	91	32	0.43	0.525	C, I, M	Single, low voltage, programmable power	2–469
TLC271A (medium bias)	3 – 16	5	0.28	91	32	0.43	0.525	C, I, M	Single, low voltage, programmable power	2–469
TLC271B (medium bias)	3 – 16	2	0.28	91	32	0.43	0.525	C, I, M	Single, low voltage, low offset, programmable power	2–469
TLC271 (low bias)	3 – 16	10	0.017	94	68	0.03	0.085	C, I, M	Single, low voltage, programmable power	2–469
TLC271A (low bias)	3 – 16	5	0.017	94	68	0.03	0.085	C, I, M	Single, low voltage, programmable power	2–469
TLC271B (low bias)	3 – 16	2	0.017	94	68	0.03	0.085	C, I, M	Single, low voltage, low offset, programmable power	2–469
TLC272	3 – 16	10	1.6	80	25	3.6	1.7	C, I, M	Dual, low voltage	2–537
TLC272A	3 – 16	5	1.6	80	25	3.6	1.7	C, I, M	Dual, low voltage	2–537
TLC272B	3 – 16	2	1.6	80	25	3.6	1.7	C, I, M	Dual, low voltage, low offset	2–537
TLC27L2	3 – 16	10	0.017	94	68	0.03	0.085	C, I, M	Dual, micropower	2–625
TLC27L2A	3 – 16	5	0.017	94	68	0.03	0.085	C, I, M	Dual, micropower	2–625
TLC27L2B	3 – 16	2	0.017	94	68	0.03	0.085	C, I, M	Dual, low offset, micropower	2–625
TLC27M2	3 – 16	10	0.28	91	32	0.43	0.525	C, I, M	Dual, low power	2–693
TLC27M2A	3 – 16	5	0.28	91	32	0.43	0.525	C, I, M	Dual, low power	2–693

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

TEXAS INSTRUMENTS
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LOW-VOLTAGE OPERATIONAL AMPLIFIERS (Continued)
V_{CC}min ≤ 3 V

DEVICE	V_{CC} V (min – max)	V_{IO} mV (max)	I_{CC} mA (max)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC27M2B	3 – 16	2	0.28	91	32	0.43	0.525	C, I, M	Dual, low offset, low power	2–693
TLC274	3 – 16	10	1.6	80	25	3.6	1.7	C, I, M	Quad, low voltage	2–573
TLC274A	3 – 16	5	1.6	80	25	3.6	1.7	C, I, M	Quad, low voltage	2–573
TLC274B	3 – 16	2	1.6	80	25	3.6	1.7	C, I, M	Quad, low voltage, low offset	2–573
TLC274x2	3 – 16	10	1.6	80	25	3.6	1.7	C, I, M	Octal, low voltage	2–609
TLC27L4	3 – 16	10	0.017	94	70	0.03	0.085	C, I, M	Quad, micropower	2–657
TLC27L4A	3 – 16	5	0.017	94	70	0.03	0.085	C, I, M	Quad, micropower	2–657
TLC27L4B	3 – 16	2	0.017	94	70	0.03	0.085	C, I, M	Quad, low offset, micropower	2–657
TLC27M4	3 – 16	10	0.28	91	32	0.43	0.525	C, I, M	Quad, low power	2–727
TLC27M4A	3 – 16	5	0.28	91	32	0.43	0.525	C, I, M	Quad, low power	2–727
TLC27M4B	3 – 16	2	0.28	91	32	0.43	0.525	C, I, M	Quad, low offset, micropower	2–727
TLC277	3 – 16	0.5	1.6	80	25	3.6	1.7	C, I, M	Dual, precision, single supply, low power	2–537
TLC279	3 – 16	0.9	1.6	80	25	3.6	1.7	C, I, M	Quad, precision, single supply, low power	2–573
TLC27L7	3 – 16	0.5	0.017	94	68	0.3	0.085	C, I, M	Dual, precision, single supply, micropower	2–625
TLC27L9	3 – 16	0.9	0.017	94	70	0.3	0.085	C, I, M	Quad, precision, single supply, micropower	2–657
TLC27M7	3 – 16	0.5	0.28	91	32	0.43	0.525	C, I, M	Dual, precision, single supply, low power	2–693
TLC27M9	3 – 16	0.9	0.28	91	32	0.43	0.525	C, I, M	Quad, precision, single supply, low power	2–727
NE5534	3 – 20	4	8	100	4	13	—	C	Single, low noise, high performance	2–89
NE5534A	3 – 20	4	8	100	4	13	—	C	Single, low noise, high performance	2–89
OP07C	3 – 20	0.15	—	120	9.8	0.3	—	C	Single, ultra-low offset voltage	2–95
OP07D	3 – 20	0.15	—	110	9.8	0.3	—	C	Single, ultra-low offset voltage	2–95
SE5534	3 – 20	2	6.5	100	3.5	13	—	M	Single, low noise, high performance	2–89
SE5534A	3 – 20	2	6.5	100	3.5	13	—	M	Single, low noise, high performance	2–89
LM2902	3 – 26	7	0.7	80	—	0.3	—	Q	Quad, general purpose, bipolar	2–17
LM2902Q	3 – 26	7	0.7	80	—	0.3	—	Q	Quad, general purpose, bipolar	2–17
LM2904	3 – 26	7	2	80	—	0.2	—	Q	Dual, high gain, low power, bipolar	2–29
LM2904Q	3 – 26	7	2	80	—	0.2	—	Q	Dual, high gain, low power, bipolar	2–29
LM124	3 – 30	5	0.7	80	—	0.13	—	M	Quad, general purpose, bipolar	2–17
LM124A	3 – 30	2	1.5	80	—	0.13	—	M	Quad, general purpose, bipolar	2–17
LM158	3 – 30	5	2	80	—	0.2	—	M	Dual, high gain, low power, bipolar	2–29

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C, Q = –40°C to 105°C

LOW-VOLTAGE OPERATIONAL AMPLIFIERS (Continued)
V_{CC}min ≤ 3 V

DEVICE	V_{CC} V (min – max)	V_{IO} mV (max)	I_{CC} mA (max)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
LM158A	3 – 30	2	2	80	—	0.2	—	M	Dual, high gain, low power, bipolar	2–29
LM224	3 – 30	5	0.7	80	—	0.3	—	I	Quad, general purpose, bipolar	2–17
LM224A	3 – 30	3	1.5	80	—	0.3	—	I	Quad, general purpose, bipolar	2–17
LM258	3 – 30	5	2	80	—	0.2	—	I	Dual, high gain, low power, bipolar	2–29
LM258A	3 – 30	3	2	80	—	0.2	—	I	Dual, high gain, low power, bipolar	2–29
LM324	3 – 30	7	0.7	80	—	0.3	—	C	Quad, general purpose, bipolar	2–17
LM324A	3 – 30	3	1.5	80	—	0.3	—	C	Quad, general purpose, bipolar	2–17
LM324x2	3 – 30	7	0.7	80	—	0.3	—	C	Octal, general purpose, bipolar	2–39
LM358	3 – 30	7	2	80	—	0.2	—	C	Dual, high gain, low power, bipolar	2–29
LM358A	3 – 30	3	2	80	—	0.2	—	C	Dual, high gain, low power, bipolar	2–29

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

HIGH-TEMPERATURE OPERATIONAL AMPLIFIERS
−40°C ≤ T_A ≤ 150°C

DEVICE	V_{IO} mV (max)	α_{VIO} μV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TL2828	7	15	1	−100	75	23	0.15	0.4	Z	Dual, high temperature, bipolar	2–391
TL2829	7	15	0.3	−100	75	23	0.25	0.4	Z	Quad, high temperature, low power, bipolar	2–397
TLC2801	0.5	0.5	1.5	0.001	110	8	2.5	1.8	Z	Single, precision, low noise, rail-to-rail output	2–1041
TLC2810	10	3.5	1.6	0.007	90	25	3.6	1.7	Z	Dual, high temperature, CMOS	2–1051
TLC2872	2.5	2	1.5	0.001	75	9	3.6	2.18	Z	Dual, low noise, high temperature	2–1073

† Z = −40°C to 150°C

TEXAS INSTRUMENTS
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HIGH-SPEED OPERATIONAL AMPLIFIERS
GBW typ > 6 MHz

DEVICE	GBW MHz (typ)	SR V/μs (typ)	V_{IO} mV (max)	αV_{IO} μV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLE2037	76	7.5	0.1	0.4	5.3	15	131	2.5	C, I, M	Single, decompensated, precision, low noise	5–109
TLE2037A	76	7.5	0.025	0.2	4.7	15	131	2.5	C, I, M	Single, decompensated, precision, low noise	5–109
TLE2237	50	5	0.35	0.4	5.3	15	115	2.5	C, I, M	Dual, precision, low noise, decompensated	5–569
TLE2071	10	40	4	3.2	2.2	0.02	98	11.6	C, I, M	Single, high speed, low noise, JFET input	5–227
TLE2071A	10	40	2	3.2	2.2	0.02	98	11.6	C, I, M	Single, high speed, low noise, JFET input	5–227
TLE2072	10	40	6	2.4	1.8	0.02	98	11.6	C, I, M	Dual, high speed, low noise, JFET input	5–263
TLE2072A	10	40	3.5	2.4	1.8	0.02	98	11.6	C, I, M	Dual, high speed, low noise, JFET input	5–263
TLE2074	10	40	5	10.1	1.875	0.025	98	11.6	C, I, M	Quad, high speed, low noise, JFET input	5–299
TLE2074A	10	40	3	10.1	1.875	0.025	98	11.6	C, I, M	Quad, high speed, low noise, JFET input	5–299
TLE2081	10	40	6	3.2	2.2	0.02	98	11.6	C, I, M	Single, high speed, JFET input	5–335
TLE2081A	10	40	3	3.2	2.2	0.02	98	11.6	C, I, M	Single, high speed, JFET input	5–335
TLE2082	10	40	7	2.4	1.8	0.02	98	11.8	C, I, M	Dual, JFET input	5–367
TLE2082A	10	40	4	2.4	1.8	0.2	98	11.8	C, I, M	Dual, JFET input	5–367
TLE2084	10	40	7	10.1	1.875	0.025	98	11.6	C, I, M	Quad, JFET input, high speed	5–403
TLE2084A	10	40	4	10.1	1.875	0.025	98	11.6	C, I, M	Quad, JFET input, high speed	5–403
TLE2161	6.4	10	3	6	0.35	0.004	90	40	C, I, M	Single, decompensated, micropower, high output drive	5–519
TLE2161A	6.4	10	1.5	6	0.35	0.004	90	40	C, I, M	Single, decompensated, micropower, high output drive	5–519
TLE2161B	6.4	10	0.5	6	0.35	0.004	90	40	C, I, M	Single, decompensated, precision, high output drive	5–519

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

LOW-POWER OPERATIONAL AMPLIFIERS
I_{CC}max ≤ 500 μA/Channel

DEVICE	I_{CC} μA (max)	V_{IO} mV (max)	α_{VIO} μV/°C (typ)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC251 (low bias)	17	10	1.1	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251A (low bias)	17	5	1.1	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251B (low bias)	17	2	1.1	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC25L2	17	10	1.1	0.0006	94	68	0.03	0.085	C	Single, low voltage	2–429
TLC25L2A	17	5	1.1	0.0006	94	68	0.03	0.085	C	Dual, low voltage	2–429
TLC25L2B	17	2	1.1	0.0006	94	68	0.03	0.085	C	Dual, low voltage, low offset	2–429
TLC25L4	17	10	1.1	0.0006	94	70	0.03	0.085	C	Quad, low voltage	2–449
TLC25L4A	17	5	1.1	0.0006	94	70	0.03	0.085	C	Quad, low voltage	2–449
TLC25L4B	17	2	1.1	0.0006	94	70	0.03	0.085	C	Quad, low voltage, low offset	2–449
TLC271 (low bias)	17	10	1.1	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–469
TLC271A (low bias)	17	10	1.1	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–469
TLC271B (low bias)	17	2	1.1	0.0006	94	68	0.03	0.085	C	Single, low voltage, low offset, programmable power	2–469
TLC27L7	17	0.5	1.1	0.0006	94	68	0.03	0.085	C, I, M	Dual, precision, single supply	2–625
TLC27L9	17	0.9	1.1	0.0006	94	70	0.03	0.085	C, I, M	Quad, precision, single supply	2–657
TLC1078	17	0.45	1.1	0.0006	94	68	0.032	0.085	C, I, M	Dual, precision, low voltage	2–763
TLC1079	17	0.85	1.1	0.0006	94	68	0.032	0.085	C, I, M	Quad, precision, low voltage	2–779
TLV2322	17	9	1.1	0.0006	94	68	0.03	0.085	I	Dual, low voltage	5–755
TLV2324	17	10	1.1	0.0006	94	68	0.03	0.085	I	Dual, low voltage	5–779
TLV2341 (low bias)	17	8	1.1	0.0006	94	68	0.03	0.085	I	Single, low voltage, programmable power	5–851
TL022	250	5	—	100	72	50	0.5	—	C,M	Dual, low power	2–111
TL061	250	15	10	0.03	86	42	3.5	—	C, I, M	Single, low power, JFET input, BiFET	2–291
TL061A	250	6	10	0.03	86	42	3.5	—	C	Single, low power, JFET input, BiFET	2–291
TL061B	250	3	10	0.03	86	42	3.5	—	C	Single, low power, JFET input, BiFET	2–291
TL062	250	15	10	0.03	86	42	3.5	—	C, I, M	Dual, low power, JFET input, BiFET	2–291
TL062A	250	6	10	0.03	86	42	3.5	—	C	Dual, low power, JFET input, BiFET	2–291
TL062B	250	3	10	0.03	86	42	3.5	—	C	Dual, low power, JFET input, BiFET	2–291
TL064	250	15	10	0.03	86	42	3.5	—	C, I, M	Quad, low power, JFET input, BiFET	2–291
TL064A	250	6	10	0.03	86	42	3.5	—	C	Quad, low power, JFET input, BiFET	2–291
TL064B	250	3	10	0.03	86	42	3.5	—	C	Quad, low power, JFET input, BiFET	2–291
TL064B	250	3	10	0.03	86	42	3.5	—	C	Quad, low power, JFET input, BiFET	2–291

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

TEXAS INSTRUMENTS
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LOW-POWER OPERATIONAL AMPLIFIERS (Continued)
I_{CC}max ≤ 500 μA/Channel

DEVICE	I_{CC} μA (max)	V_{IO} mV (max)	α_{VIO} μV/°C (typ)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TL064x2	250	7	10	0.03	86	42	3.5	—	C, I, M	Octal, low power, JFET input, BiFET	2–311
TLC2262	250	2.5	2	0.001	85	12	0.55	0.82	C, I	Dual, low noise, low voltage	2–855
TLC2262A	250	0.95	2	0.001	85	12	0.55	0.82	C, I	Dual, precision, low noise, low voltage	2–855
TLC2264	250	2.5	2	0.001	85	12	0.55	0.82	C, I	Quad, low noise, low voltage	2–889
TLC2264A	250	0.95	2	0.001	85	12	0.55	0.82	C, I	Quad, precision, low noise, low voltage	2–889
TLV2262	250	2.5	2	0.001	85	12	0.55	0.82	C, I	Dual, precision, low noise, low voltage	5–695
TLV2262A	250	0.95	2	0.001	85	12	0.55	0.82	C, I	Dual, low noise, low voltage	5–695
TLV2264	250	2.5	2	0.001	85	12	0.55	0.82	C, I	Quad, precision, low noise, low voltage	5–725
TLV2264A	250	0.95	2	0.001	85	12	0.55	0.82	C, I	Quad, low noise, low voltage	5–725
TL031	280	1.5	5.9	0.2	94	41	5.1	1.1	C, I, M	Single, JFET input, low power, precision	2–115
TL031A	280	0.8	5.9	0.2	94	41	5.1	1.1	C, I, M	Single, JFET input, low power, precision	2–115
TL032	280	1.5	10.8	0.2	94	41	5.1	1.1	C, I, M	Dual, JFET input, low power, precision	2–143
TL032A	280	0.8	10.8	0.2	94	41	5.1	1.1	C, I, M	Dual, JFET input, low power, precision	2–143
TL034	280	4	12	0.2	94	43	5.1	1.1	C, I, M	Quad, JFET input, low power, precision	2–171
TL034A	280	1.5	12	0.2	94	43	5.1	1.1	C, I, M	Quad, JFET input, low voltage, micropower	2–171
TLC251 (medium bias)	280	10	1.7	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251A (medium bias)	280	5	1.7	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251B (medium bias)	280	2	1.7	0.0006	91	32	0.43	0.525	C	Single, low offset, programmable power	2–411
TLC25M2	280	10	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage	2–429
TLC25M2A	280	5	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset	2–429
TLC25M2B	280	2	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset	2–429
TLC25M4	280	10	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, micropower	2–449
TLC25M4A	280	5	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, micropower	2–449
TLC25M4B	280	2	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset, micropower	2–449
TLC271 (medium bias)	280	10	1.7	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–469
TLC271A (medium bias)	280	5	1.7	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–469
TLC271B (medium bias)	280	2	1.7	0.0006	91	32	0.43	0.525	C	Single, low offset, programmable power	2–469
TLC27M2	280	10	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low power	2–693
TLC27M2A	280	5	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset, low power	2–693
TLC27M2B	280	2	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset, low power	2–693

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

LOW-POWER OPERATIONAL AMPLIFIERS (Continued)
I_{CC}max ≤ 500 μA/Channel

DEVICE	I_{CC} μA (max)	V_{IO} mV (max)	α_{VIO} μV/°C (typ)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC27M4	280	10	1.7	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low power	2–727
TLC27M4A	280	5	1.7	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low power	2–727
TLC27M4B	280	2	1.7	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low power	2–727
TL031	280	1.5	5.9	0.2	94	41	5.1	1.1	C	Single, low voltage, programmable power	2–115
TL031A	280	0.8	5.9	0.2	94	41	5.1	1.1	C	Single, low voltage, programmable power	2–115
TL032	280	1.5	10.8	0.2	94	41	5.1	1.1	C	Single, low offset, programmable power	2–143
TL032A	280	0.8	10.8	0.2	94	41	5.1	1.1	C	Single, low offset, programmable power	2–143
TLC27M7	280	0.5	1.7	0.0006	91	32	0.43	0.525	C, I, M	Dual, precision, single supply, low power	2–693
TLC27M9	280	0.9	1.7	0.0006	91	32	0.43	0.525	C, I, M	Quad, precision, single supply, low power	2–727
TLV2332	280	9	1.7	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset, low power	5–803
TLV2334	280	10	1.7	0.0006	91	32	0.43	0.525	C	Quad, low voltage	5–827
TLV2341 (medium bias)	280	8	1.7	0.0006	91	32	0.43	0.525	C	Quad, low voltage	5–851
TLE2021A	300	0.2	2	25	115	15	0.65	2	C	Quad, low voltage, micropower	5–3
TLE2062	345	4	6	0.004	90	40	3.4	2	C	Quad, low voltage, low offset, micropower	5–167
TLE2062A	345	2	6	0.004	90	40	3.4	2	C	Quad, low voltage, low power	5–167
TLE2022	350	0.5	2	25	100	15	0.65	2.8	C	Quad, low voltage, low power	5–29
TLE2022A	350	0.3	2	25	102	15	0.65	2.8	C	Quad, low voltage, low offset, micropower	5–29
TLE2022B	350	0.15	2	25	105	15	0.65	2.8	C, I, M	Dual, precision, low voltage, micropower	5–29
TLE2024	350	1	2	50	102	15	0.7	2.8	C, I, M	Quad, precision, low voltage, micropower	5–57
TLE2024A	350	0.75	2	45	105	15	0.7	2.8	I	Dual, low voltage, micropower	5–57
TLE2024B	350	0.5	2	40	108	15	0.7	2.8	I	Dual, low voltage, low power	5–57
TLE2061	350	3	6	0.004	90	40	3.4	2	I	Dual, low voltage	5–137
TLE2061A	350	1.5	6	0.004	90	40	3.4	2	I	Quad, low voltage, micropower	5–137
TLE2064	350	6	6	0.004	90	40	3.4	2	I	Quad, low voltage	5–197
TLE2064A	350	4	6	0.004	90	40	3.4	1.7	I	Single, low voltage, programmable power	5–197
TLE2161	350	3	6	0.004	90	40	10	0.525	I	Single, low voltage, programmable power	5–519
TLE2161A	350	1.5	6	0.004	90	40	10	0.085	I	Single, low voltage, programmable power	5–519
TLE2161B	350	0.5	6	0.004	90	40	10	6.4	C, I, M	Single, decompensated, high output drive	5–519
LT1013A	500	0.15	0.3	12	117	22	0.4	—	C, I, M	Dual, precision	2–51

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

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RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

DEVICE	V_{IO} mV (max)	I_{CC} mA (max)	$V_{OL} - V_{OH}$ V (typ)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/μs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC2201	0.2	1.5	0 – 4.8	0.001	110	8	2.5	1.8	C, I, M	Single, precision, low noise	2–795
TLC2201A	0.2	1.5	0 – 4.8	0.001	110	8	2.5	1.8	C, I, M	Single, precision, low noise	2–795
TLC2202	0.5	1.2	0 – 4.8	0.001	110	8	2.5	1.9	C, I, M	Dual, precision, low noise	2–825
TLC2202A	0.5	1.2	0 – 4.8	0.001	110	8	2.5	1.9	C, I, M	Dual, precision, low noise	2–825
TLC2262	2.5	0.25	0 – 4.99	0.001	80	12	0.55	0.82	C, I	Dual, low power, low noise	2–855
TLC2262A	0.95	0.25	0 – 4.99	0.001	80	12	0.55	0.82	I	Dual, precision, low power, low noise	2–855
TLC2264	2.5	0.25	0 – 4.99	0.001	80	12	0.55	0.82	C, I	Quad, low power, low noise	2–889
TLC2264A	0.95	0.25	0 – 4.99	0.001	80	12	0.55	0.82	I	Quad, precision, low power, low noise	2–889
TLC2272	2.5	1.5	0 – 4.99	0.001	75	9	3.6	2.18	C, I, M	Dual, low noise	2–923
TLC2272A	0.95	1.5	0 – 4.99	0.001	75	9	3.6	2.18	C, I, M	Dual, precision, low noise	2–923
TLC2274	2.5	1.5	0 – 4.99	0.001	75	9	3.6	2.18	C, I, M	Quad, low noise	2–957
TLC2274A	0.95	1.5	0 – 4.99	0.001	75	9	3.6	2.18	C, I, M	Quad, precision, low noise	2–957
TLV2262	2.5	0.25	0 – 4.99	0.001	80	12	0.55	0.82	C, I	Dual, low power, low voltage	5–695
TLV2262A	0.95	0.25	0 – 4.99	0.001	80	12	0.55	0.82	I	Dual, precision, low power, low noise	5–695
TLV2264	2.5	0.25	0 – 4.99	0.001	80	12	0.55	0.82	C, I	Quad, low power, low voltage	5–725
TLV2264A	0.95	0.25	0 – 4.99	0.001	80	12	0.55	0.82	I	Quad, precision, low power, low noise	5–725

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

OPERATIONAL AMPLIFIERS (Listed Alphanumerically)

DEVICE	V_{IO} mV (max)	αV_{IO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
LF347	10	18	11	0.05	100	18	13	—	C	Quad, wide bandwidth, JFET input	2–3
LF347B	5	18	11	0.05	100	18	13	—	C	Quad, wide bandwidth, JFET input	2–3
LF351	10	10	3.4	0.05	100	18	13	—	C	Dual, wide bandwidth, JFET input	2–5
LF353	10	10	6.5	0.05	100	18	13	—	C	Dual, wide bandwidth, JFET input	2–7
LF411C	2	10	3.4	0.05	100	18	13	—	C	Single, JFET input	2–9
LF412C	3	10	6.8	0.05	100	18	13	—	C	Dual, JFET input	2–11
LM118	4	—	8	120	100	—	70	—	M	Single, high performance	2–13
LM124	5	—	0.7	–20	80	—	0.13	—	M	Quad, general purpose, bipolar	2–17
LM124A	2	—	1.5	—	80	—	0.13	—	M	Quad, general purpose, bipolar	2–17
LM148	5	—	2.4	30	90	—	0.5	—	M	Quad, general purpose, bipolar	2–25
LM158	5	7	2	–20	80	—	0.2	—	M	Dual, high gain, low power, bipolar	2–29
LM158A	2	7	2	–15	80	—	0.2	—	M	Dual, high gain, low power, bipolar	2–29
LM218	4	—	8	120	100	—	70	—	I	Single, high performance	2–13
LM224	5	—	0.7	–20	80	—	0.3	—	I	Quad, general purpose, bipolar	2–17
LM224A	3	—	1.5	–15	80	—	0.3	—	I	Quad, general purpose, bipolar	2–17
LM248	6	—	—	30	90	—	0.5	—	I	Quad, general purpose, bipolar	2–25
LM258	5	7	2	–20	80	—	0.2	—	I	Dual, high gain, low power, bipolar	2–29
LM258A	3	7	2	–15	80	—	0.2	—	I	Dual, high gain, low power, bipolar	2–29
LM318	10	—	10	150	100	—	70	—	C	Single, high performance	2–13
LM324	7	—	0.7	–20	80	—	0.3	—	C	Quad, general purpose, bipolar	2–17
LM324A	3	—	1.5	–15	80	—	0.3	—	C	Quad, general purpose, bipolar	2–17
LM324x2	7	—	0.7	–20	80	—	0.3	—	C	Octal, general purpose, bipolar	2–39
LM348	6	—	—	30	90	—	0.5	—	C	Quad, general purpose, bipolar	2–25
LM358	7	7	2	–20	80	—	0.2	—	C	Dual, high gain, low power, bipolar	2–29
LM358A	3	7	2	–15	80	—	0.2	—	C	Dual, high gain, low power, bipolar	2–29
LM2900	—	—	6.2	30	—	—	0.6	—	I	Quad, Norton amplifier, bipolar	2–43
LM2902	7	—	0.7	–20	80	—	0.3	—	Q	Quad, general purpose, bipolar	2–17
LM2902Q	7	—	0.7	–20	80	—	0.3	—	Q	Quad, general purpose, bipolar	2–17
LM2904	7	7	2	–20	80	—	0.2	—	Q	Dual, high gain, low power, bipolar	2–29
LM2904Q	7	7	2	–20	80	—	0.2	—	Q	Dual, high gain, low power, bipolar	2–29

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C, Q = –40°C to 105°C

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OPERATIONAL AMPLIFIERS (Listed Alphanumerically) (Continued)

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
LM3900	—	—	6.2	30	—	—	0.6	—	C	Quad, Norton amplifier, bipolar	2–43
LT1013	0.3	0.4	0.55	15	117	22	0.4	—	C, I, M	Dual, precision	2–51
LT1013A	0.15	0.3	0.5	12	117	22	0.4	—	C, I, M	Dual, precision	2–51
LT1013D	0.8	0.7	0.55	15	114	22	0.4	—	C, I, M	Dual, precision	2–51
MC1458	6	—	5.6	80	90	45	0.5	—	C	Dual, general purpose	2–75
MC1558	5	—	5	80	90	45	0.5	—	M	Dual, general purpose	2–75
MC3303	8	10	7	–200	90	—	0.6	—	I	Quad, low power, bipolar	2–79
MC3403	10	10	7	–200	90	—	0.6	—	C	Quad, low power, bipolar	2–79
NE5532	4	—	16	200	100	5	9	—	C, I	Dual, low noise	2–85
NE5532A	4	—	16	200	100	5	9	—	C, I	Dual, low noise	2–85
NE5534	4	—	8	500	100	4	13	—	C	Single, low noise, high performance	2–89
NE5534A	4	—	8	500	100	4	13	—	C	Single, low noise, high performance	2–89
OP07C	0.15	0.5	—	1.8	120	9.8	0.3	—	C	Single, ultra-low offset voltage	2–95
OP07D	0.15	0.5	—	2	110	9.8	0.3	—	C	Single, ultra-low offset voltage	2–95
RC4136	6	—	2.8	140	90	—	1.7	—	C	Quad, high performance	2–101
RC4558	6	—	5.6	5	90	—	1.7	—	C	Dual, high performance	2–105
RM4136	4	—	2.8	140	90	—	1.7	—	M	Quad, high performance	2–101
RM4558	6	—	5.6	5	90	—	1.7	—	M	Dual, high performance	2–105
RV4146	6	—	2.8	140	90	—	1.7	—	I	Quad, high performance	2–101
RV4558	6	—	5.6	5	90	—	1.7	—	I	Dual, high performance	2–105
SE5534	2	—	6.5	400	100	3.5	13	—	M	Single, low noise, high performance	2–89
SE5534A	2	—	6.5	400	100	3.5	13	—	M	Single, low noise, high performance	2–89
TL022	5	—	0.25	100	72	50	0.5	—	C,M	Dual, low power	2–111
TL031	1.5	5.9	0.28	0.2	94	41	5.1	1.1	C, I, M	Single, JFET input, low power, precision	2–115
TL031A	0.8	5.9	0.28	0.2	94	41	5.1	1.1	C, I, M	Single, JFET input, low power, precision	2–115
TL032	1.5	10.8	0.28	0.2	94	41	5.1	1.1	C, I, M	Dual, JFET input, low power, precision	2–143
TL032A	0.8	10.8	0.28	0.2	94	41	5.1	1.1	C, I, M	Dual, JFET input, low power, precision	2–143
TL034	4	12	0.28	0.2	94	43	5.1	1.1	C, I, M	Quad, JFET input, low power, precision	2–171
TL034A	1.5	12	0.28	0.2	94	43	5.1	1.1	C, I, M	Quad, JFET input, low voltage, micropower	2–171
TL051	1.5	8	3.2	0.2	93	18	23.7	3.1	C, I, M	Single, JFET-input, high speed, precision	2–199

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

OPERATIONAL AMPLIFIERS (Listed Alphanumerically) (Continued)

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TL051A	0.8	8	3.2	0.2	93	18	23.7	3.1	C, I, M	Single, JFET input, high speed, precision	2–199
TL052	1.5	8	2.8	0.2	93	19	20.7	3	C, I, M	Dual, JFET-input, high speed, precision	2–229
TL052A	0.8	8	2.8	0.2	93	19	20.7	3	C, I, M	Dual, JFET input, high speed, precision	2–229
TL054	4	23	2.8	0.2	92	21	17.8	2.7	C, I, M	Quad, JFET-input, high speed, precision	2–261
TL054A	1.5	23	2.8	0.2	92	21	17.8	2.7	C, I, M	Quad, JFET input, high speed, precision	2–261
TL061	15	10	0.25	0.03	86	42	3.5	--	C, I, M	Single, low power, JFET input, BiFET	2–291
TL061A	6	10	0.25	0.03	86	42	3.5	—	C	Single, low power, JFET input, BiFET	2–291
TL061B	3	10	0.25	0.03	86	42	3.5	—	C	Single, low power, JFET input, BiFET	2–291
TL062	15	10	0.25	0.03	86	42	3.5	—	C, I, M	Dual, low power, JFET input, BiFET	2–291
TL062A	6	10	0.25	0.03	86	42	3.5	—	C	Dual, low power, JFET input, BiFET	2–291
TL062B	3	10	0.25	0.03	86	42	3.5	—	C	Dual, low power, JFET input, BiFET	2–291
TL064	15	10	0.25	0.03	86	42	3.5	—	C, I, M	Quad, low power, JFET input, BiFET	2–291
TL064A	6	10	0.25	0.03	86	42	3.5	—	C	Quad, low power, JFET input, BiFET	2–291
TL064B	3	10	0.25	0.03	86	42	3.5	—	C	Quad, low power, JFET input, BiFET	2–291
TL064x2	7	10	0.25	0.03	86	42	3.5	—	C	Octal, low power, JFET input, BiFET	2–311
TL070	10	18	2.5	0.065	100	18	13	—	C	Single, low noise JFET input, BiFET	2–321
TL071	10	18	2.5	0.065	100	18	13	—	C, I, M	Single, low noise JFET input, BiFET	2–335
TL071A	6	18	2.5	0.065	100	18	13	—	C	Single, low noise JFET input, BiFET	2–335
TL071B	3	18	2.5	0.065	100	18	13	—	C	Single, low noise JFET input, BiFET	2–335
TL072	10	18	2.5	0.065	100	18	13	—	C, I, M	Dual, low noise JFET input, BiFET	2–335
TL072A	6	18	2.5	0.065	100	18	13	—	C	Dual, low noise JFET input, BiFET	2–335
TL072B	3	18	2.5	0.065	100	18	13	—	C	Dual, low noise JFET input, BiFET	2–335
TL074	10	18	2.5	0.065	100	18	13	—	C, I, M	Quad, low noise JFET input, BiFET	2–335
TL074A	6	18	2.5	0.065	100	18	13	—	C	Quad, low noise JFET input, BiFET	2–335
TL074B	3	18	2.5	0.065	100	18	13	—	C	Quad, low noise JFET input, BiFET	2–335
TL074x2	10	18	2.5	0.065	100	18	13	—	C	Octal, low noise, JFET input, BiFET	2–351
TL081	15	18	2.8	0.03	86	18	13	—	C, I, M	Single, general purpose, JFET input, BiFET	2–361
TL081A	6	18	2.8	0.03	86	18	13	—	C	Single, general purpose, JFET input, BiFET	2–361
TL081B	3	18	2.8	0.03	86	18	13	—	C	Single, general purpose, JFET input, BiFET	2–361
TL082	15	18	2.8	0.03	86	18	13	—	C, I, M	Dual, general purpose, JFET input, BiFET	2–361

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

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OPERATIONAL AMPLIFIERS (Listed Alphanumerically) (Continued)

DEVICE	V_{IO} mV (max)	αV_{IO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TL082A	6	18	2.8	0.03	86	18	13	—	C	Dual, general purpose, JFET input, BiFET	2–361
TL082B	3	18	2.8	0.03	86	18	13	—	C	Dual, general purpose, JFET input, BiFET	2–361
TL084	15	18	2.8	0.03	86	18	13	—	C, I, M	Quad, general purpose, JFET input, BiFET	2–361
TL084A	6	18	2.8	0.03	86	18	13	—	C	Quad, general purpose, JFET input, BiFET	2–361
TL084B	3	18	2.8	0.03	86	18	13	—	C	Quad, general purpose, JFET input, BiFET	2–361
TL084x2	15	18	2.8	0.03	86	18	13	—	C	Octal, general purpose, JFET input, BiFET	2–381
TL2828	7	15	1	−100	75	23	0.15	0.4	Z	Dual, high temperature, bipolar	2–391
TL2829	7	15	0.3	−100	75	23	0.25	0.4	Z	Quad, high temperature, low power, bipolar	2–397
TLC251 (high bias)	10	1.8	1.6	0.0006	80	25	3.6	1.7	C	Single, low voltage, programmable power	2–411
TLC251A (high bias)	5	1.8	1.6	0.0006	80	25	3.6	1.7	C	Single, low voltage, programmable power	2–411
TLC251B (high bias)	2	1.8	1.6	0.0006	80	25	3.6	1.7	C	Single, low offset, programmable power	2–411
TLC251 (medium bias)	10	1.7	0.28	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251A (medium bias)	5	1.7	0.28	0.0006	91	32	0.43	0.525	C	Single, low voltage, programmable power	2–411
TLC251B (medium bias)	2	1.7	0.28	0.0006	91	32	0.43	0.525	C	Single, low offset, programmable power	2–411
TLC251 (low bias)	10	1.1	0.017	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251A (low bias)	5	1.1	0.017	0.0006	94	68	0.03	0.085	C	Single, low voltage, programmable power	2–411
TLC251B (low bias)	2	1.1	0.017	0.0006	94	68	0.03	0.085	C	Single, low offset, programmable power	2–411
TLC252	10	1.8	1.6	0.0006	80	25	3.6	1.7	C	Dual, low voltage	2–429
TLC252A	5	1.8	1.6	0.0006	80	25	3.6	1.7	C	Dual, low voltage	2–429
TLC252B	2	1.8	1.6	0.0006	80	25	3.6	1.7	C	Dual, low voltage, low offset	2–429
TLC25L2	10	1.1	0.017	0.0006	94	68	0.03	0.085	C	Dual, low voltage, micropower	2–429
TLC25L2A	5	1.1	0.017	0.0006	94	68	0.03	0.085	C	Dual, low voltage, micropower	2–429
TLC25L2B	2	1.1	0.017	0.0006	94	68	0.03	0.085	C	Dual, low voltage, low offset, micropower	2–429
TLC25M2	10	1.7	0.28	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low power	2–429
TLC25M2A	5	1.7	0.28	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low power	2–429
TLC25M2B	2	1.7	0.28	0.0006	91	32	0.43	0.525	C	Dual, low voltage, low offset, low power	2–429
TLC254	10	1.8	1.6	0.0006	80	25	3.6	1.7	C	Quad, low voltage	2–449
TLC254A	5	1.8	1.6	0.0006	80	25	3.6	1.7	C	Quad, low voltage	2–449
TLC254B	2	1.8	1.6	0.0006	80	25	3.6	1.7	C	Quad, low voltage, low offset	2–449
TLC25L4	10	1.1	0.017	0.0006	94	70	0.03	0.085	C	Quad, low voltage, micropower	2–449

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C, Z = −40°C to 150°C

OPERATIONAL AMPLIFIERS (Listed Alphanumerically) (Continued)

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC25L4A	5	1.1	0.017	0.0006	94	70	0.03	0.085	C	Quad, low voltage, micropower	2–449
TLC25L4B	2	1.1	0.017	0.0006	94	70	0.03	0.085	C	Quad, low voltage, low offset, micropower	2–449
TLC25M4	10	1.7	0.28	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low power	2–449
TLC25M4A	5	1.7	0.28	0.0006	91	32	0.43	0.525	C	Quad, low voltage, low power	2–449
TLC25M4B	2	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, low voltage, low offset, micropower	2–449
TLC271 (high bias)	10	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Single, programmable power	2–469
TLC271A (high bias)	5	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Single, programmable power	2–469
TLC271B (high bias)	2	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Single, low offset, programmable power	2–469
TLC271 (medium bias)	10	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Single, programmable power	2–469
TLC271A (medium bias)	5	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Single, programmable power	2–469
TLC271B (medium bias)	2	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Single, low offset, programmable power	2–469
TLC271 (low bias)	10	1.1	0.017	0.0006	94	68	0.03	0.085	C, I, M	Single, programmable power	2–469
TLC271A (low bias)	5	1.1	0.017	0.0006	94	68	0.03	0.085	C, I, M	Single, programmable power	2–469
TLC271B (low bias)	2	1.1	0.017	0.0006	94	68	0.03	0.085	C, I, M	Single, low offset, programmable power	2–469
TLC272	10	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, single supply	2–537
TLC272A	5	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, single supply	2–537
TLC272B	2	1.8	1.6	0.0006	80	25	3.6	1.7	C	Dual, low offset, single supply	2–537
TLC27L2	10	1.1	0.017	0.0006	94	68	0.03	0.085	C	Dual, micropower, single supply	2–625
TLC27L2A	5	1.1	0.017	0.0006	94	68	0.03	0.085	C	Dual, micropower, single supply	2–625
TLC27L2B	2	1.1	0.017	0.0006	94	68	0.03	0.085	C	Dual, low offset, micropower, single supply	2–625
TLC27M2	10	1.7	0.28	0.0006	91	32	0.43	0.525	C	Dual, low power, single supply	2–693
TLC27M2A	5	1.7	0.28	0.0006	91	32	0.43	0.525	C	Dual, low offset, low power, single supply	2–693
TLC27M2B	2	1.7	0.28	0.0006	91	32	0.43	0.525	C	Dual, low offset, low power, single supply	2–693
TLC274	10	1.8	1.6	0.0006	80	25	3.6	1.7	C	Quad, single supply	2–573
TLC274A	5	1.8	1.6	0.0006	80	25	3.6	1.7	C	Quad, single supply	2–573
TLC274B	2	1.8	1.6	0.0006	80	25	3.6	1.7	C	Quad, low offset, single supply	2–573
TLC274x2	10	1.8	1.6	0.0006	80	25	3.6	1.7	C	Octal, single supply	2–609
TLC27L4	10	1.1	0.017	0.0006	94	70	0.03	0.085	C	Quad, micropower, single supply	2–657
TLC27L4A	5	1.1	0.017	0.0006	94	70	0.03	0.085	C	Quad, micropower, single supply	2–657
TLC27L4B	2	1.1	0.017	0.0006	94	70	0.03	0.085	C	Quad, low offset, micropower, single supply	2–657

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

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OPERATIONAL AMPLIFIERS (Listed Alphanumerically) (Continued)

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC27M4	10	1.7	0.28	0.0006	91	32	0.43	0.525	C	Quad, low power, single supply	2–727
TLC27M4A	5	1.7	0.28	0.0006	91	32	0.43	0.525	C	Quad, low power, single supply	2–727
TLC27M4B	2	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, low offset, micropower, single supply	2–727
TLC277	0.5	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Dual, precision, single supply, low power	2–537
TLC279	0.9	1.8	1.6	0.0006	80	25	3.6	1.7	C, I, M	Quad, precision, single supply, low power	2–573
TLC27L7	0.5	1.1	0.017	0.0006	94	68	0.03	0.085	C, I, M	Dual, precision, single supply, micropower	2–625
TLC27L9	0.9	1.1	0.017	0.0006	94	70	0.03	0.085	C, I, M	Quad, precision, single supply, micropower	2–657
TLC27M7	0.5	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Dual, precision, single supply, low power	2–693
TLC27M9	0.9	1.7	0.28	0.0006	91	32	0.43	0.525	C, I, M	Quad, precision, single supply, low power	2–727
TLC1078	0.45	1.1	0.017	0.0006	95	68	0.032	0.085	C, I, M	Dual, precision, low voltage, micropower	2–763
TLC1079	0.85	1.1	0.017	0.0006	95	68	0.032	0.085	C, I, M	Quad, precision, low voltage, micropower	2–779
TLC2201	0.5	0.5	1.5	0.001	110	8	2.5	1.8	C, I, M	Single, precision, low noise, rail-to-rail output	2–795
TLC2201A	0.2	0.5	1.5	0.001	110	8	2.5	1.8	C, I, M	Single, precision, low noise, rail-to-rail output	2–795
TLC2202	1	0.5	1.2	0.001	110	8	2.5	1.9	C, I, M	Dual, precision, low noise, rail-to-rail output	2–825
TLC2202A	0.5	0.5	1.2	0.001	110	8	2.5	1.9	C, I, M	Dual, precision, low noise, rail-to-rail output	2–825
TLC2262	2.5	2	0.25	0.001	80	12	0.55	0.82	C, I	Dual, low power, rail-to-rail output, low noise	2–855
TLC2262A	0.95	2	0.25	0.001	80	12	0.55	0.82	C, I	Dual, precision, low power, rail-to-rail output	2–855
TLC2264	2.5	2	0.25	0.001	80	12	0.55	0.82	C, I	Quad, low power, rail-to-rail output, low noise	2–889
TLC2264A	0.95	2	0.25	0.001	80	12	0.55	0.82	I	Quad, low power, rail-to-rail output, low noise	2–889
TLC2272	2.5	2	3	0.001	75	9	3.6	2.18	C, I, M	Dual, rail-to-rail output	2–923
TLC2272A	0.95	2	3	0.001	75	9	3.6	2.18	C, I, M	Dual, rail-to-rail output, precision	2–923
TLC2274	2.5	2	3	0.001	75	9	3.6	2.18	C, I, M	Quad, rail-to-rail output	2–957
TLC2274A	0.95	2	3	0.001	75	9	3.6	2.18	C, I, M	Quad, rail-to-rail output, precision	2–957
TLC2652	0.003	0.03	2.4	0.004	140	23	2.8	1.9	C, I, M	Single, precision, chopper stabilized	2–993
TLC2652A	0.001	0.03	2.4	0.004	140	23	2.8	1.9	C, I, M	Single, precision, chopper stabilized	2–993
TLC2654	0.02	0.3	2.4	0.05	125	13	2	1.9	C, I, M	Single, precision, chopper stabilized	2–1017
TLC2654A	0.01	0.3	2.4	0.05	125	13	2	1.9	C, I, M	Single, precision, chopper stabilized	2–1017
TLC2801	0.5	0.5	1.5	0.001	110	8	2.5	2.18	Z	Single, precision, low noise, rail-to-rail output	2–1041
TLC2810	10	3.5	1.6	0.007	90	25	3.6	1.7	Z	Dual, high temperature, CMOS	2–1051
TLC2872	2.5	2	3	0.001	75	9	3.6	2	Z	Dual, low noise, high temperature	2–1073

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C, Z = −40°C to 150°C

OPERATIONAL AMPLIFIERS (Listed Alphanumerically) (Continued)

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLE2021	0.5	2	0.3	25	115	15	0.65	2	C, I, M	Single, precision, low power, high speed	5–3
TLE2021A	0.2	2	0.3	25	115	15	0.65	2.8	C, I, M	Single, precision, low power, high speed	5–3
TLE2022	0.5	2	0.35	25	100	15	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2022A	0.3	2	0.35	25	102	15	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2022B	0.15	2	0.35	25	105	15	0.65	2.8	C, I, M	Dual, precision, low power, high speed	5–29
TLE2024	1	2	0.35	50	102	15	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2024A	0.75	2	0.35	45	105	15	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2024B	0.5	2	0.35	40	108	15	0.7	2.8	C, I, M	Quad, precision, low power, high speed	5–57
TLE2027	0.1	0.4	5.3	15	131	3.3	2.8	13	C, I, M	Single, low noise, high speed, precision	5–83
TLE2027A	0.025	0.2	4.7	15	131	3.3	2.8	13	C, I, M	Single, low noise, high speed, precision	5–83
TLE2037	0.1	0.4	5.3	15	131	3.3	2.8	76	C, I, M	Single, low noise, high speed, precision, decompensated	5–109
TLE2037A	0.025	0.2	4.7	15	131	3.3	2.8	76	C, I, M	Single, low noise, high speed, precision, decompensated	5–109
TLE2061	3	6	0.35	0.004	90	40	3.4	2	C, I, M	Single, JFET input, micropower, high output drive	5–137
TLE2061A	1.5	6	0.35	0.004	90	40	3.4	2	C, I, M	Single, JFET input, micropower, high output drive	5–137
TLE2062	4	6	0.345	0.004	90	40	3.4	2	C, I, M	Dual, JFET input, micropower, high output drive	5–167
TLE2062A	2	6	0.345	0.004	90	40	3.4	2	C, I, M	Dual, JFET input, micropower, high output drive	5–167
TLE2064	6	6	0.35	0.004	90	40	3.4	2	C, I, M	Quad, JFET input, micropower, high output drive	5–197
TLE2064A	4	6	0.35	0.004	90	40	3.4	2	C, I, M	Quad, JFET input, micropower, high output drive	5–197
TLE2071	4	3.2	2.2	0.02	98	11.6	40	10	C, I, M	Single, high speed, low noise, JFET input	5–227
TLE2071A	2	3.2	2.2	0.02	98	11.6	40	10	C, I, M	Single, high speed, low noise, JFET input	5–227
TLE2072	6	2.4	1.8	0.02	98	11.6	40	10	C, I, M	Dual, high speed, low noise, JFET input	5–263
TLE2072A	3.5	2.4	1.8	0.02	98	11.6	40	10	C, I, M	Dual, high speed, low noise, JFET input	5–263
TLE2074	5	10.1	1.875	0.025	98	11.6	40	10	C, I, M	Quad, high speed, low noise, JFET input	5–299
TLE2074A	3	10.1	1.875	0.025	98	11.6	40	10	C, I, M	Quad, high speed, low noise, JFET input	5–299
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TLE2081A	3	3.2	2.2	0.02	98	11.6	40	10	C, I, M	Single, high speed, JFET input	5–335
TLE2082	7	2.4	1.8	0.02	98	11.8	40	10	C, I, M	Dual, JFET input, high speed	5–367
TLE2082A	4	2.4	1.8	0.02	98	11.8	40	10	C, I, M	Dual, JFET input, high speed	5–367
TLE2084	7	10.1	1.875	0.025	98	11.6	40	10	C, I, M	Quad, JFET input, high speed	5–403
TLE2084A	4	10.1	1.875	0.025	98	11.6	40	10	C, I, M	Quad, JFET input, high speed	5–403

† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

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OPERATIONAL AMPLIFIERS (Listed Alphanumerically) (Continued)

DEVICE	V_{IO} mV (max)	α_{VIO} µV/°C (typ)	I_{CC} mA (max)	I_{IB} nA (typ)	CMRR dB (typ)	V_n (1 kHz) nV/√Hz (typ)	SR V/µs (typ)	GBW MHz (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLE2141	0.9	1.7	4.5	−700	108	10.5	45	6	C, I, M	Single, precision, high speed, high output drive	5–435
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TLE2142	1.2	1.7	4.5	−700	108	10.5	45	6	C, I, M	Dual, precision, high speed, high output drive, low noise	5–463
TLE2142A	0.75	1.7	4.5	−700	108	10.5	45	6	C, I, M	Dual, precision, high speed, high output drive, low noise	5–463
TLE2144	2.4	1.7	4.5	−700	108	10.5	45	6	C, I, M	Quad, precision, high speed, high output drive, low noise	5–491
TLE2144A	1.5	1.7	4.5	−700	108	10.5	45	6	C, I, M	Quad, precision, high speed, high output drive, low noise	5–491
TLE2161	3	6	0.35	0.004	90	40	10	6.4	C, I, M	Single, decompensated, micropower, high output drive	5–519
TLE2161A	1.5	6	0.35	0.004	90	40	10	6.4	C, I, M	Single, decompensated, micropower, high output drive	5–519
TLE2227	0.35	0.4	5.3	15	115	2.5	2.5	13	C	Dual, precision, low noise, high speed	5–547
TLE2237	0.35	0.4	5.3	15	115	2.5	5	50	C	Dual, precision, low noise, decompensated	5–569
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TLE2682	7.5	2.4	3.6	15	89	—	35	—	I	Single with switched-capacitor voltage converter	5–647
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TLV2324	10	1.1	0.017	0.0006	94	68	0.03	0.085	I	Quad, low voltage, micropower	5–779
TLV2332	9	1.7	0.28	0.0006	91	32	0.43	0.525	I	Dual, low voltage, low power	5–803
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TLV2341 (high bias)	8	2.7	1.6	0.0006	80	25	3.6	1.7	I	Single, low voltage, programmable power	5–851
TLV2341 (medium bias)	8	1.7	0.28	0.0006	91	32	0.43	0.525	I	Single, low voltage, programmable power	5–851
TLV2341 (low bias)	8	1.1	0.017	0.0006	94	68	0.03	0.085	I	Single, low voltage, programmable power	5–851
TLV2342	9	2.7	1.6	0.0006	80	25	3.6	1.7	I	Dual, low voltage	5–901
TLV2344	10	2.7	1.6	0.0006	80	25	3.6	1.7	I	Quad, low voltage	5–925
TLV2262	2.5	2	0.25	0.001	80	12	0.55	0.82	I	Dual, precision, low voltage, low power, rail to rail	5–695
TLV2262A	2.5	2	0.25	0.001	80	12	0.55	0.82	I	Dual, precision, low voltage, low power, rail to rail	5–695
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† C = 0°C to 70°C, I = −40°C to 85°C, M = −55°C to 125°C

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

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α_{IIO} Average Temperature Coefficient of Input Offset Current

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \frac{\left(I_{IO} \text{ at } T_{A(1)}\right) - \left(I_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

α_{VIO} Average Temperature Coeffiicient of Input Offset Voltage

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range. The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

$$\alpha_{VIO} = \frac{\left(V_{IO} \text{ at } T_{A(1)}\right) - \left(V_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

ΔV_{CC}

See k_{SVS}

ΔV_{IO}

See k_{SVS}

ϕ_m Phase Margin

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

A_m Gain Margin

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

A_V Large-Signal Voltage Amplification

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output

A_{VD} Differential Voltage Amplification

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant

B_1 Unity-Gain Bandwidth

The range of frequencies within which the maximum output voltage swing is above a specified value.

B_{OM} Maximum-Output-Swing Bandwidth

The range of frequencies within which the maximum output voltage swing is above the specified value.

c_i Input Capacitance

The capacitance between the input terminals with either input grounded

CMRR, k_{CMR}
Common-Mode Rejection Ratio

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

$\overline{F}$ **Average Noise Figure**

The ratio of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

I_{CC+}, I_{CC-}
Supply Current

The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit

I_{IB} **Input Bias Current**

The average of the currents into the two input terminals with the output at the specified level

I_{IO} **Input Offset Current**

The difference between the currents into the two input terminals with the output at the specified level

I_n **Equivalent Input Noise Current**

The current of an ideal current source (having internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

I_{OL} **Low-Level Output Current**

The current into an output with input conditions applied that according to the product specification will establish a low level at the output.

I_{OS} **Short-Circuit Output Current**

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point

k_{CMR}

See CMRR

k_{SVS}, ΔV_{CC}, ΔV_{IO}
Supply Voltage Sensitivity

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

k_{SVR} **Supply Voltage Rejection Ratio**

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

P_D Total Power Dissipation

The total dc power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$

r_i Input Resistance

The resistance between the input terminals and either input grounded

r_{id} Differential Input Resistance

The small-signal resistance between two ungrounded input terminals

r_o Output Resistance

The resistance between an output terminal and ground

SR Slew Rate

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input

t_r Rise Time

The time required for an output voltage step to change from 10% to 90% of its final value

t_{tot} Total Response Time

The time between a step-function change of the input signal and the instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm\varepsilon$) containing the final output signal level.

V_I Input Voltage Range

The range of voltage that if exceeded at either input terminal may cause the operational amplifier to cease functioning properly.

V_{IO} Input Offset Voltage

The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

V_{IC} Common-Mode Input Voltage

The average of the two input voltages

V_{ICR} Common-Mode Input Voltage Range

The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

V_n Equivalent Input Noise Voltage

The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

V_{O1}/V_{O2} Crosstalk Attenuation

The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel

V_{OH} High-Level Output Voltage

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-Level Output Voltage

The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

V_{ID} Differential Input Voltage

The voltage at the noninverting input with respect to the inverting input

V_{OM} Maximum Peak Output Voltage Swing

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

$V_{O(PP)}$ Maximum Peak-to-Peak Output Voltage Swing

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

z_{ic} Common-Mode Input Impedance

The parallel sum of the small-signal impedance between each input terminal and ground

z_o Output Impedance

The small-signal impedance between the output terminal and ground

Overshoot Factor

The ratio of the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal to the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

COMPARATORS (Listed Alphanumerically)

DEVICE	V_{CC+} V (nom)	V_{CC-} V (nom)	V_{IO} mV (max)	I_{IB} µA (max)	I_{OL} mA (min)	RESPONSE TIME ns (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
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LM239A	4 – 30	0	2	–0.25	6	300	I	Quad, low offset, low power, bipolar	6–19
LM293	4 – 30	0	5	0.25	6	300	I	Dual, precision input	6–27
LM293A	4 – 30	0	2	0.25	6	300	I	Dual, low offset, precision input, bipolar	6–27
LM306	12	–6	5	40	100	28	C	Single, strobe	6–33
LM311	4 – 30	0	7.5	0.25	8	115	C	Single, strobe	6–3
LM339	4 – 30	0	5	–0.25	6	300	C	Quad, low power, bipolar	6–19
LM339A	4 – 30	0	2	–0.25	6	300	C	Quad, precision input	6–19
LM339x2	4 – 30	0	2	–0.25	6	300	C	Octal, precision input	6–41
LM393	4 – 30	0	5	0.25	6	300	C	Dual, low power	6–27
LM393A	4 – 30	0	2	0.25	6	300	C	Dual, precision input	6–27
LM2901	4 – 30	0	7	–0.25	6	300	I	Quad, low power, bipolar	6–19
LM2901Q	4 – 30	0	7	–0.25	6	300	I	Quad, low power, bipolar	6–19
LM2903	4 – 30	0	7	0.25	6	300	I	Dual, low power	6–27
LM2903Q	4 – 30	0	7	0.25	6	300	I	Dual, low power	6–27
LM3302	4 – 26	0	20	0.5	6	300	I	Quad, low power, bipolar	6–45
LP111	4 – 30	0	7.5	0.1	1.6	1200	M	Single, low power, strobe	6–49
LP211	4 – 30	0	7.5	0.1	1.6	1200	I	Single, low power, strobe	6–49
LP239	4 – 30	0	±5	–0.025	20	8000	I	Quad, ultra-low power, bipolar	6–53
LP311	4 – 30	0	7.5	0.1	1.6	1200	C	Single, low power, strobe	6–49
LP339	4 – 30	0	±5	–0.025	6	8000	C	Quad, ultra-low power, bipolar	6–53
TL712	5	0	±1	—	max 16	25	C	Single, output enable	6–65
TL714C	5	0	—	—	max 16	7	C	Single, high speed	6–69
TLC139	4 – 16	0	5	typ 5 pA	—	2500	M	Quad, low power	6–73
TLC339	4 – 16	0	5	typ 5 pA	6	1100	C, I, M	Quad, ultra-low power, open-drain output	6–73

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

COMPARATORS (Listed Alphanumerically) (Continued)

DEVICE	V_{CC+} V (nom)	V_{CC-} V (nom)	V_{IO} mV (max)	I_{IB} µA (max)	I_{OL} mA (min)	RESPONSE TIME ns (typ)	TEMP† RANGE	DESCRIPTION	PAGE NO.
TLC352	1.4 – 18	0	10	typ 5 pA	6	200	C, I, M	Dual, ultra-low supply	6–89
TLC354	1.4 – 18	0	10	typ 5 pA	6	200	C, I, M	Quad, low supply	6–97
TLC371	3 – 16	0	3	typ 5 pA	6	200	C, I, M	Single, high speed	6–107
TLC372	3 – 16	0	5	typ 5 pA	6	200	C, I, M	Dual, high speed	6–117
TLC374	3 – 18	0	10	typ 5 pA	6	200	C, I, M	Quad, high speed, CMOS	6–128
TLC393	3 – 18	0	5	typ 5 pA	6	1100	C, I, M	Dual, ultra-low power, open-drain output	6–141
TLC3702	3 – 18	0	5	typ 5 pA	4	1300	C, I, M	Dual, ultra-low power, push-pull output	6–157
TLC3704	3 – 18	0	5	typ 5 pA	4	1300	C, I, M	Quad, ultra-low power, push-pull output	6–179
TLV1393	2 – 7	0	5	–0.25	0.5	700	I	Dual, low voltage	6–203
TLV2352	2 – 8	0	5	typ 5 pA	6	200	I	Dual, low voltage	6–217
TLV2354	2 – 8	0	5	typ 5 pA	6	200	I	Quad, low voltage	6–229
TLV2393	2 – 7	0	5	–0.25	4	450	I	Dual, low voltage	6–203

† C = 0°C to 70°C, I = –40°C to 85°C, M = –55°C to 125°C

TEXAS INSTRUMENTS
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Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and the buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

Manufacturers are arranged in alphabetical order.

LINEAR TECHNOLOGY			
PART NO.	**DIRECT TI REPLACEMENT**	**SUGGESTED TI REPLACEMENT**	**PAGE NO.**
LT1017		TLC352	6–89
		TLC3702	6–157
LT1018		TLC352	6–89
		TLC3702	6–157
NATIONAL			
LM311	LM311		6–3
LM339	LM339		6–19
		TLC339	6–73
LM393	LM393		6–27
		TLC393	6–141
LM2901	LM2901		6–19
		TLC339	6–73
LM3302	LM3302		6–45
LP339	LP339		6–53
		TLC339	6–73
PMI			
CMP04F		LM339	6–19
		LM2901	6–19
		LM3302	6–45
		TLC339	6–73

α_{IIO} Average Temperature Coefficient of Input Offset Current

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \frac{\left(I_{IO} \text{ at } T_{A(1)}\right) - \left(I_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

α_{VIO} Average Temperature Coefficient of Input Offset Voltage

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \frac{\left(V_{IO} \text{ at } T_{A(1)}\right) - \left(V_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

A_{VD} Differential Voltage Amplification

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant

CMRR

See k_{CMR}

I_{CC+}, I_{CC-} Supply Current

The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit

$I_{IH(S)}$ High-Level Strobe Current

The current flowing into or out of† the strobe at a high-level voltage

I_{IB} Input Bias Current

The average of the currents into the two input terminals with the output at the specified level

$I_{IL(S)}$ Low-Level Strobe Current

The current flowing out of† the strobe at a low-level voltage

I_{IO} Input Offset Current

The difference between the currents into the two input terminals with the output at the specified level

I_{OH} High-Level Output Current

The current into an output with input conditions applied that according to the product specification will establish a high level at the output.

I_{OL} Low-Level Output Current

The current into an output with input conditions applied that according to the product specification will establish a low level at the output.

k_{CMR} or CMRR Common-Mode Rejection Ratio

The ratio of differential voltage amplification to common-mode voltage amplification.

NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

† Current out of a terminal is given as a negative value.

P_D Total Power Dissipation

The total dc power supplied to the device less any power delivered from the device to a load.

NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$.

r_o Output Resistance

The resistance between an output terminal and ground

V_{IC} Common-Mode Input Voltage

The average of the two input voltages

V_{ICR} Common-Mode Input Voltage Range

The range of common-mode input voltage that if exceeded may cause the comparator to cease functioning properly.

V_{ID} Differential Input Voltage

The voltage at the noninverting input with respect to the inverting input

V_{ID} Differential Input Voltage Range

The range of voltage between the two input terminals that if exceeded may cause the comparator to cease functioning properly.

V_I Input Voltage Range

The range of voltage that if exceeded at either input terminal may cause the comparator to cease functioning properly.

$V_{IH(S)}$ High-Level Strobe Voltage

For a device having an active-low strobe, a voltage within that range is guaranteed not to interfere with the operation of the comparator.

$V_{IL(S)}$ Low-Level Strobe Voltage

For a device having an active-low strobe, a voltage within the range that is guaranteed to force the output high or low, as specified, independently of the differential inputs.

V_{IO} Input Offset Voltage

The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to the specified level.

V_{OH} High-Level Output Voltage

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-Level Output Voltage

The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

Response Time

The interval between the application of an input step function and the instant the output crosses the logic threshold voltage.

NOTE: The input step drives the comparator from some initial condition sufficient to saturate the output (or in the case of high-to-low-level response time, to turn the output off) to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time

The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from its active logic level to its inactive logic level.

General Information (Volume A) 1
Operational Amplifiers 2
Mechanical Data (Volume A) 3
General Information (Volume B) 4
Operational Amplifiers (continued) 5
Comparators 6
Mechanical Data (Volume B) 7

- **Supply Current . . . 230 μA Max**
- **High Unity-Gain Bandwidth . . . 2 MHz Typ**
- **High Slew Rate . . . 0.45 V/μs Min**
- **Supply-Current Change Over Military Temp Range . . . 10 μA Typ at $V_{CC\pm}$ = ± 15 V**
- **Specified for Both 5-V Single-Supply and ±15-V Operation**
- **Phase-Reversal Protection**
- **High Open-Loop Gain . . . 6.5 V/μV (136 dB) Typ**
- **Low Offset Voltage . . . 100 μV Max**
- **Offset Voltage Drift With Time 0.005 μV/mo Typ**
- **Low Input Bias Current . . . 50 nA Max**
- **Low Noise Voltage . . . 19 nV/√Hz Typ**

description

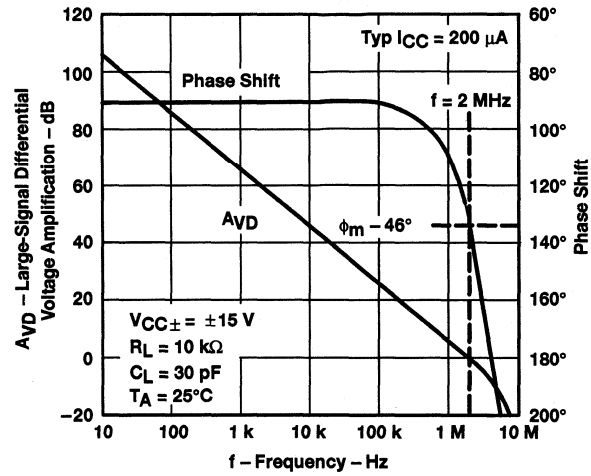
The TLE2021, TLE2021A, and TLE2021B devices are precision, high-speed, low-power operational amplifiers using a new Texas Instruments Excalibur process. These devices combine the best features of the OP21 with highly improved slew rate and unity-gain bandwidth.

The complementary bipolar Excalibur process utilizes isolated vertical pnp transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a precision device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VS FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	200 μV 500 μV	TLE2021ACD TLE2021CD	— TLE2021CDBLE	—	—	TLE2021ACP TLE2021CP	— TLE2021CPWLE	TLE2021Y
–40°C to 85°C	200 μV 500 μV	TLE2021AID TLE2021ID	—	—	—	TLE2021AIP TLE2021IP	—	—
–55°C to 125°C	100 μV 200 μV 500 μV	— TLE2021AMD TLE2021MD	—	TLE2021BMFK TLE2021AMFK TLE2021MFK	TLE2021BMJG TLE2021AMJG TLE2021MJG	— TLE2021AMP TLE2021MP	—	—

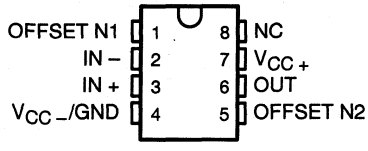
The D packages are available taped and reeled. Add the suffix R (e.g., TLE2021CDR). The DB and PW packages are only available left-end taped and reeled. Chips are tested at 25°C.

description (continued)

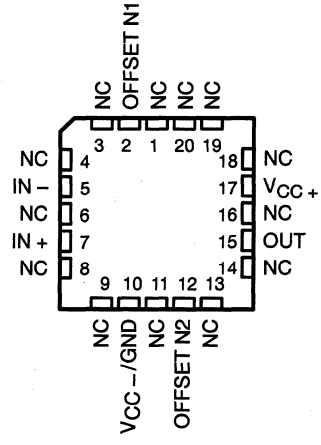
A variety of available options includes small-outline and chip-carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

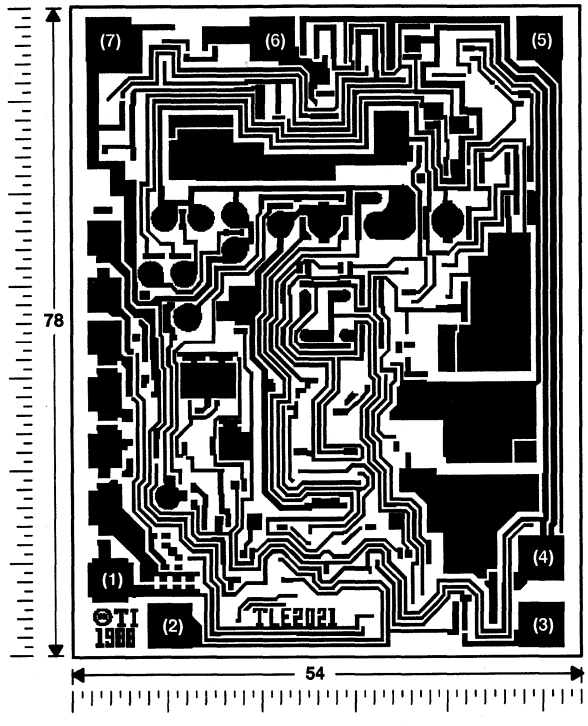


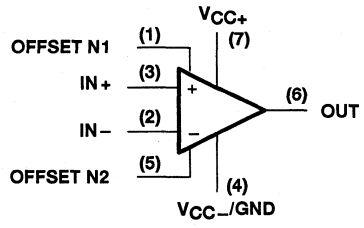
NC – No internal connection

TLE2021Y chip information

This chip, when properly assembled, display characteristics similar to the TLE2021. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

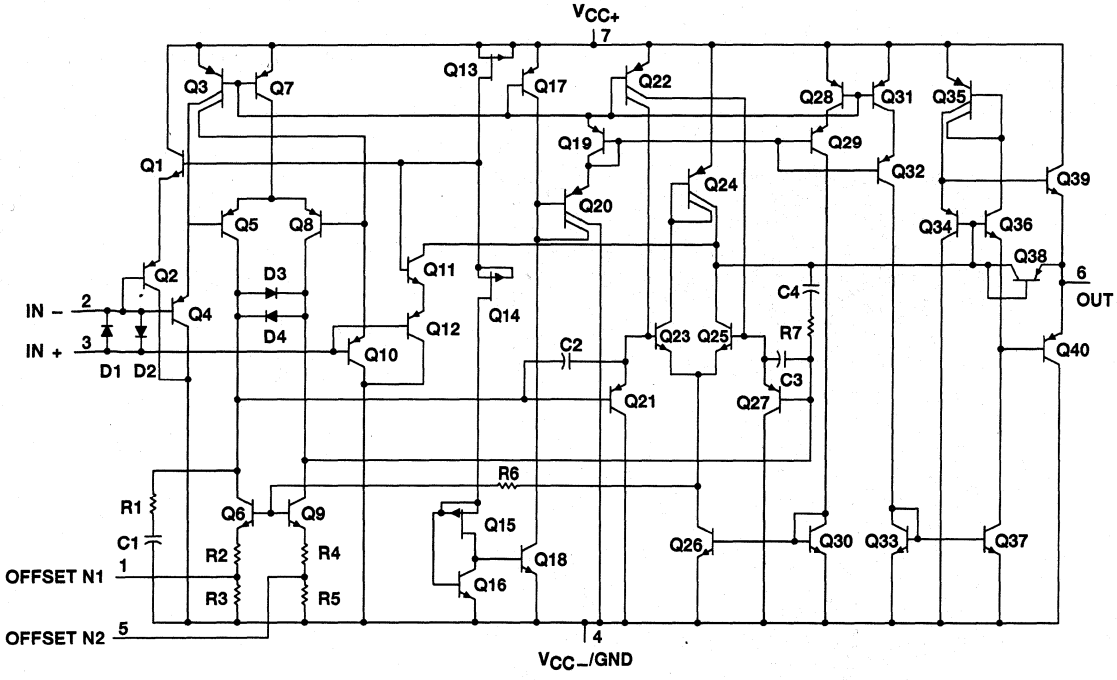
T_{Jmax}= 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



Pin numbers shown are for the D, DB, JG, P, and PW packages.

COMPONENT COUNT	
Transistors	40
Diodes	4
Resistors	7
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 20 V
Supply voltage, V_{CC-} (see Note 1) ..... −20 V
Differential input voltage, V_{ID} (see Note 2) ..... ±0.6 V
Input voltage range, V_I (any input, see Note 1) ..... $\pm V_{CC}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±20 mA
Total current into V_{CC+} ..... 20 mA
Total current out of V_{CC-} ..... 20 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DP, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current will flow if a differential input voltage in excess of approximately ±600 mV is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB, PW	525 mW	4.2 mW/°C	336 mW	—	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	668 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		±2	±20	±2	±20	±2	±20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	0	3.5	0	3.2	0	3.2	V
	$V_{CC\pm} = \pm 15$ V	−15	13.5	−15	13.2	−15	13.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021C			TLE2021AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	600		100	300	μV
			Full range			850			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005		μV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			3			3	
I_{IB}	Input bias current		25°C		25	70		25	65	nA
			Full range			70			65	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		V
			Full range	3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8	V
			Full range			0.85			0.85	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		V/μV
			Full range	0.3			0.3			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	110		85	110		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		170	230		170	230	μA
			Full range			230			230	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		5			5		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021C			TLE2021AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	500		80	200	µV
			Full range			750			500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			3			3	
I_{IB}	Input bias current		25°C		25	70		25	65	nA
			Full range			70			65	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.5			15 to 13.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		V
			Full range	13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.7			−13.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 10 kΩ	25°C	1	6.5		1	6.5		V/µV
			Full range	1			1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	115		100	115		dB
			Full range	96			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 0, No load	25°C		200	300		200	300	µA
			Full range			300			300	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		6			6		µA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021I			TLE2021AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	600		100	300	μV
			Full range			950			600	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005		μV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			4			4	
I_{IB}	Input bias current		25°C		25	70		25	65	nA
			Full range			70			65	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	−15 to 3.2			15 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		V
			Full range	3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8	V
			Full range			0.9			0.9	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		V/μV
			Full range	0.25			0.25			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	85	110		85	110		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		170	230		170	230	μA
			Full range			230			230	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		6			6		μA

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021I			TLE2021AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	500		80	200	µV
			Full range			850			500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3	nA
			Full range			4			4	
I_{IB}	Input bias current		25°C		25	70		25	65	nA
			Full range			70			65	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 3.2			15 to 3.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		V
			Full range	13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = 10 V, R_L = 10 kΩ	25°C	1	6.5		1	6.5		V/µV
			Full range	0.75			0.75			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	100	115		100	115		dB
			Full range	96			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ± 15 V	25°C	105	120		105	120		dB
			Full range	100			100			
I_{CC}	Supply current	V_O = 0 V, No load	25°C		200	300		200	300	µA
			Full range			300			300	
ΔI_{CC}	Supply current change over operating temperature range		Full range		7			7		µA

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021M			TLE2021AM			TLE2021BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	600		100	300		80	200	µV
			Full range			1100			600			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3		0.2	3	nA
			Full range			5			5			5	
I_{IB}	Input bias current		25°C		25	70		25	65		25	60	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.8			3.8			3.8			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.3	1.5		0.3	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	110		85	110		85	110		dB
			Full range	80			80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	105	120		105	120		105	120		dB
			Full range	100			100			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		170	230		170	230		170	230	µA
			Full range			230			230			230	
ΔI_{CC}	Supply current change over operating temperature range		Full range		9			9			9		µA

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2021M			TLE2021AM			TLE2021BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		120	500		80	200		40	100	µV
			Full range			1000			500			200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.2	3		0.2	3		0.2	3	nA
			Full range			5			5			5	
I_{IB}	Input bias current		25°C		25	70		25	65		25	60	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.2			−15 to 13.2			0 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.8			13.8			13.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	25°C	1	6.5		1	6.5		1	6.5		V/µV
			Full range	0.5			0.5			0.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	115		100	115		100	115		dB
			Full range	96			96			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ±15 V	25°C	105	120		105	120		105	120		dB
			Full range	100			100			100			
I_{CC}	Supply current	V_O = 0, No load	25°C		200	300		200	300		200	300	µA
			Full range			300			300			300	
ΔI_{CC}	Supply current change over operating temperature range		Full range		10			10			10		µA

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1	25°C		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		21	50		21	50		21		nV/Hz
		f = 1 kHz	25°C		17	30		17	30		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.09			0.09			0.9		pA/Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		1.2			1.2			1.2		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		42°			42°			42°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1V to 3 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/μs
			Full range	0.45			0.42			0.45			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19		nV/Hz
		f = 1 kHz	25°C		15	30		15	30		15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.09			0.09			0.09		pA/Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2			2			2		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		46°			46°			46°		

† Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –55°C to 125°C for the M-suffix devices.

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electrical characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

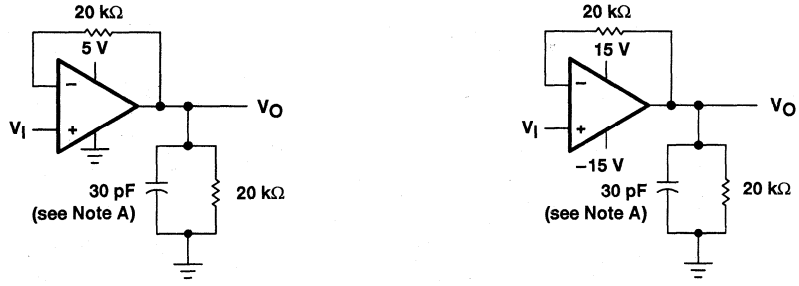
PARAMETER		TEST CONDITIONS	TLE2021Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		150	600	μV
	Input offset voltage long-term drift (see Note 4)			0.005		μV/mo
I_{IO}	Input offset current			0.5	5	nA
I_{IB}	Input bias current			35	70	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	0 to 3.5	– 0.3 to 4		V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	4	4.3		V
V_{OL}	Maximum low-level output voltage			0.7	0.8	V
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 to 4 V, R_L = 10 kΩ	0.3	1.5		V/μV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	85	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	100	115		dB
I_{CC}	Supply current	V_O = 2.5 V, No load		400	500	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2021Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V		0.5		V/μs
V_n	Equivalent input noise voltage	f = 10 Hz		21	50	nV/√Hz
		f = 1 kHz		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16		μV
		f = 0.1 to 10 Hz		0.47		
I_n	Equivalent input noise current			0.1		pA/√Hz
B_1	Unity-gain bandwidth			1.7		MHz
ϕ_m	Phase margin at unity gain			47°		

PARAMETER MEASUREMENT INFORMATION

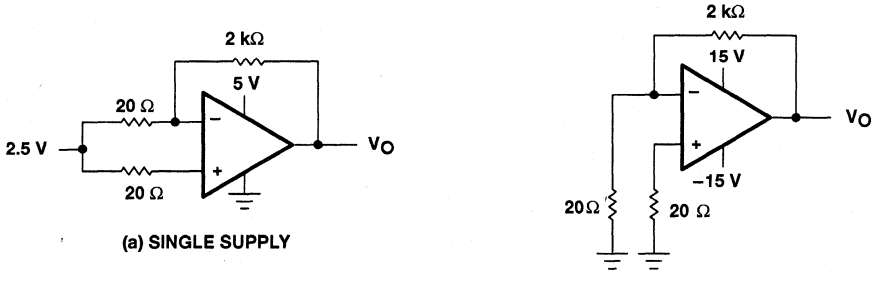


(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

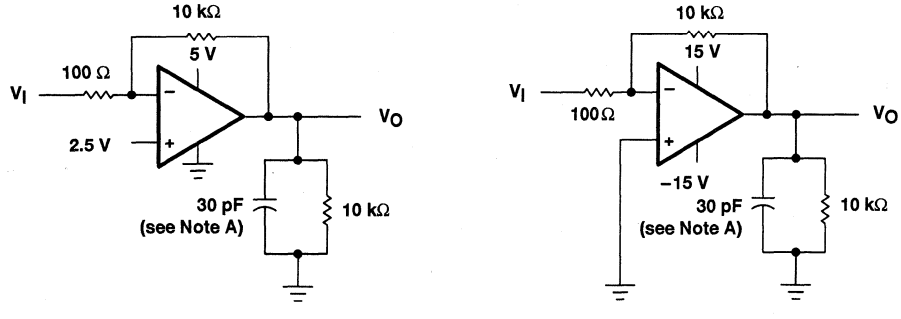
Figure 1. Slew-Rate Test Circuit



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

Figure 2. Noise-Voltage Test Circuit



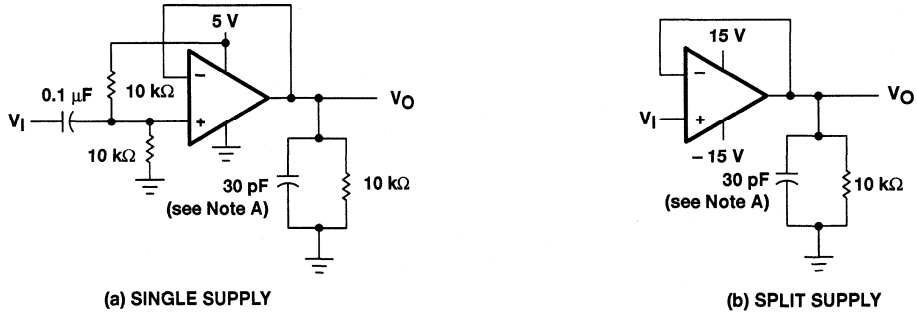
(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION



(a) SINGLE SUPPLY

(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance of initial devices from three wafer lots used for characterization.

TYPICAL CHARACTERISTICS

Table of Graphs

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V_{IO}	Input offset voltage	Distribution	5
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I_I	Input current	vs Differential input voltage	8
V_{OM}	Maximum peak output voltage	vs Output current vs Free-air temperature	9 10
V_{OH}	High-level output voltage	vs High-level output current vs Free-air temperature	11 12
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	13 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15, 16
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	19, 20 21, 22
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	23 24
CMRR	Common-mode rejection ratio	vs Frequency	25
SR	Slew rate	vs Free-air temperature	26
	Pulse response	Small signal Large signal	27, 28 29, 30
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	31 32
V_n	Equivalent input noise voltage	vs Frequency	33
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	34 35
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	36 37 38
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

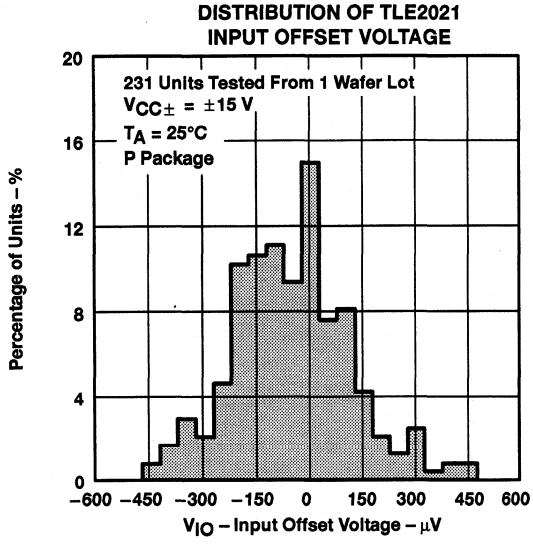


Figure 5

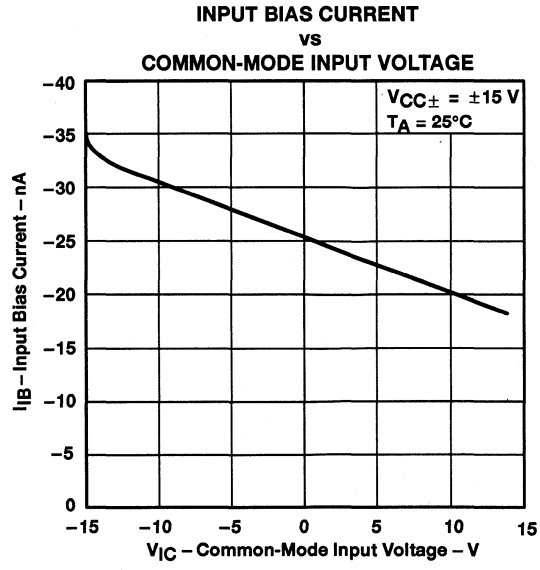


Figure 6

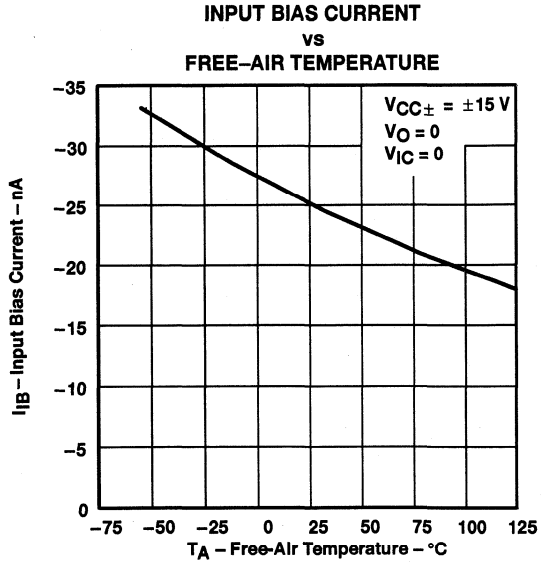


Figure 7

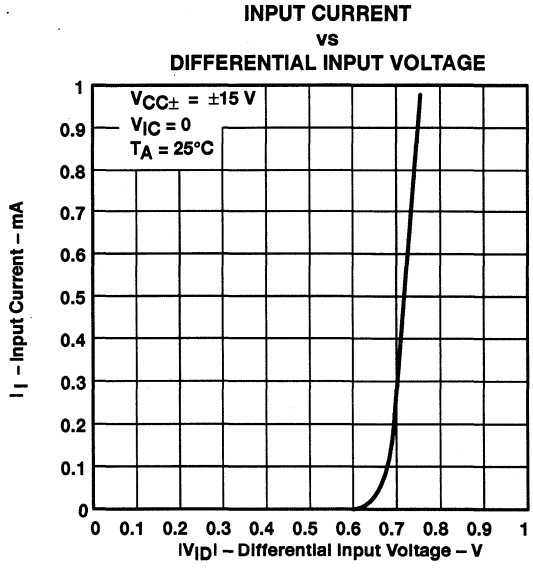


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

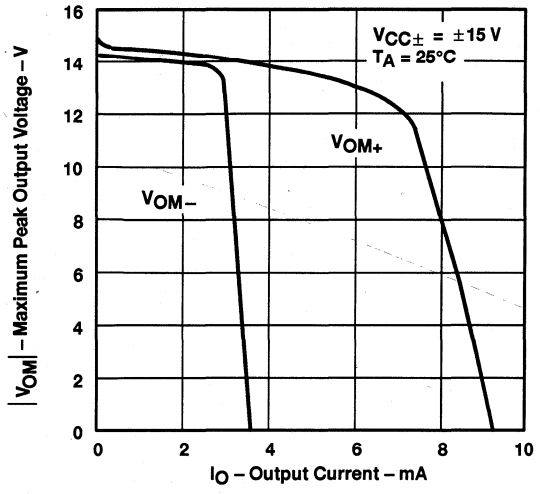


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

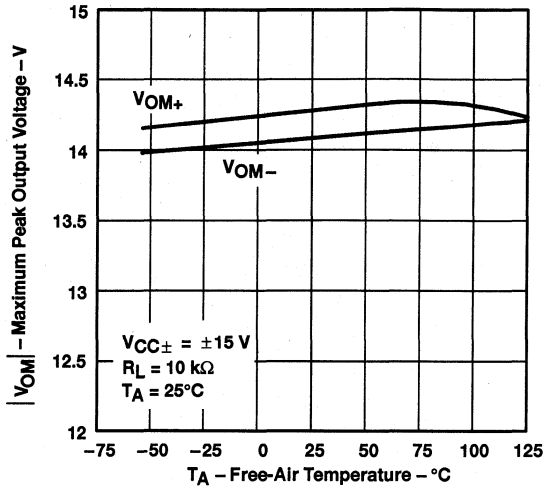


Figure 10

HIGH–LEVEL OUTPUT VOLTAGE
vs
HIGH–LEVEL OUTPUT CURRENT

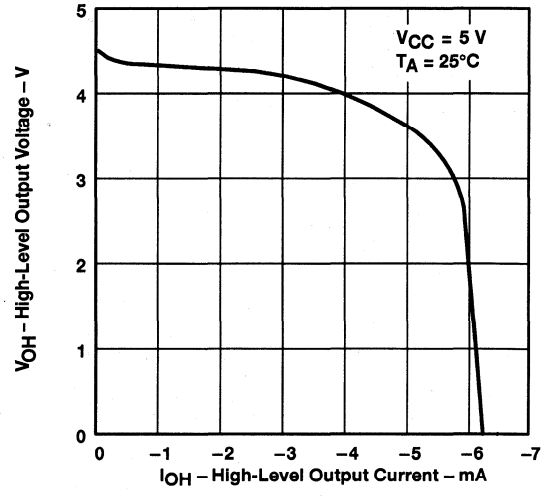


Figure 11

HIGH–LEVEL OUTPUT VOLTAGE
vs
FREE–AIR TEMPERATURE

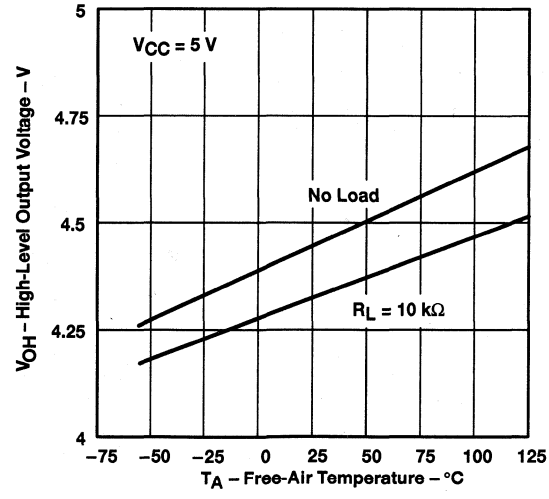


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

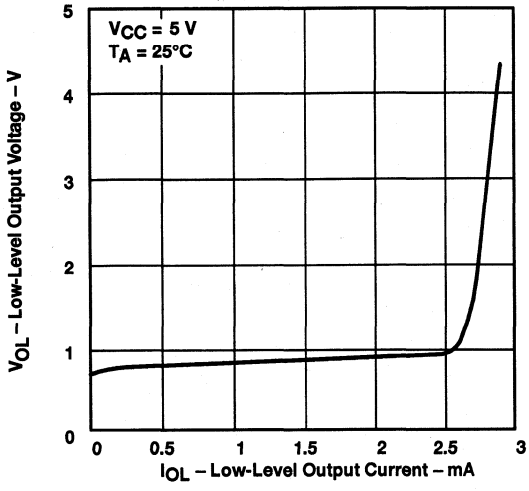


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

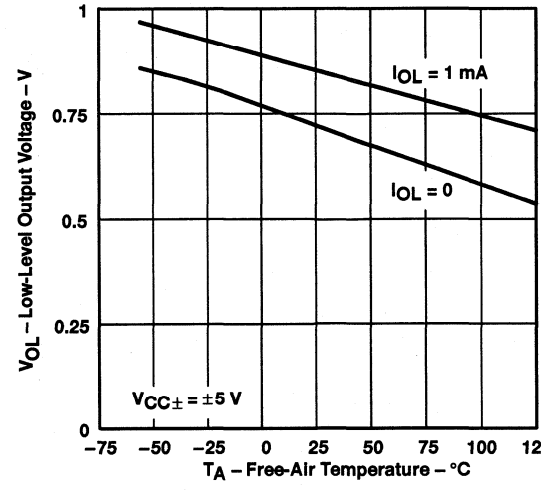


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

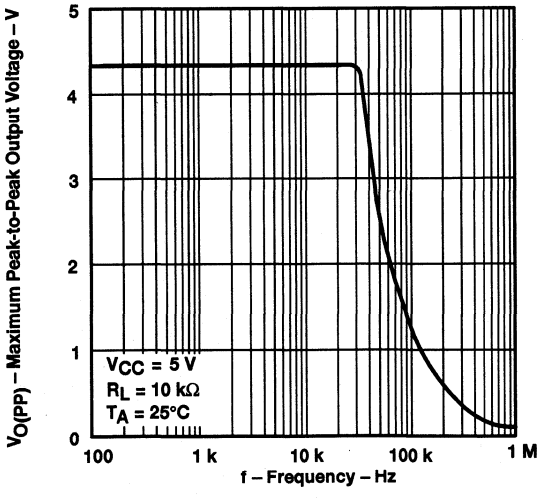


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

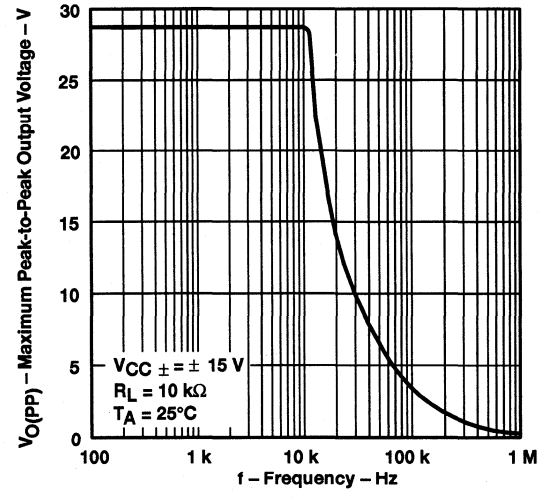


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

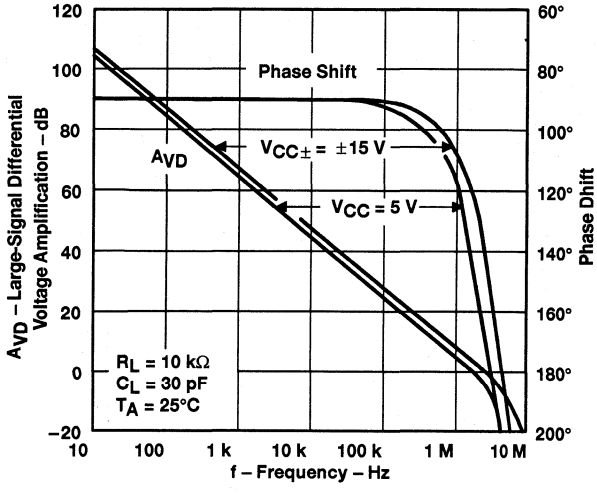


Figure 17

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE–AIR TEMPERATURE

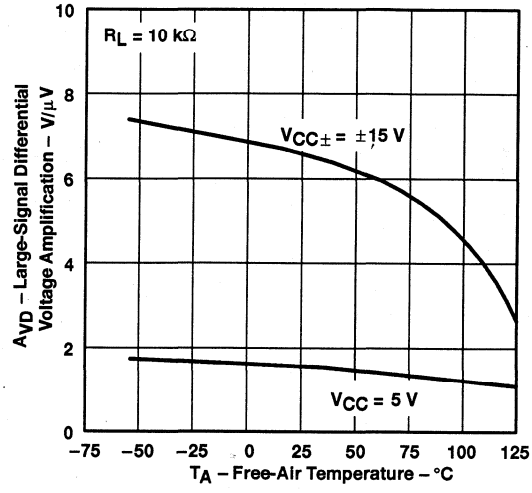


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

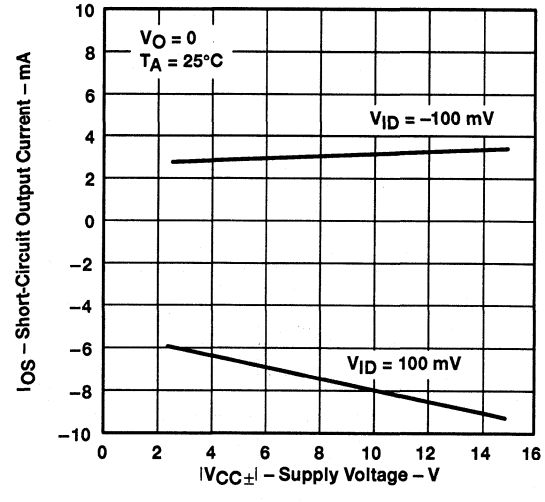


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

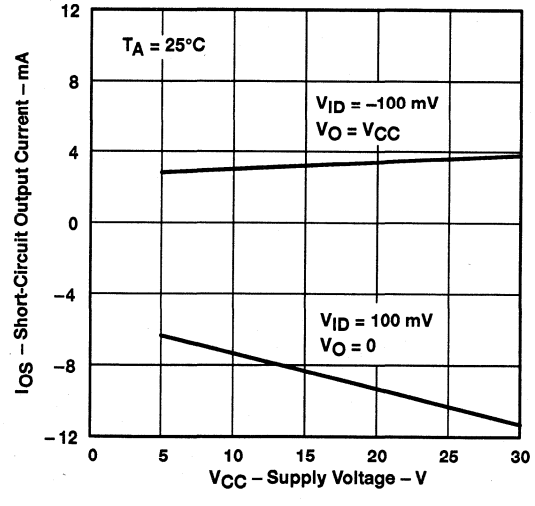


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

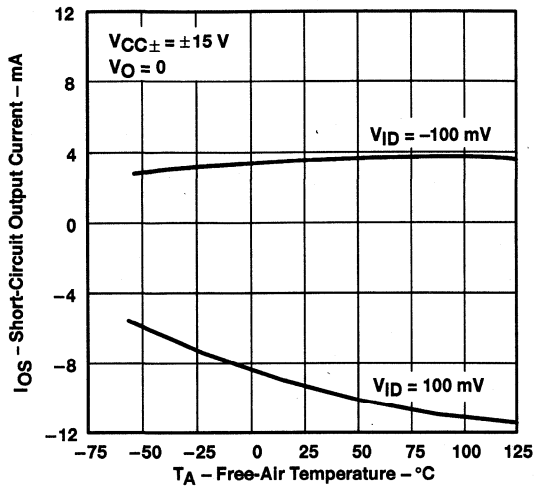


Figure 21

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

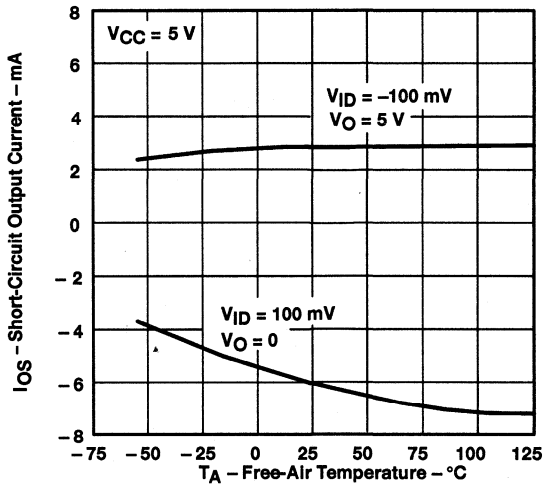


Figure 22

SUPPLY CURRENT vs SUPPLY VOLTAGE

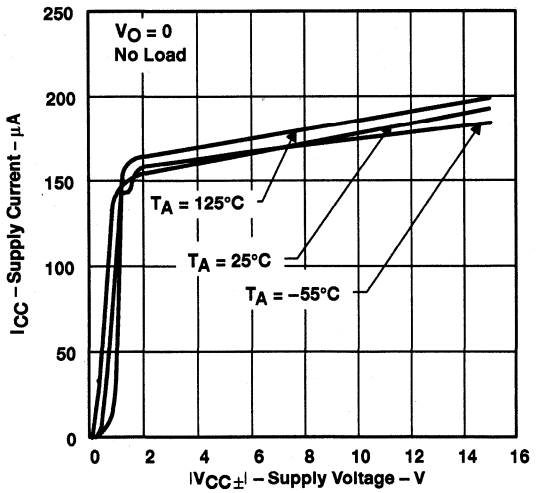


Figure 23

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

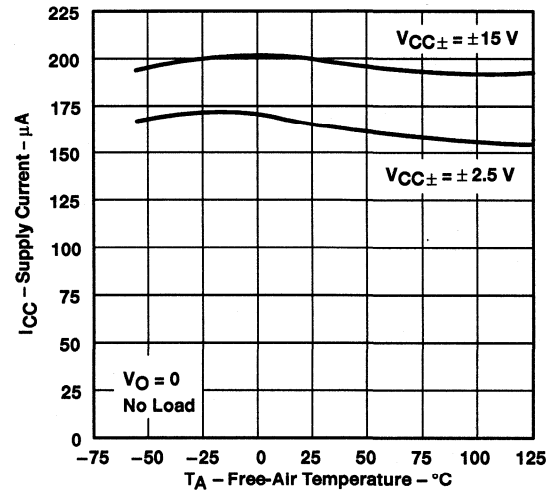


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

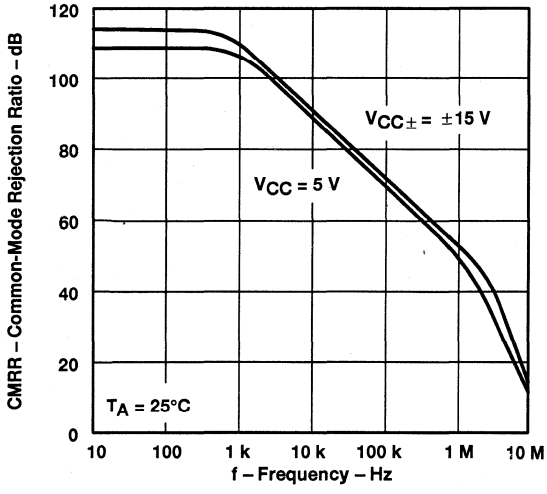


Figure 25

SLEW RATE vs FREE-AIR TEMPERATURE

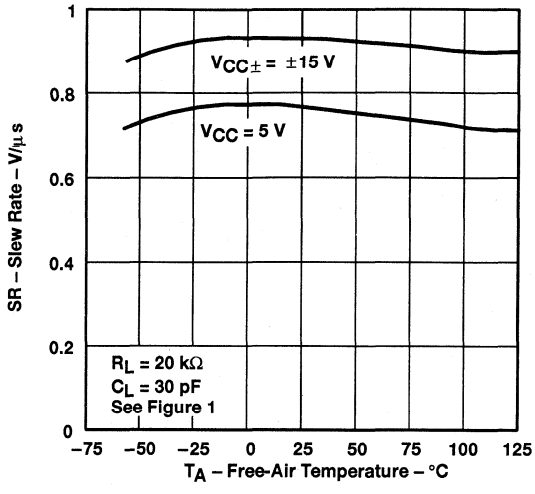


Figure 26

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

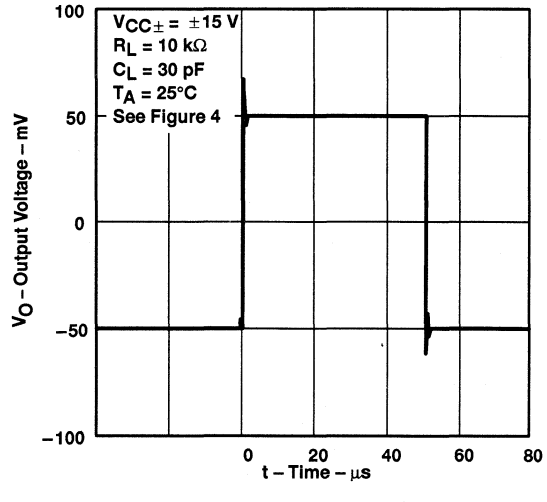


Figure 27

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

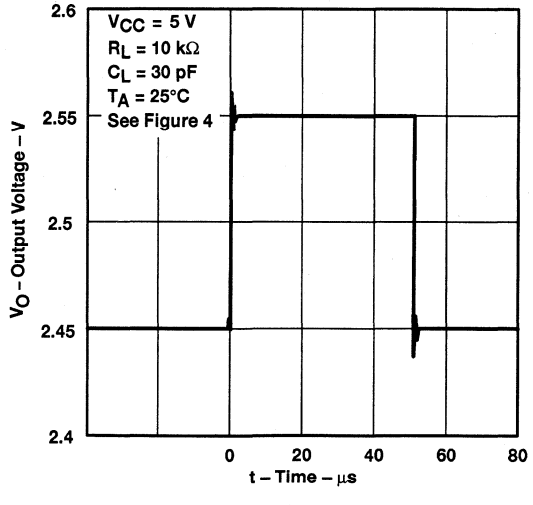


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

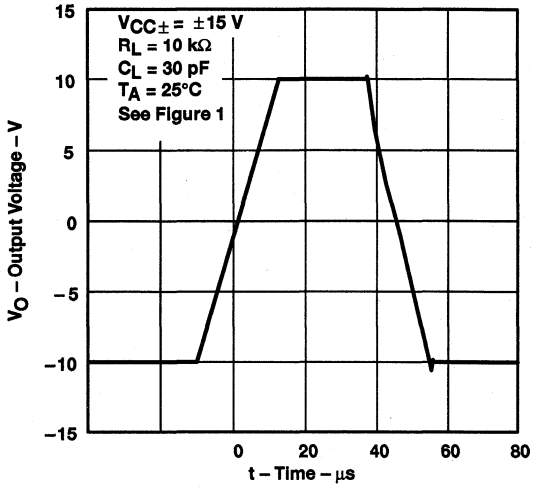


Figure 29

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

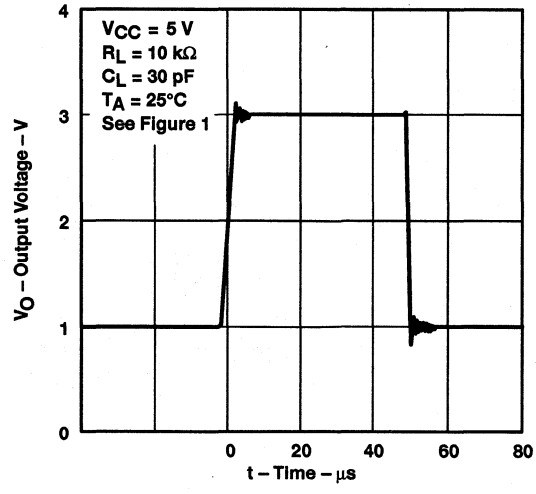


Figure 30

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

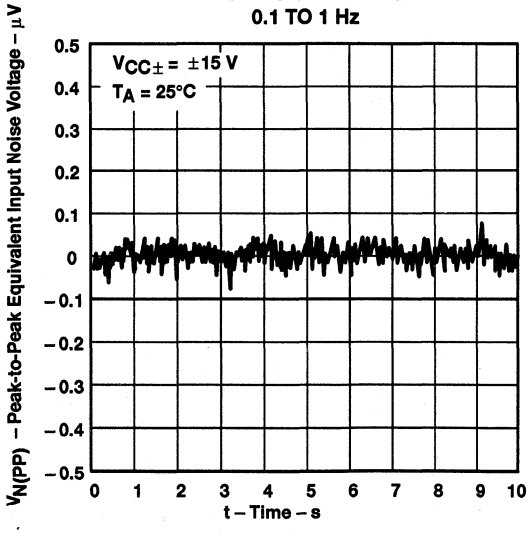


Figure 31

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

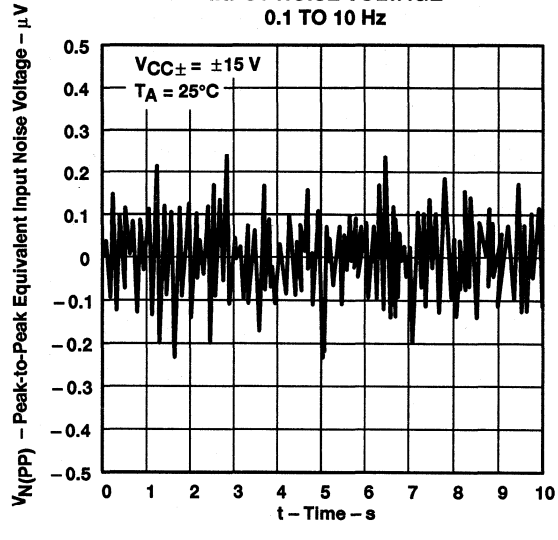


Figure 32

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

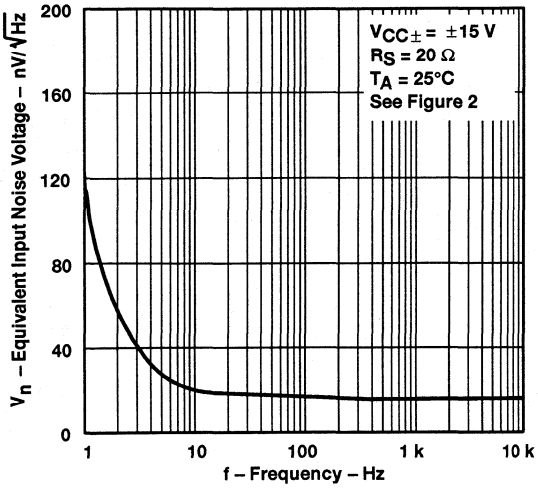


Figure 33

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

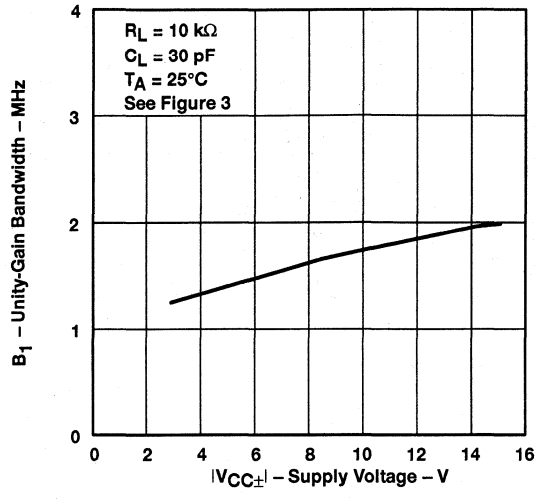


Figure 34

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

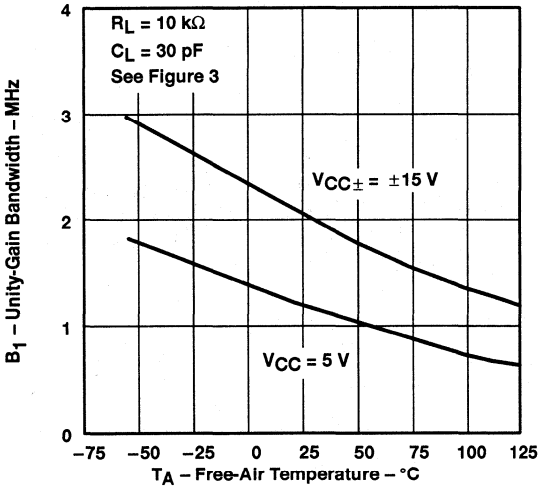


Figure 35

PHASE MARGIN vs SUPPLY VOLTAGE

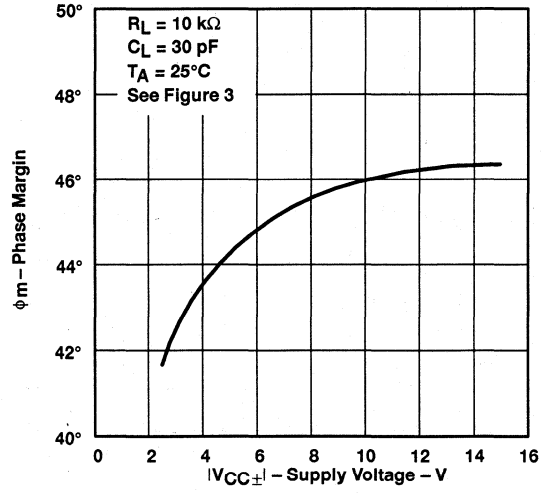


Figure 36

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

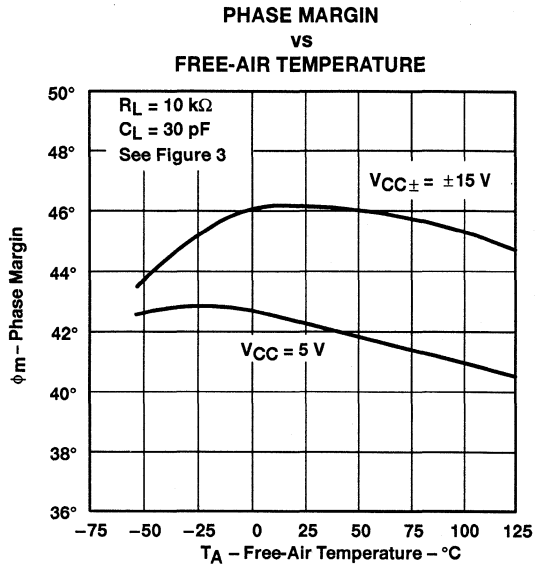


Figure 37

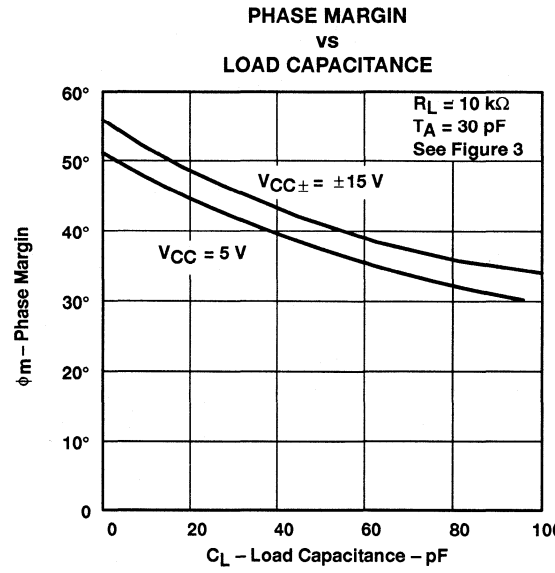


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

The TLE2021 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. This feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 39).

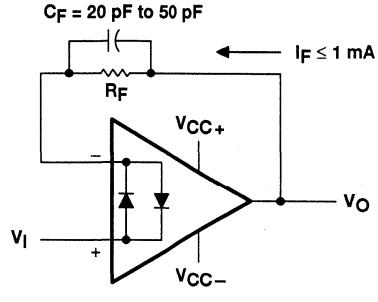


Figure 39. Voltage Follower

APPLICATION INFORMATION

Input offset voltage nulling

The TLE2021 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 40 can be connected as shown if this feature is desired. If external nulling is not needed, the null pins may be left disconnected.

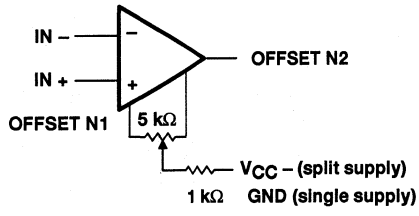


Figure 40. Input Offset Voltage Null Circuit

- **Supply Current . . . 500 μA Max**
- **High Unity-Gain Bandwidth . . . 2.8 MHz Typ**
- **High Slew Rate . . . 0.45 V/μs Min**
- **Supply-Current Change Over Military Temperature Range . . . 37 μA Typ**
- **Specified for Both 5-V Single-Supply and ±15-V Operation**
- **Phase-Reversal Protection**
- **High Open-Loop Gain 10 V/μV (140 dB) Typ**
- **Low Offset Voltage . . . 150 μV Max**
- **Offset Voltage Drift With Time 0.005 μV/mo Typ**
- **Low Input Bias Current . . . 50 nA Max**
- **Low Noise Voltage . . . 19 nV/√Hz Typ at f = 10 Hz**

description

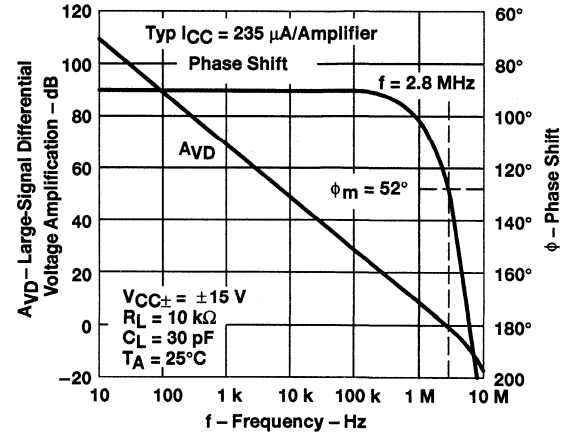
The TLE2022, TLE2022A, and TLE2022B devices are precision, high-speed, low-power operational amplifiers using Texas Instruments Excalibur process. These devices combine the best features of the OP221 with highly improved slew rate and unity-gain bandwidth.

The complementary bipolar Excalibur process utilizes isolated vertical pnp transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a patent-pending bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a precision device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

LARGE-SIGNAL DIFFERNTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT VS FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D)	SSOP (DBLE)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PWLE)	
0°C to 70°C	300 μV 500 μV	TLE2022ACD TLE2022CD	— TLE2022CDBLE	—	—	TLE2022ACP TLE2022CP	— TLE2022CPWLE	TLE2022Y
−40°C to 85°C	300 μV 500 μV	TLE2022AID TLE2022ID	—	—	—	TLE2022AIP TLE2022IP	—	—
−55°C to 125°C	150 μV 300 μV 500 μV	— TLE2022AMD TLE2022MD	—	— TLE2022AMFK TLE2022MFK	TLE2022BMJG TLE2022AMJG TLE2022MJG	— TLE2022AMP TLE2022MP	—	—

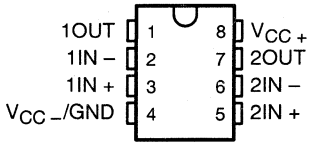
The D packages are available taped and reeled. Add the suffix R (e.g., TLE2022CDR). The DB and PW packages are only available left-end taped and reeled. Chips are tested at 25°C.

description (continued)

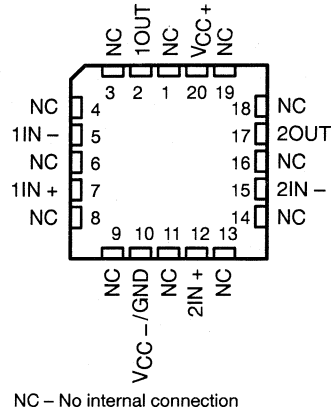
Available packaging options include small-outline and chip-carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

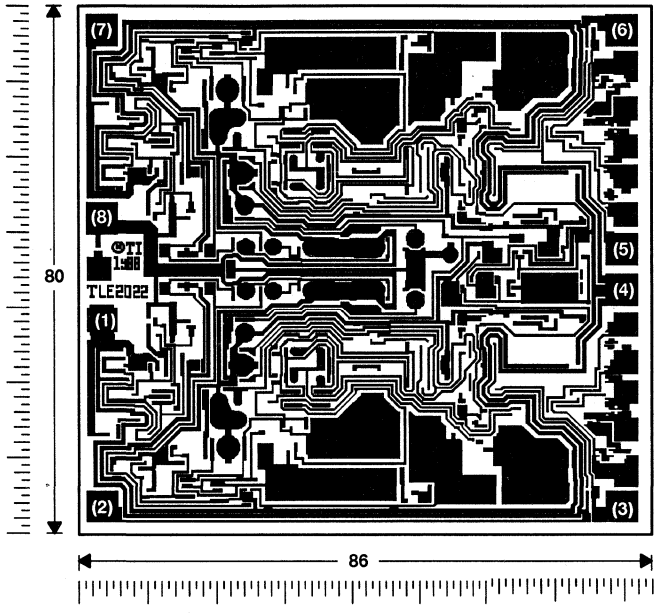


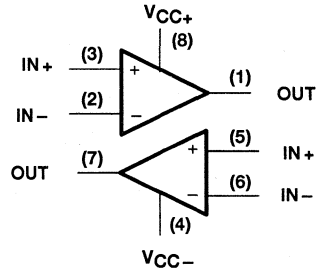
NC – No internal connection

TLE2022Y chip information

This chip, when properly assembled, displays characteristics similar to TLE2022. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

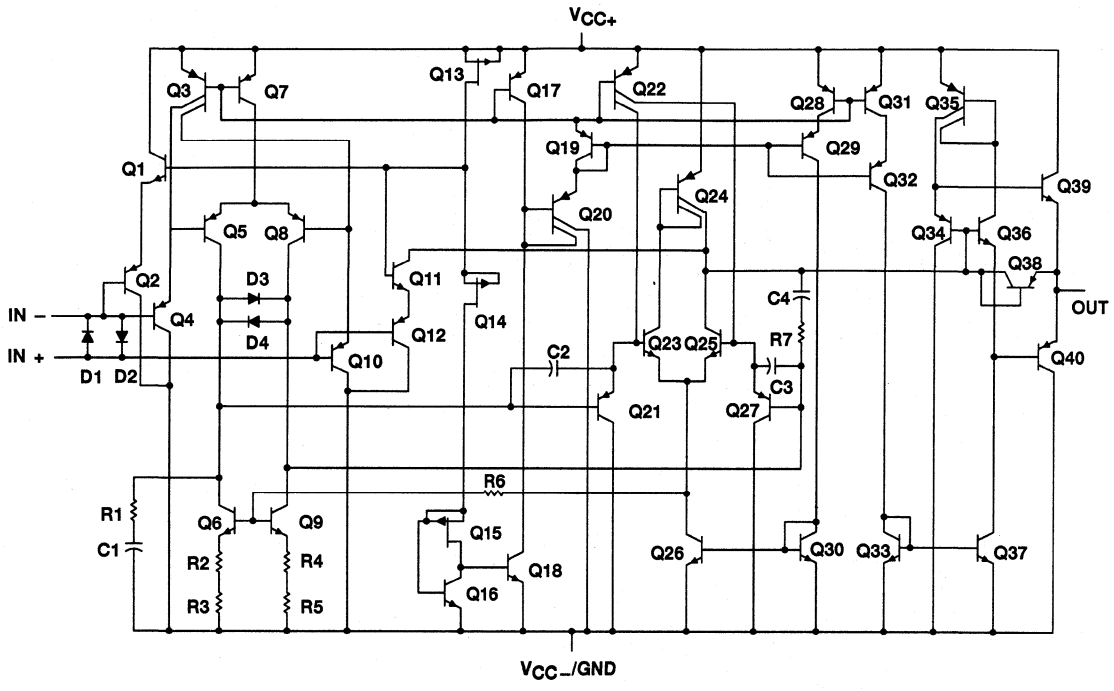
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	80
Diodes	8
Resistors	14
Capacitors	8

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 20 V
Supply voltage, V_{CC-} (see Note 1) ..... −20 V
Differential input voltage, V_{ID} (see Note 2) ..... ±0.6 V
Input voltage range, V_I (any input, see Note 1) ..... $V_{CC\pm}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±30 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current will flow if a differential input voltage in excess of approximately ±600 mV is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB, PW	525 mW	4.2 mW/°C	336 mW	273 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2	±20	±2	±20	±2	±20	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5$ V	0	3.5	0	3.2	0	3.2	V
	$V_{CC\pm} = \pm 15$ V	−15	13.5	−15	13.2	−15	13.2	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022C			TLE2022AC			TLE2022BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			600			400			250	μV
			Full range			800			550			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		μV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	70		33	65		30	60	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.5			0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.9			3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.85			0.85			0.85	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.4	1.5		0.5	1.5		V/μV
			Full range	0.3			0.4			0.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	100		87	102		90	105		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC} \pm / \Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		450	600		450	600		450	600	μA
			Full range			600			600			600	
ΔI_{CC}	Supply current change over operating temperature range		Full range		7			7			7		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022C			TLE2022AC			TLE2022BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		150	500		120	300		70	150	µV
			Full range			700			450			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	70		33	65		30	60	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.5			−15 to 13.5			−15 to 13.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.9			13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.7			−13.7			−13.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	25°C	0.8	4		1	7		1.5	10		V/µV
			Full range	0.8			1			1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	95	106		97	109		100	112		dB
			Full range	91			93			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 0, No load	25°C		550	700		550	700		550	700	µA
			Full range			700			700			700	
ΔI_{CC}	Supply current change over operating temperature range		Full range		9			9			9		µA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2022C			TLE2022AC			TLE2022BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2022C			TLE2022AC			TLE2022BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/μs
			Full range	0.45			0.45			0.45			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

† Full range is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022I			TLE2022AI			TLE2022BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			600			400			250	μV
			Full range			800			550			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		μV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	70		33	65		30	60	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	4	4.3		4	4.3		4	4.3		V
			Full range	3.9			3.9			3.9			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.9			0.9			0.9	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.3	1.5		0.4	1.5		0.5	1.5		V/μV
			Full range	0.2			0.2			0.2			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	100		87	102		90	105		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		450	600		450	600		450	600	μA
			Full range			600			600			600	
ΔI_{CC}	Supply current change over operating temperature range		Full range		15			15			15		μA

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022I			TLE2022AI			TLE2022BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		150	500		120	300		70	150	µV
			Full range			700			450			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	70		33	65		30	60	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.2			−15 to 13.2			−15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.9			13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L = 10 kΩ	25°C	0.8	4		1	7		1.5	10		V/µV
			Full range	0.8			1			1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	95	106		97	109		100	112		dB
			Full range	91			93			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±2.5 V to ±15 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 0, No load	25°C		550	700		550	700		550	700	µA
			Full range			700			700			700	
ΔI_{CC}	Supply current change over operating temperature range		Full range		30			30			30		µA

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2022I			TLE2022AI			TLE2022BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2022I			TLE2022AI			TLE2022BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/μs
			Full range	0.42			0.42			0.42			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

† Full range is –40°C to 85°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2022M			TLE2022AM			TLE2022BM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C			600			400			250	μV
				Full range			800			550			400	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2			2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.005			0.005			0.005		μV/mo
I_{IO}	Input offset current			25°C		0.5	5		0.4	4		0.3	3	nA
				Full range			5			4			3	
I_{IB}	Input bias current			25°C		35	70		33	65		30	60	nA
				Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
				Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OH}	High-level output voltage	R_L = 10 kΩ		25°C	4	4.3		4	4.3		4	4.3		V
				Full range	3.8			3.8			3.8			
V_{OL}	Low-level output voltage			25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
				Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V,	R_L = 10 kΩ	25°C	0.3	1.5		0.4	1.5		0.5	1.5		V/μV
				Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	100		87	102		90	105		dB
				Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V		25°C	100	115		103	118		105	120		dB
				Full range	95			98			100			
I_{CC}	Supply current	V_O = 2.5 V,	No load	25°C		450	600		450	600		450	600	μA
				Full range			600			600			600	
ΔI_{CC}	Supply current change over operating temperature range			Full range		37			37			37		μA

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2022M			TLE2022AM			TLE2022BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		150	500		120	300		70	150	µV
			Full range			700			450			300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.5	5		0.4	4		0.3	3	nA
			Full range			5			4			3	
I_{IB}	Input bias current		25°C		35	70		33	65		30	60	nA
			Full range			70			65			60	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.2			−15 to 13.2			−15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	14	14.3		14	14.3		14	14.3		V
			Full range	13.9			13.9			13.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	25°C	0.8	4		1	7		1.5	10		V/µV
			Full range	0.8			1			1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	95	106		97	109		100	112		dB
			Full range	91			93			96			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	100	115		103	118		105	120		dB
			Full range	95			98			100			
I_{CC}	Supply current	V_O = 0, No load	25°C		550	700		550	700		550	700	µA
			Full range			700			700			700	
ΔI_{CC}	Supply current change over operating temperature range		Full range		60			60			60		µA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2022M			TLE2022AM			TLE2022BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21			21			21		nV/√Hz
		f = 1 kHz		17			17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2022M			TLE2022AM			TLE2022BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.65		0.45	0.65		0.45	0.65		V/μs
			Full range	0.4			0.4			0.4			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19			19			19		nV/√Hz
		f = 1 kHz	25°C		15			15			15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

† Full range is 0°C to 70°C.

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electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

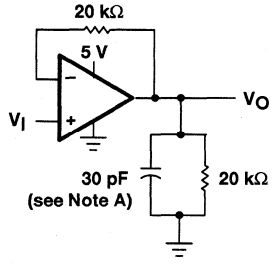
PARAMETER		TEST CONDITIONS	TLE2022Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		150	600	μV
	Input offset voltage long-term drift (see Note 4)			0.005		μV/mo
I_{IO}	Input offset current			0.5	5	nA
I_{IB}	Input bias current			35	70	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	0 to 3.5	−0.3 to 4		V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	4	4.3		V
V_{OL}	Maximum low-level output voltage			0.7	0.8	V
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 to 4 V, R_L = 10 kΩ	0.3	1.5		V/μV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	85	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	100	115		dB
I_{CC}	Supply current	V_O = 2.5 V, No load		450	600	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

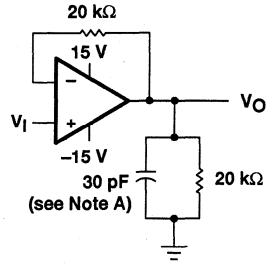
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2022Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50	nV/√Hz
		f = 1 kHz		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16		μV
		f = 0.1 to 10 Hz		0.47		
I_n	Equivalent input noise current			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°		

PARAMETER MEASUREMENT INFORMATION



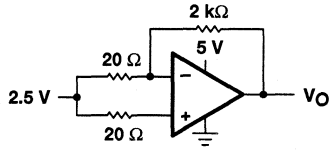
(a) SINGLE SUPPLY



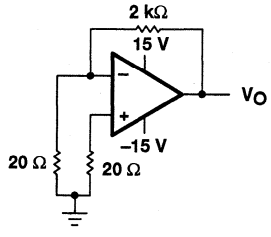
(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

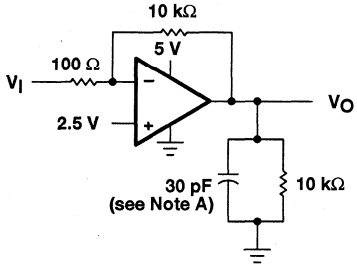


(a) SINGLE SUPPLY

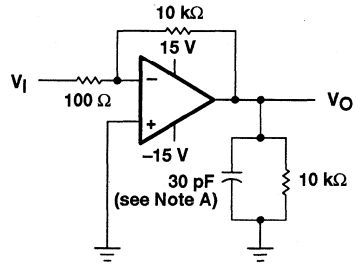


(b) SPLIT SUPPLY

Figure 2. Noise-Voltage Test Circuit



(a) SINGLE SUPPLY

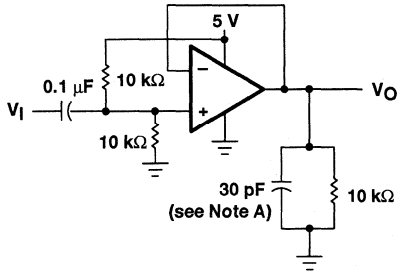


(b) SPLIT SUPPLY

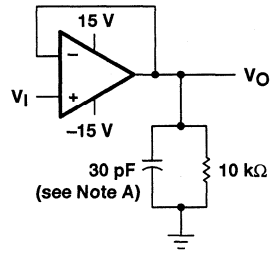
NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION



(a) SINGLE SUPPLY



(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	6 7
I_I	Input current	vs Differential input voltage	8
V_{OM}	Maximum peak output voltage	vs Output current vs Free-air temperature	9 10
V_{OH}	High-level output voltage	vs High-level output current vs Free-air temperature	11 12
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	13 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	15, 16
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	19, 21 20, 22
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	23 24
CMRR	Common-mode rejection ratio	vs Frequency	25
SR	Slew rate	vs Free-air temperature	26
	Pulse response	Small signal Large signal	27, 28 29, 30
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	31 32
V_n	Equivalent input noise voltage	vs Frequency	33
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	34 35
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	36 37 38
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

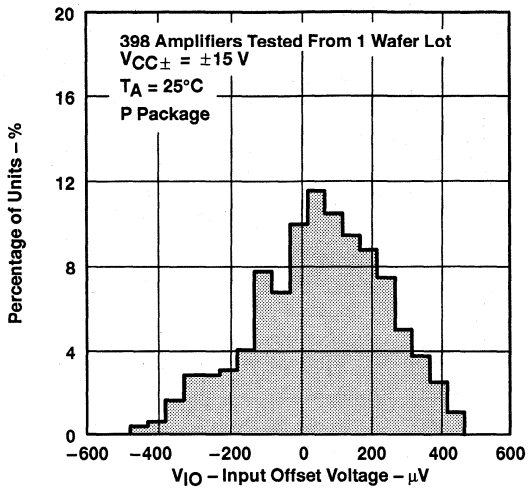


Figure 5

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

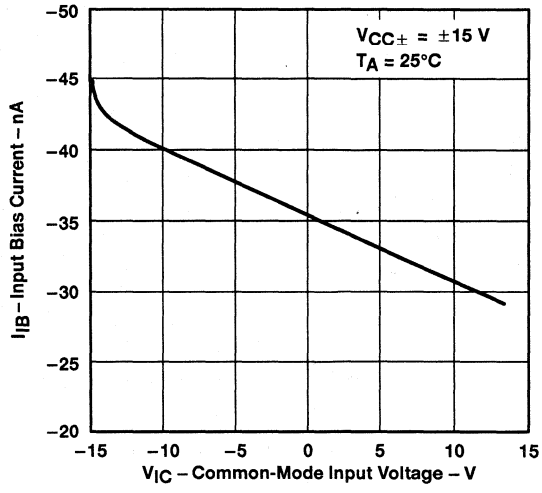


Figure 6

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

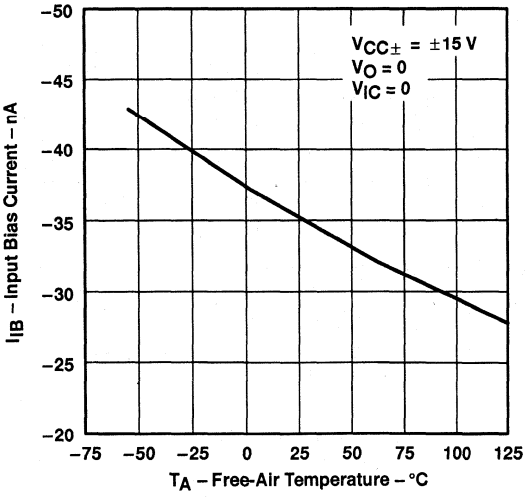


Figure 7

INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

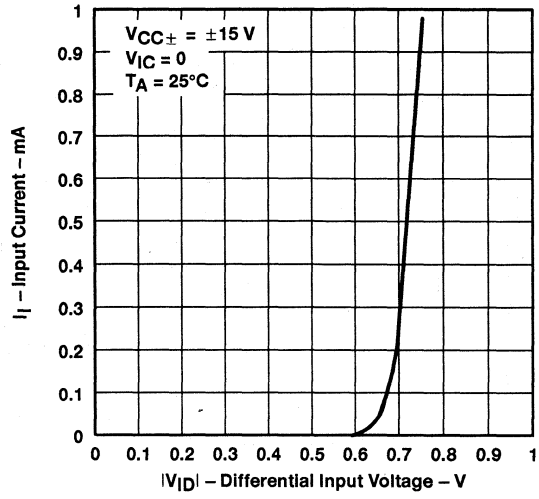


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

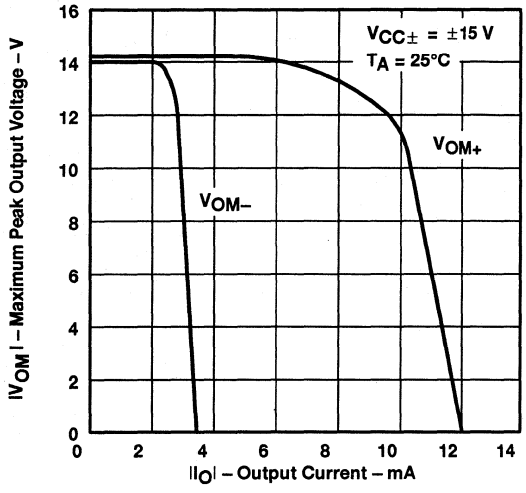


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

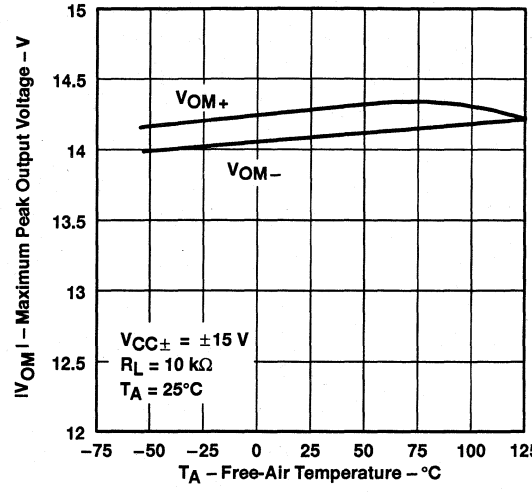


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

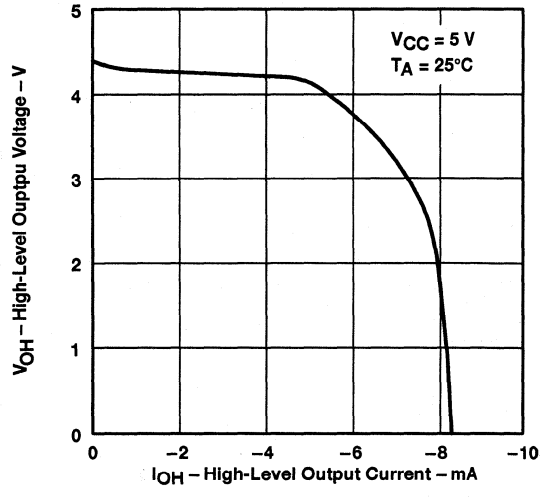


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

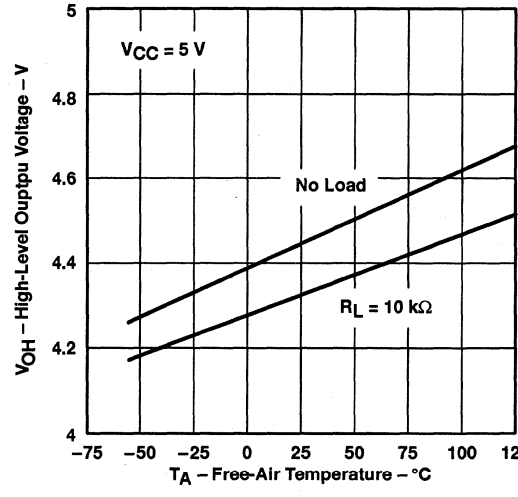


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

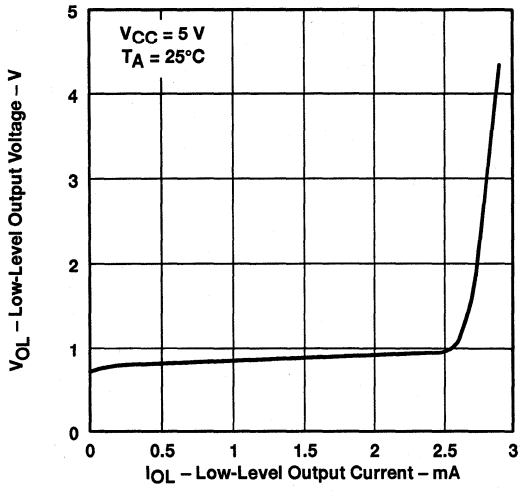


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

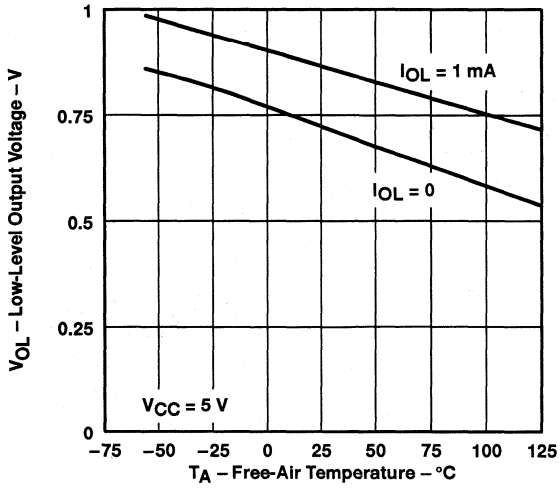


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

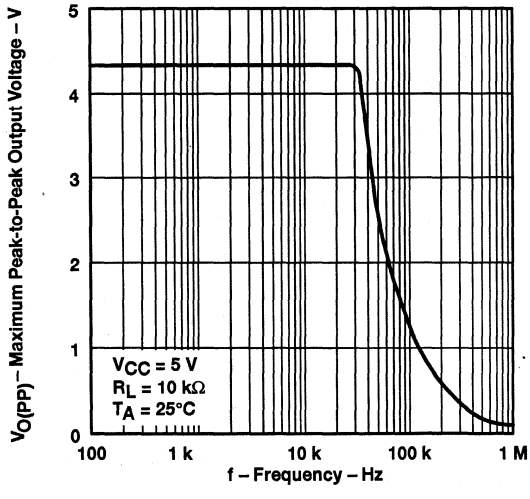


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

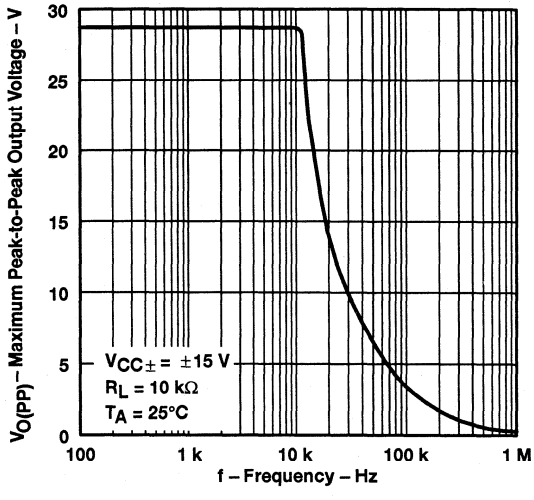


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION and PHASE SHIFT vs FREQUENCY

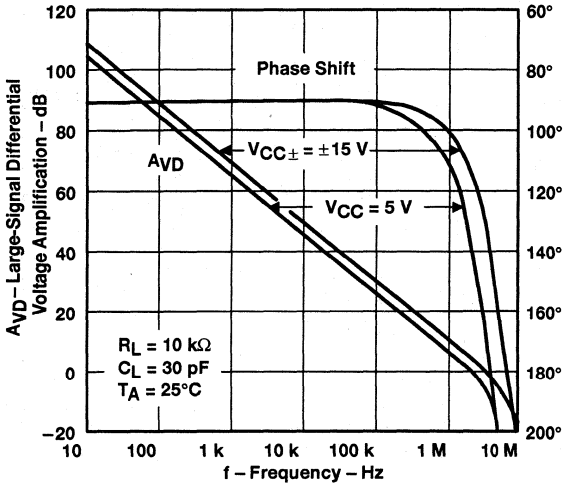


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

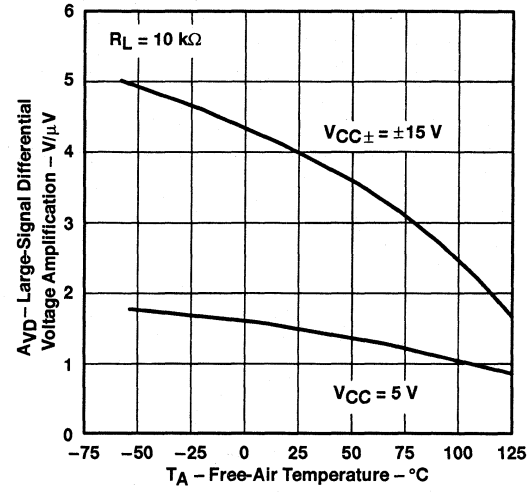


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

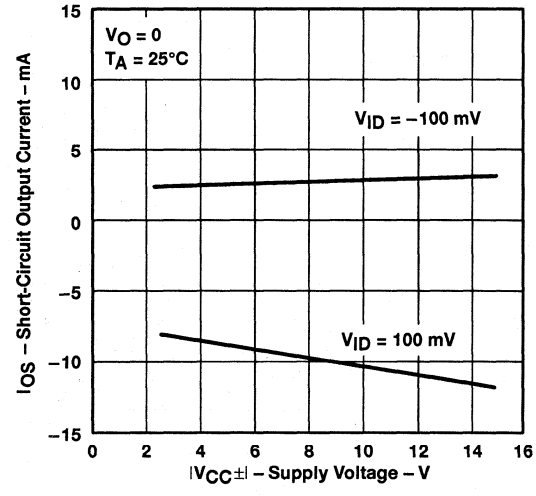


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

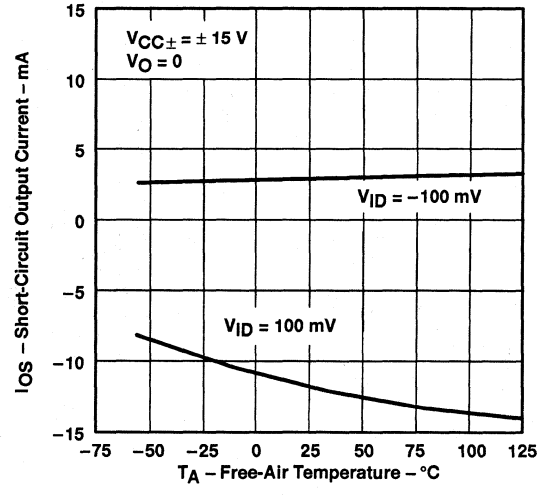


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

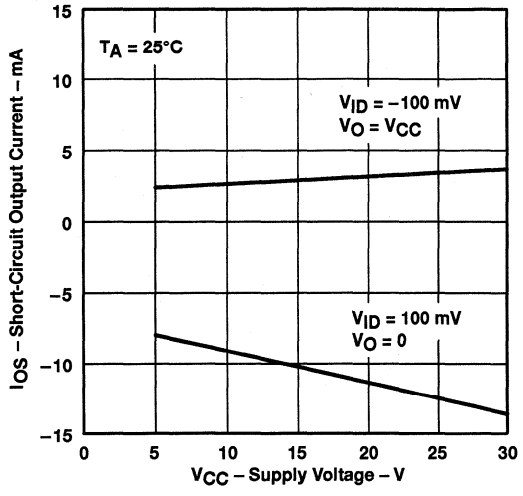


Figure 21

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

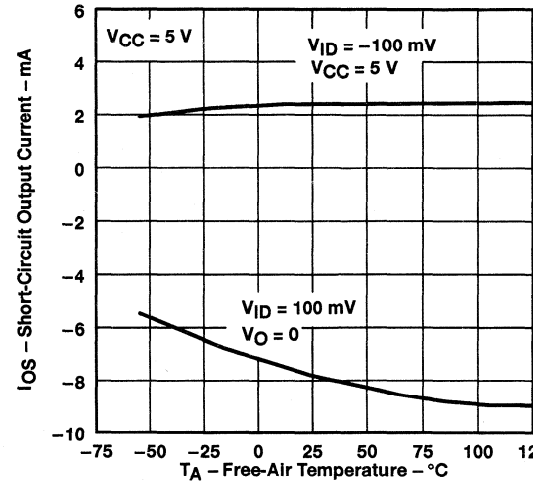


Figure 22

SUPPLY CURRENT vs SUPPLY VOLTAGE

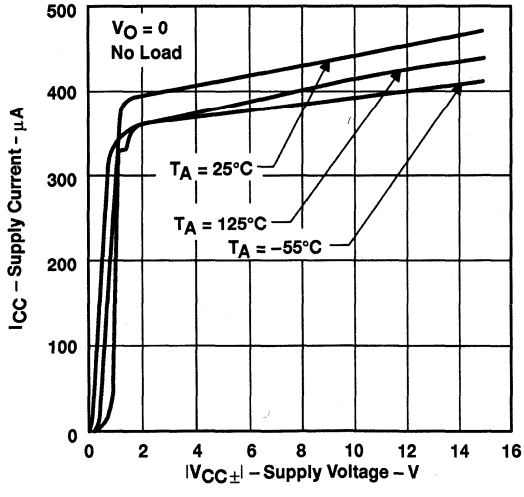


Figure 23

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

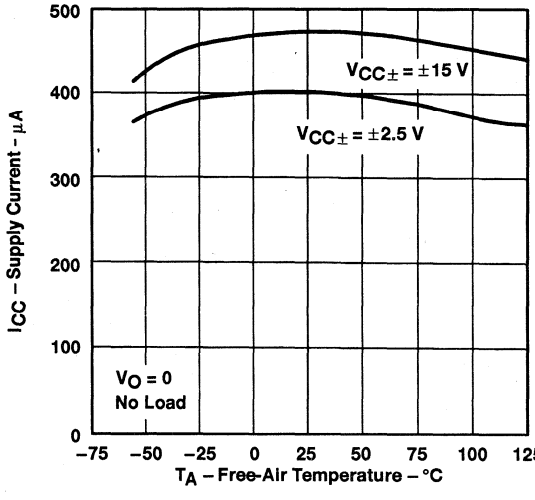


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

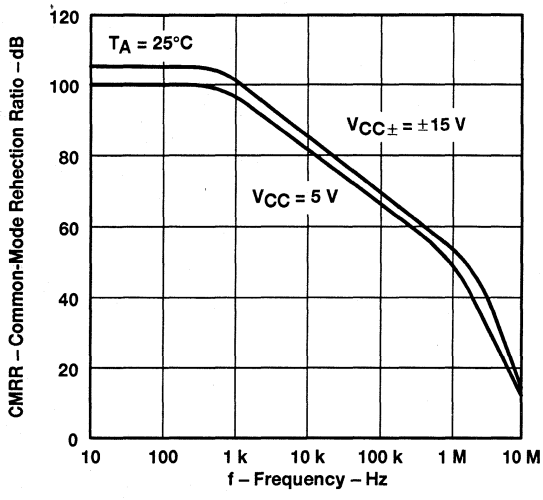


Figure 25

SLEW RATE
vs
FREE-AIR TEMPERATURE

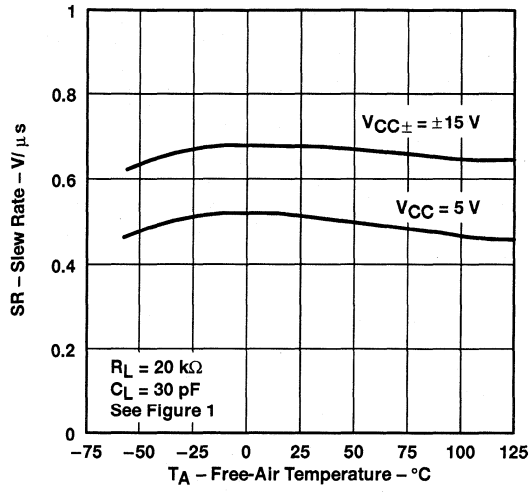


Figure 26

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

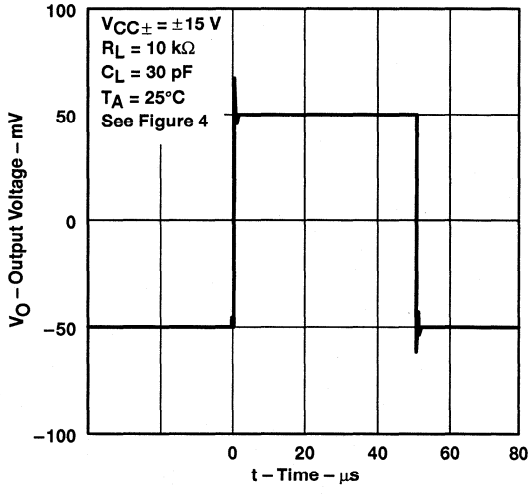


Figure 27

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

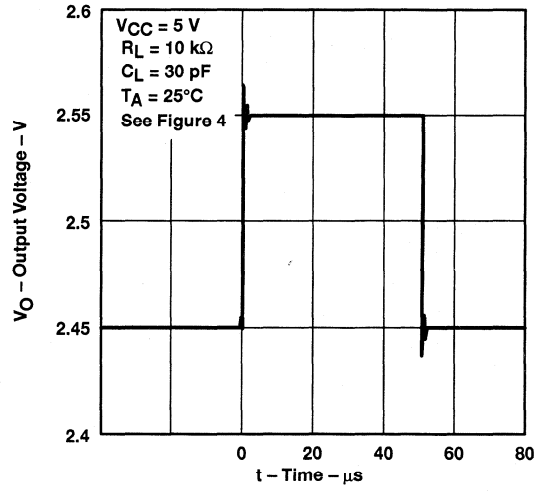


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

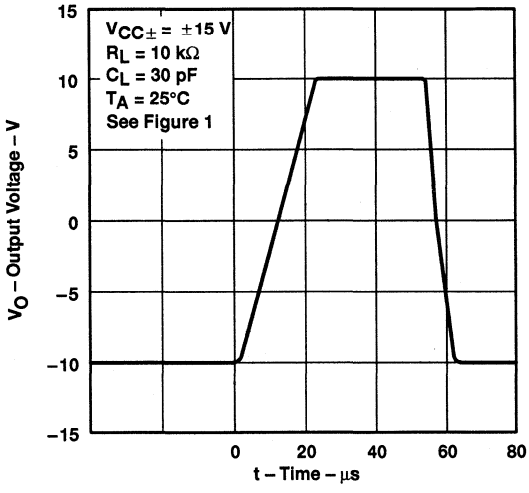


Figure 29

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

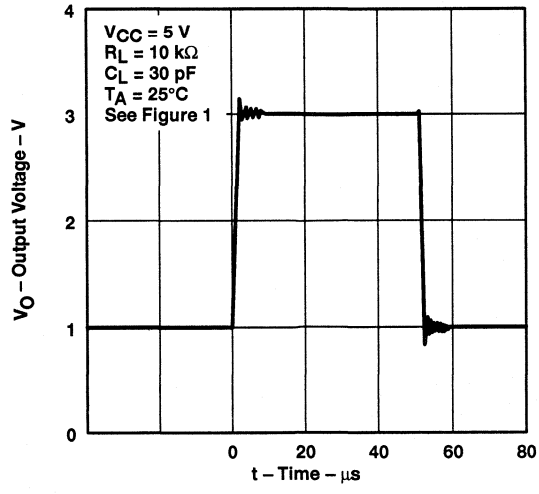


Figure 30

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

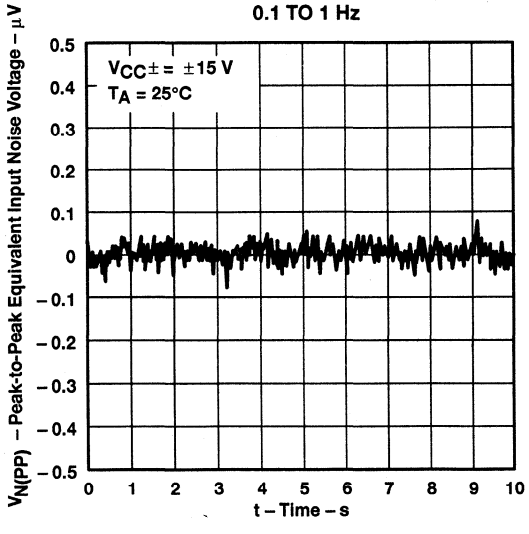


Figure 31

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

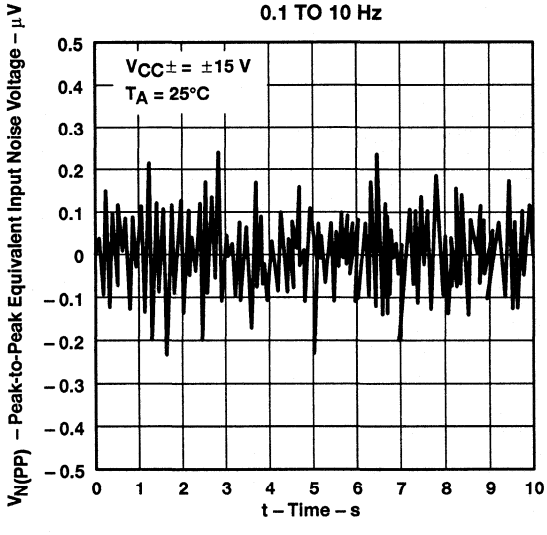


Figure 32

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

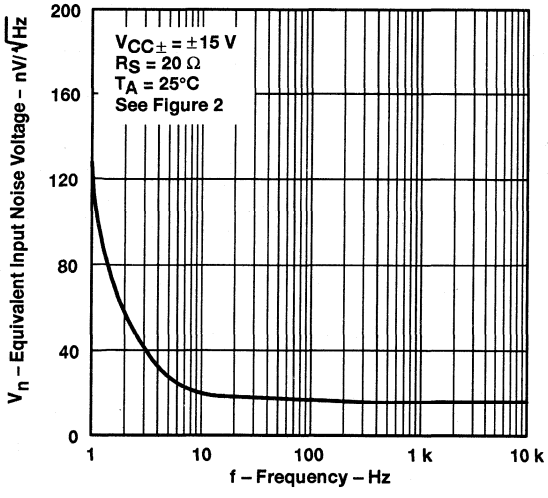


Figure 33

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

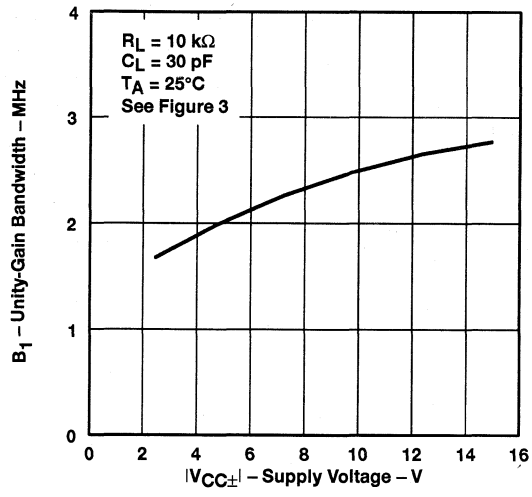


Figure 34

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

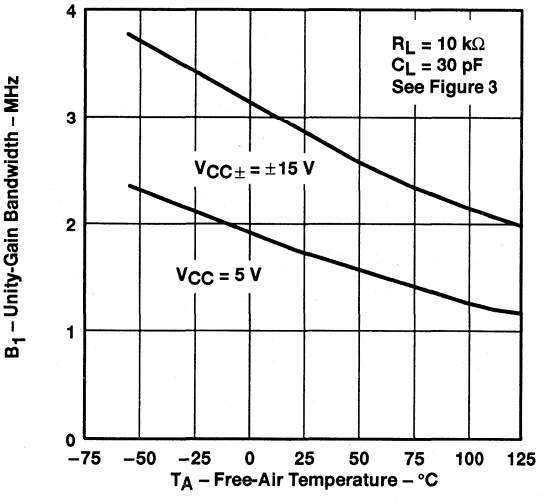


Figure 35

PHASE MARGIN vs SUPPLY VOLTAGE

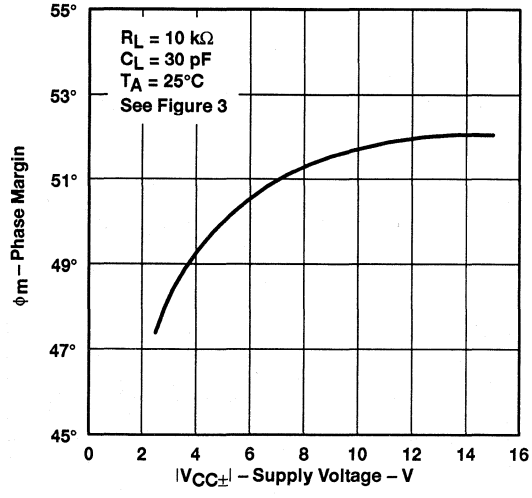


Figure 36

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

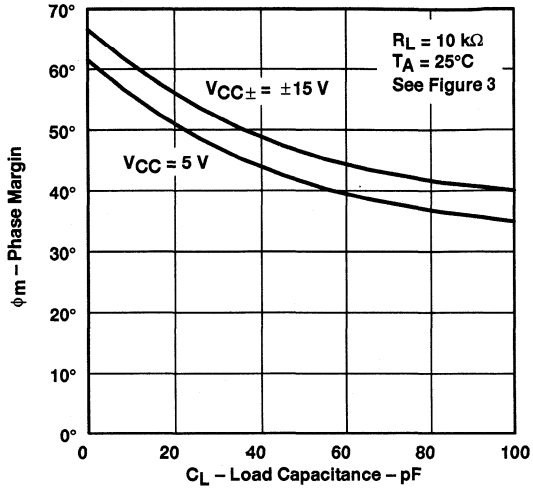


Figure 37

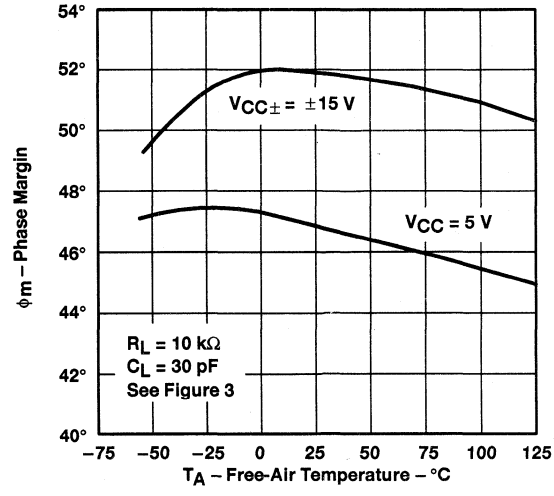


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

The TLE2022 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 39).

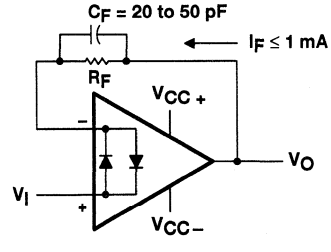


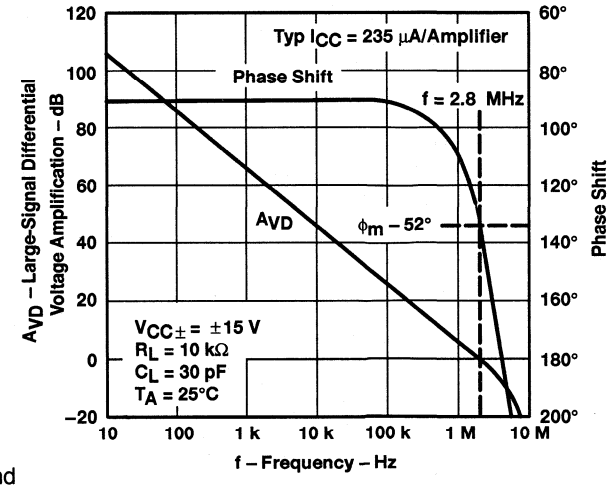
Figure 39. Voltage Follower

Input characteristics

The input of any unused amplifiers should be tied to ground to avoid possible oscillation.

- **Supply Current . . . 1 mA Max**
- **High Unity-Gain Bandwidth . . . 2.8 MHz Typ**
- **High Slew Rate . . . 0.45 V/μs Min**
- **Supply-Current Change Over Military Temperature Range . . . 50 μA Typ**
- **Specified for Both 5 V/GND and ±15-V Operation**
- **Phase-Reversal Protection**
- **High Open-Loop Gain 7 V/μV (137 dB) Typ**
- **Low Offset Voltage . . . 500 μV Max**
- **Offset Voltage Drift With Time 0.005 μV/mo Typ**
- **Low Input Bias Current . . . 50 nA Max**
- **Low Noise Voltage . . . 19 nV/Hz Typ at f = 10 Hz**

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

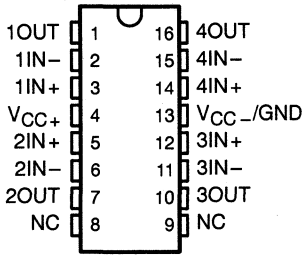


description

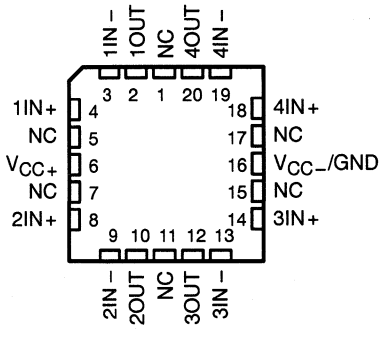
The TLE2024, TLE2024A, TLE2024B, and TLE2024Y devices are precision, high-speed, low-power operational amplifiers using Texas Instruments Excalibur process. These devices combine the best features of the OP421 with highly improved slew rate, unity-gain bandwidth, and input offset voltage. The complementary bipolar Excalibur process utilizes isolated vertical pnp transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a precision device remains a precision device even with changes in temperature and over years of use.

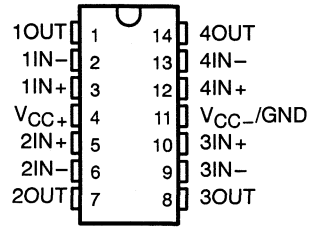
DW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



J OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description (continued)

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

A variety of available packaging options includes small-outline and chip-carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

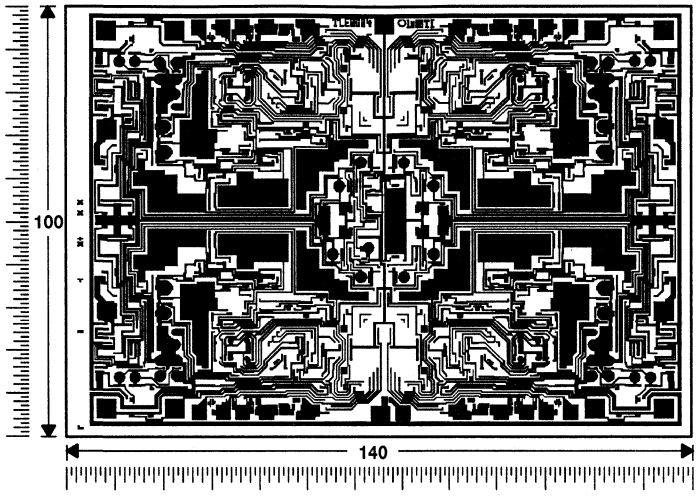
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	500 μV	TLE2024BCDW	—	—	TLE2024BCN	—
	750 μV	TLE2024ADCDW			TLE2024ACN	—
	1000 μV	TLE2024CDW			TLE2024CN	TLE2024Y
–40°C to 85°C	500 μV	TLE2024BIDW	—	—	TLE2024BIN	—
	750 μV	TLE2024AIDW			TLE2024AIN	
	1000 μV	TLE2024IDW			TLE2024IN	
–55°C to 125°C	500 μV	TLE2024BMDW	TLE2024BMFK	TLE2024BMJ	TLE2024BMN	—
	750 μV	TLE2024AMDW	TLE2024AMFK	TLE2024AMJ	TLE2024AMN	
	1000 μV	TLE2024MDW	TLE2024MFK	TLE2024MJ	TLE2024MN	

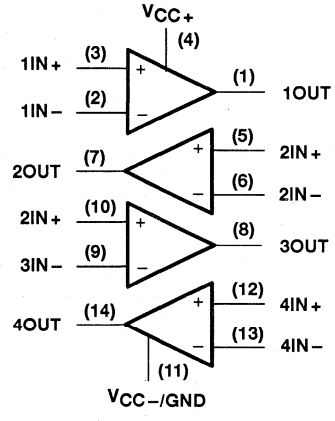
The D packages are available taped and reeled. Add the R suffix to device type (e.g., TLE2024BCDWR). Chips are tested at 25°C.

TLE2024Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2024. Thermal compression or ultrasonic bonding may be used on the doped aluminum-bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

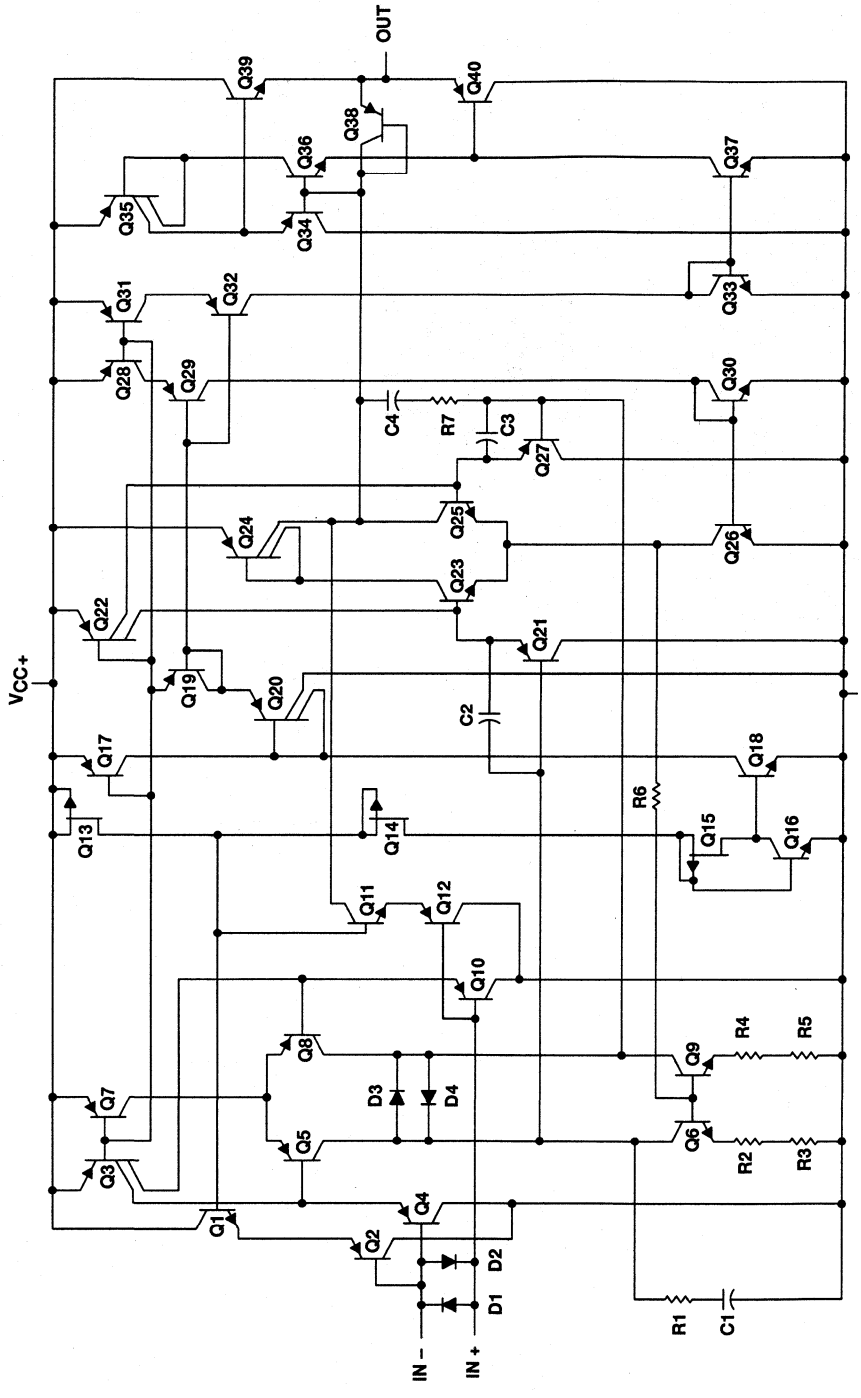
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	160
Diodes	16
Resistors	28
Capacitors	16

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 20 V
Supply voltage, V_{CC-} (see Note 1) ..... −20 V
Differential input voltage, V_{ID} (see Note 2) ..... ±0.6 V
Input voltage, V_I (any input, see Note 1) ..... $V_{CC\pm}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±40 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current will flow if a differential input voltage in excess of approximately ±600 mV is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2	±20	±2	±20	±2	±20	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0	3.5	0	3.2	0	3.2	V
	$V_{CC\pm}$ = ±15 V	−15	13.5	−15	13.2	−15	13.2	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024C			TLE2024AC			TLE2024BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1100			850			600	µV
			Full range			1300			1050			800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			6			5			4	
I_{IB}	Input bias current		25°C		45	70		40	65		35	60	nA
			Full range			75			70			65	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.5			0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	R_L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V
			Full range	3.7			3.7			3.8			
V_{OL}	Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	80	90		82	92		85	95		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to 30 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 2.5 V, No load	25°C		800	1200		800	1200		800	1200	µA
			Full range			1200			1200			1200	
ΔI_{CC}	Supply current change over operating temperature range		Full range		15			15			15		µA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024C			TLE2024AC			TLE2024BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1000			750			500	µV
			Full range			1200			950			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			6			5			4	
I_{IB}	Input bias current		25°C		50	70		45	65		40	60	nA
			Full range			75			70			65	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.5			−15 to 13.5			−15 to 13.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	13.8	14.1		13.9	14.2		14	14.3		V
			Full range	13.7			13.8			3.9			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	25°C	0.4	2		0.8	4		1	7		V/µV
			Full range	0.4			0.8			1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	92	102		94	105		97	108		dB
			Full range	88			90			93			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 0, No load	25°C		1050	1400		1050	1400		1050	1400	µA
			Full range			1400			1400			1400	
ΔI_{CC}	Supply current change over operating temperature range		Full range		20			20			20		µA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2024C			TLE2024AC			TLE2024BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024C			TLE2024AC			TLE2024BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.7		0.45	0.7		0.45	0.7		V/μs
			Full range	0.45			0.45			0.45			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

† Full range is 0°C to 70°C.

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electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024I			TLE2024AI			TLE2024BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1100			850			600	µV
			Full range			1300			1050			800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			7			6			5	
I_{IB}	Input bias current		25°C		45	70		40	65		35	60	nA
			Full range			80			75			70	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V
			Full range	3.7			3.7			3.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	80	90		82	92		85	95		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 0, No load	25°C		800	1200		800	1200		800	1200	µA
			Full range			1200			1200			1200	
ΔI_{CC}	Supply current change over operating temperature range		Full range		30			30			30		µA

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024I			TLE2024AI			TLE2024BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1000			750			500	µV
			Full range			1200			950			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			7			6			5	
I_{IB}	Input bias current		25°C		50	70		45	65		40	60	nA
			Full range			80			75			70	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.2			−15 to 13.2			−15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	13.8	14.1		13.9	14.2		14	14.3		V
			Full range	13.7			13.7			13.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	25°C	0.4	2		0.8	4		1	7		V/µV
			Full range	0.4			0.8			1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	92	102		94	105		97	108		dB
			Full range	88			90			93			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 0, No load	25°C		1050	1400		1050	1400		1050	1400	µA
			Full range			1400			1400			1400	
ΔI_{CC}	Supply current change over operating temperature range		Full range		50			50			50		µA

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2024I			TLE2024AI			TLE2024BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21	50		21	50		21	50	nV/√Hz
		f = 1 kHz		17	30		17	30		17	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024I			TLE2024AI			TLE2024BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.7		0.45	0.7		0.45	0.7		V/μs
			Full range	0.42			0.42			0.42			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19	50		19	50		19	50	nV/√Hz
		f = 1 kHz	25°C		15	30		15	30		15	30	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

† Full range is −40°C to 70°C.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024M			TLE2024AM			TLE2024BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1100			850			600	µV
			Full range			1300			1050			800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005			0.005		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			10			9			8	
I_{IB}	Input bias current		25°C		45	70		40	65		35	60	nA
			Full range			90			85			80	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		0 to 3.5	−0.3 to 4		V
			Full range	0 to 3.2			0 to 3.2			0 to 3.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	3.9	4.2		3.9	4.2		4	4.3		V
			Full range	3.7			3.7			3.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
			Full range			0.95			0.95			0.95	
A_{VD}	Large-signal differential voltage amplification	V_O = 1.4 V to 4 V, R_L = 10 kΩ	25°C	0.2	1.5		0.3	1.5		0.4	1.5		V/µV
			Full range	0.1			0.1			0.1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	80	90		82	92		85	95		dB
			Full range	80			82			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 0, No load	25°C		800	1200		800	1200		800	1200	µA
			Full range			1200			1200			1200	
ΔI_{CC}	Supply current change over operating temperature range		Full range		50			50			50		µA

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024M			TLE2024AM			TLE2024BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C			1000			750			500	µV
			Full range			1200			950			700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2			.2		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		µV/mo
I_{IO}	Input offset current		25°C		0.6	6		0.5	5		0.4	4	nA
			Full range			10			9			8	
I_{IB}	Input bias current		25°C		50	70		45	65		40	60	nA
			Full range			90			85			80	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		−15 to 13.5	−15.3 to 14		V
			Full range	−15 to 13.2			−15 to 13.2			−15 to 13.2			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	13.8	14.1		13.9	14.2		14	14.3		V
			Full range	13.7			13.7			13.8			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−13.7	−14.1		−13.7	−14.1		−13.7	−14.1		V
			Full range	−13.6			−13.6			−13.6			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	25°C	0.4	2		0.8	4		1	7		V/µV
			Full range	0.4			0.8			1			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	92	102		94	105		97	108		dB
			Full range	88			90			93			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V	25°C	98	112		100	115		103	117		dB
			Full range	93			95			98			
I_{CC}	Supply current	V_O = 0, No load	25°C		1050	1400		1050	1400		1050	1400	µA
			Full range			1400			1400			1400	
ΔI_{CC}	Supply current change over operating temperature range		Full range		85			85			85		µA

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2024M			TLE2024AM			TLE2024BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 3 V, See Figure 1		0.5			0.5			0.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21			21			21		nV/√Hz
		f = 1 kHz		17			17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz		0.47			0.47			0.47		
I_n	Equivalent input noise current			0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3		1.7			1.7			1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°			47°			47°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2024M			TLE2024AM			TLE2024BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±10 V, See Figure 1	25°C	0.45	0.7		0.45	0.7		0.45	0.7		V/μs
			Full range	0.4			0.4			0.4			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19			19			19		nV/√Hz
		f = 1 kHz	25°C		15			15			15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16			0.16			0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47			0.47			0.47		
I_n	Equivalent input noise current		25°C		0.1			0.1			0.1		pA/√Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8			2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°			52°			52°		

† Full range is −55°C to 125°C.

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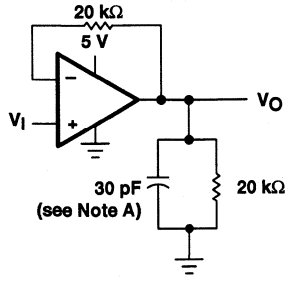
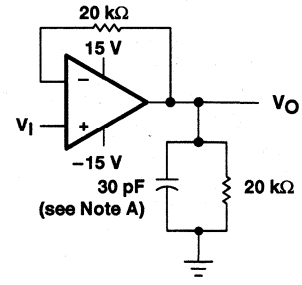
PARAMETER MEASUREMENT INFORMATION



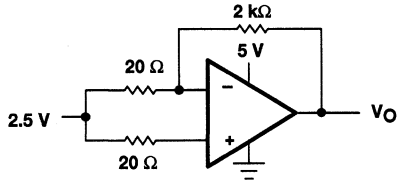
(a) SINGLE SUPPLY



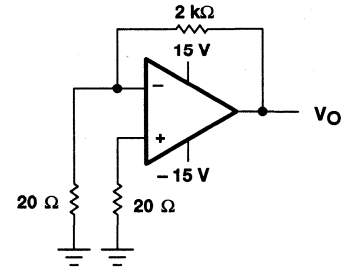
(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

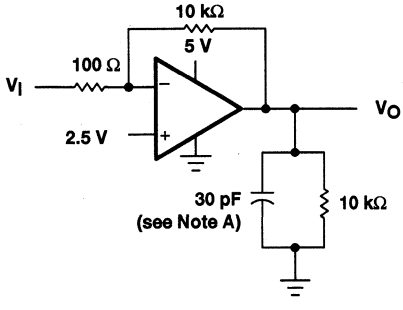


(a) SINGLE SUPPLY

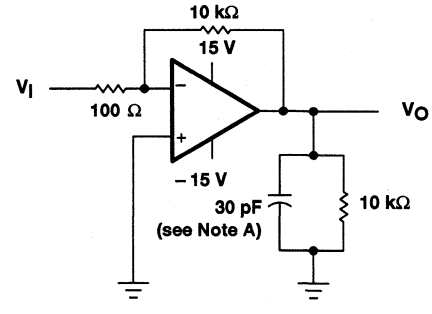


(b) SPLIT SUPPLY

Figure 2. Noise-Voltage Test Circuit



(a) SINGLE SUPPLY

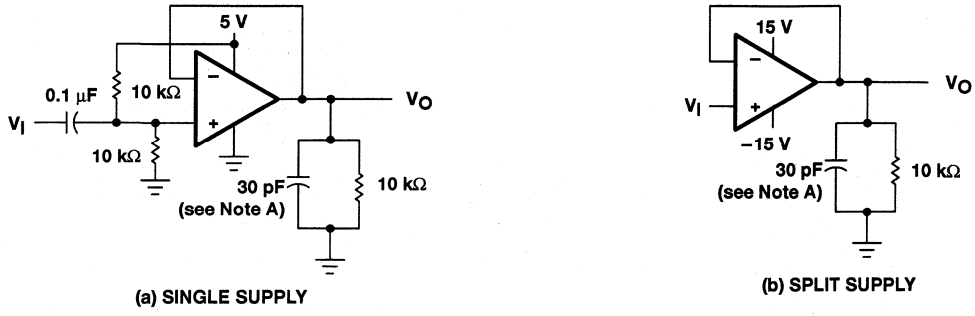


(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	6 7
I_I	Input current	vs Differential input voltage	8
V_{OM}	Maximum peak output voltage	vs Output current vs Free-air temperature	9 10
V_{OH}	High-level output voltage	vs High-level output current vs Free-air temperature	11 12
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	13 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15, 16
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	17 18
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	19, 21 20, 22
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	23 24
CMRR	Common-mode rejection ratio	vs Frequency	25
SR	Slew rate	vs Free-air temperature	26
	Pulse response	Small signal Large signal	27, 28 29, 30
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	31 32
V_n	Equivalent input noise voltage	vs Frequency	33
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	34 35
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	36 37 38
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF
INPUT OFFSET VOLTAGE

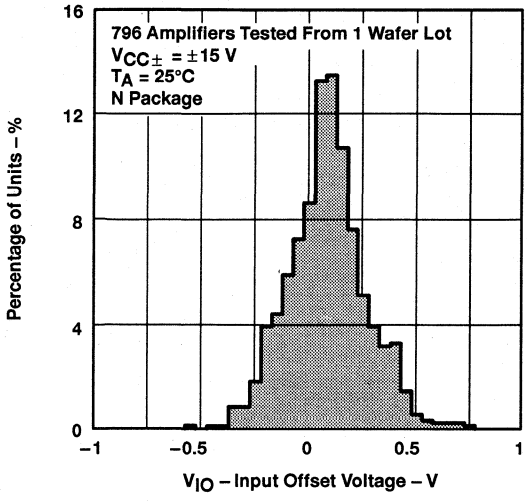


Figure 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

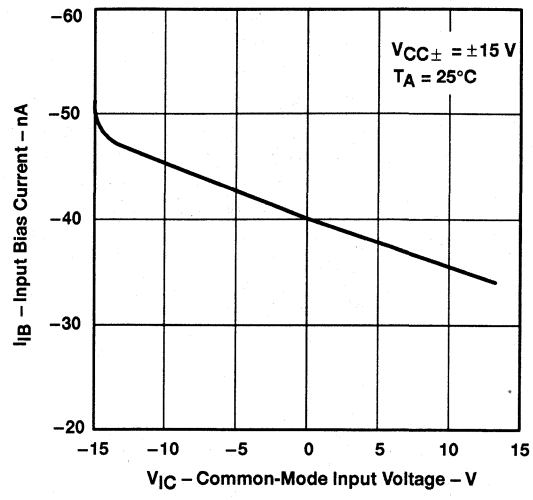


Figure 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

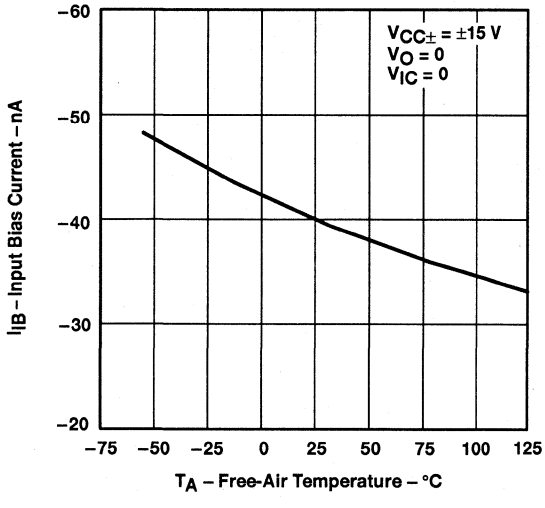


Figure 7

INPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

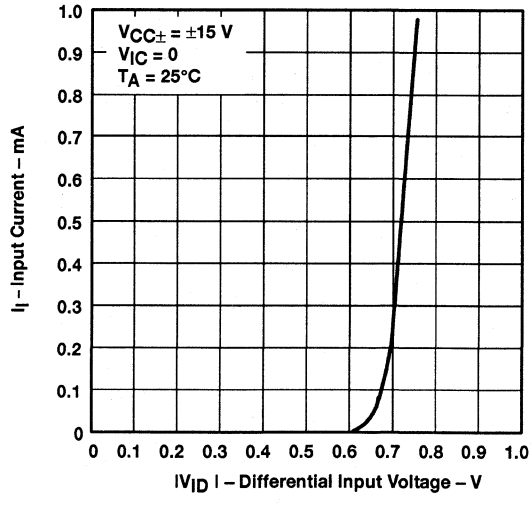


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

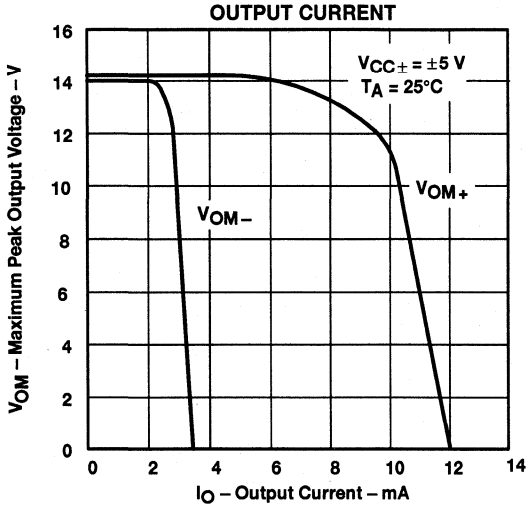


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

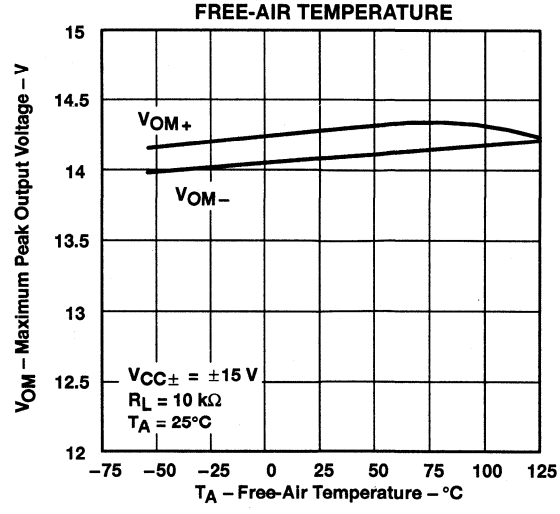


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

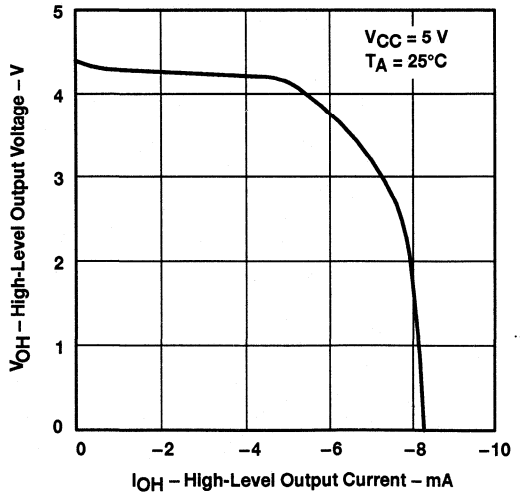


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

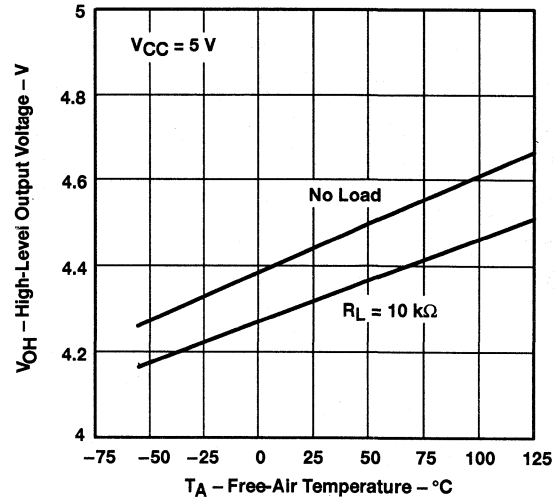


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

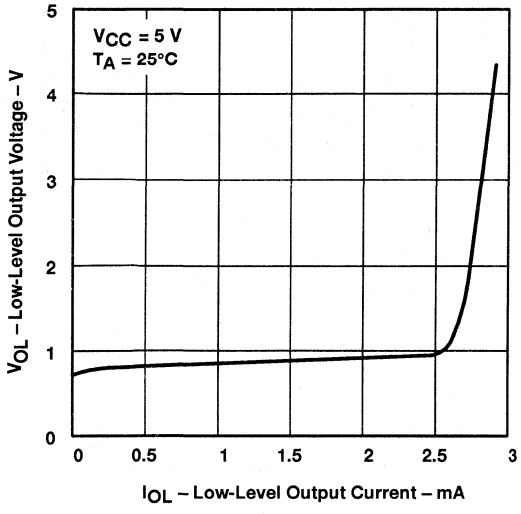


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

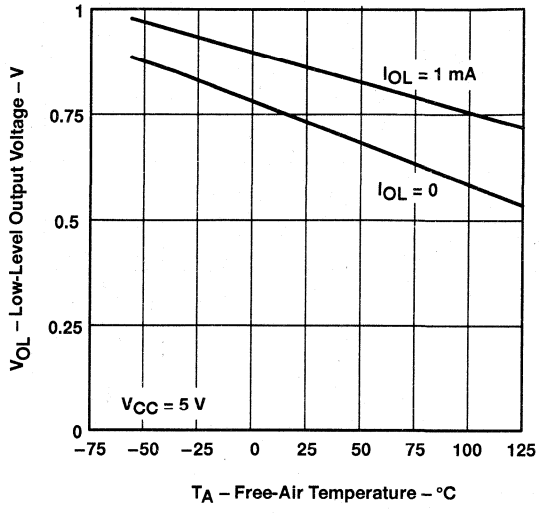


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

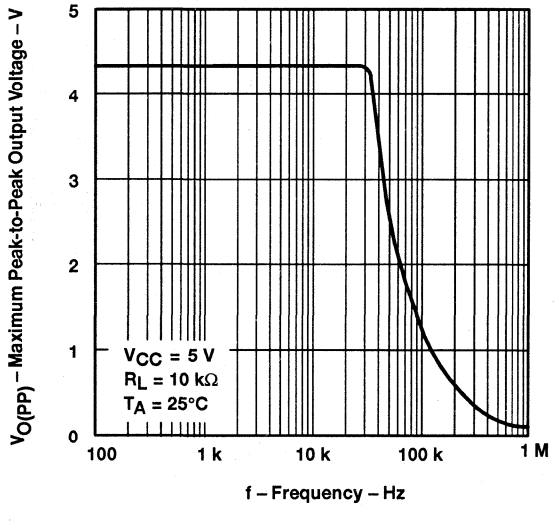


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

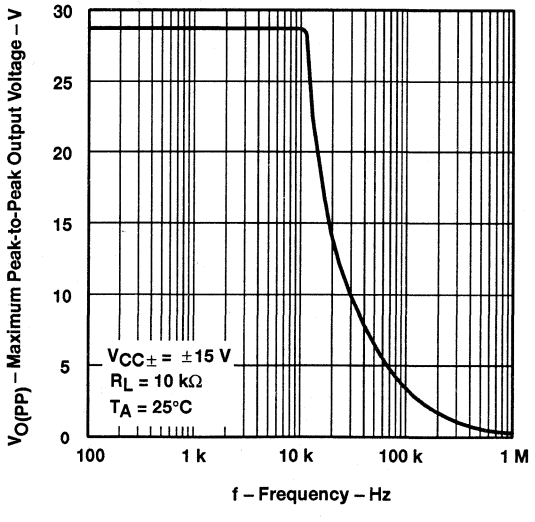


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

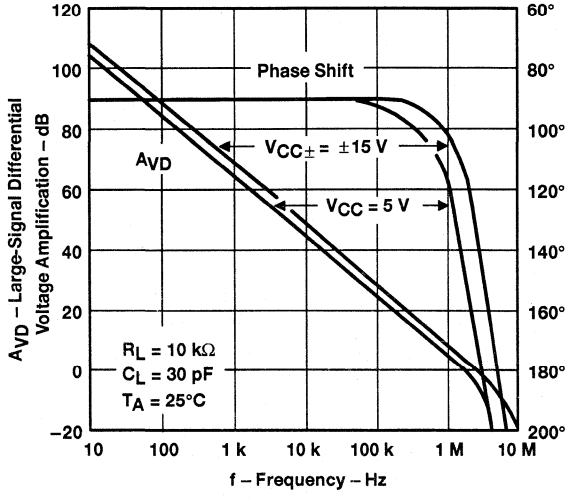


Figure 17

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

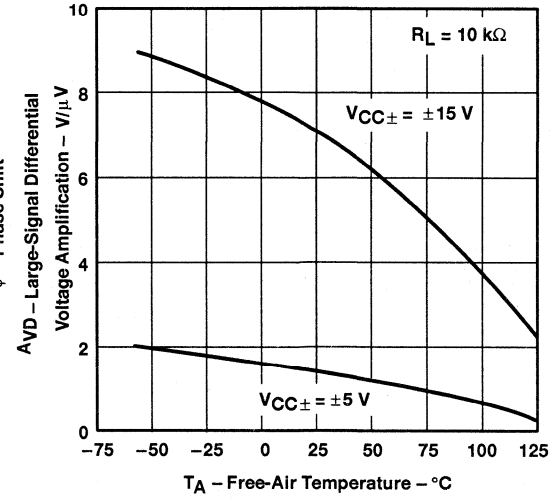


Figure 18

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

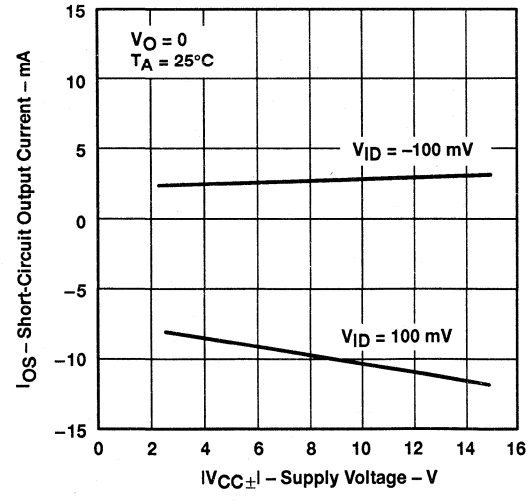


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

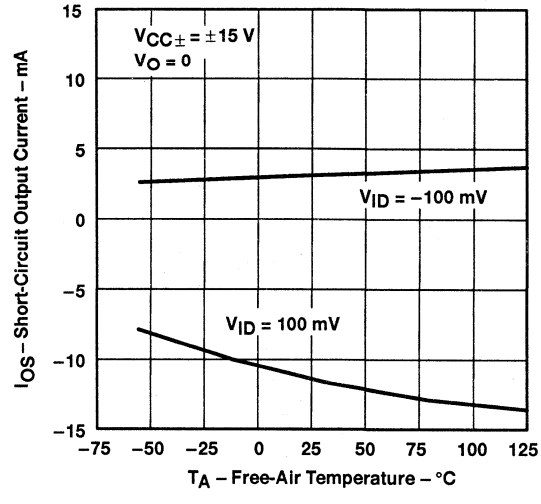


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

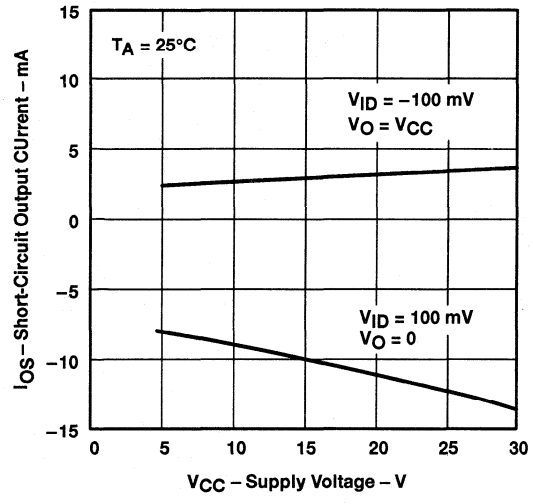


Figure 21

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

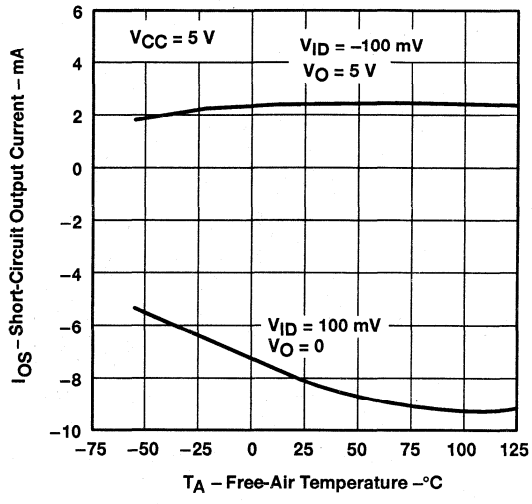


Figure 22

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

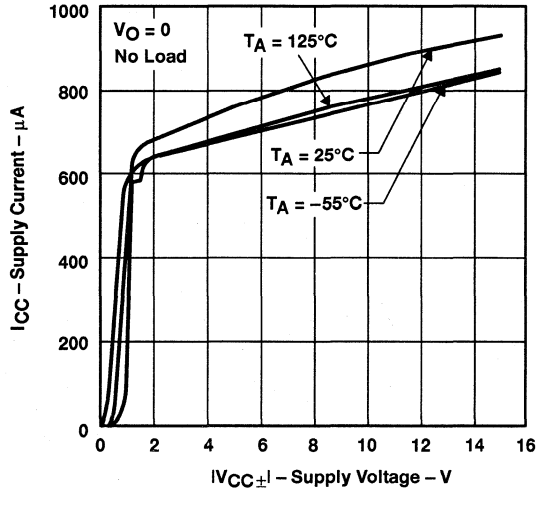


Figure 23

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

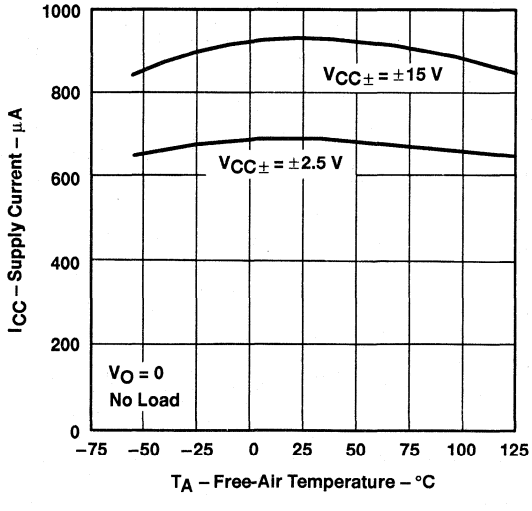


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

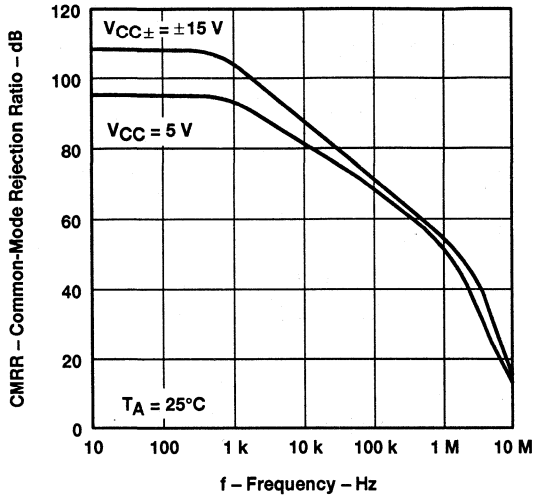


Figure 25

SLEW RATE vs FREE-AIR TEMPERATURE

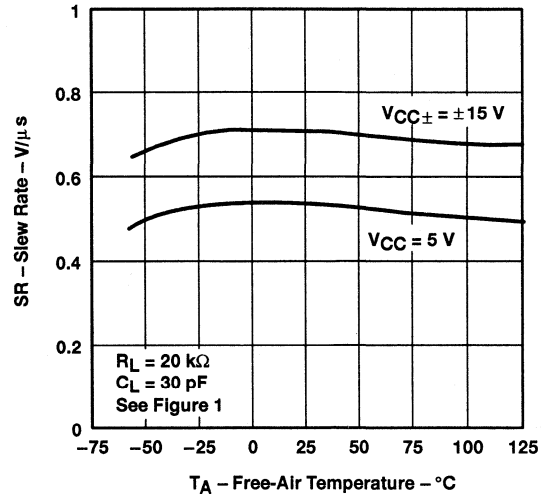


Figure 26

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

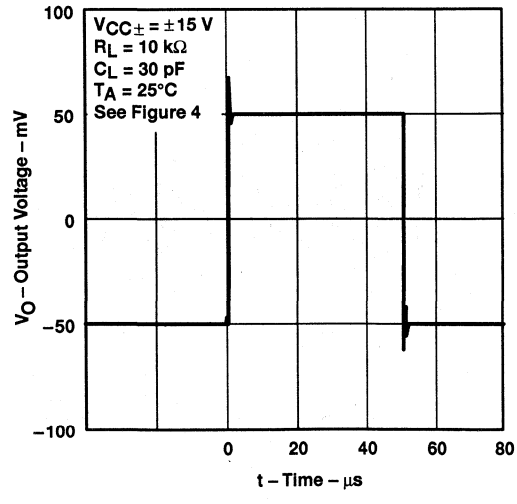


Figure 27

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

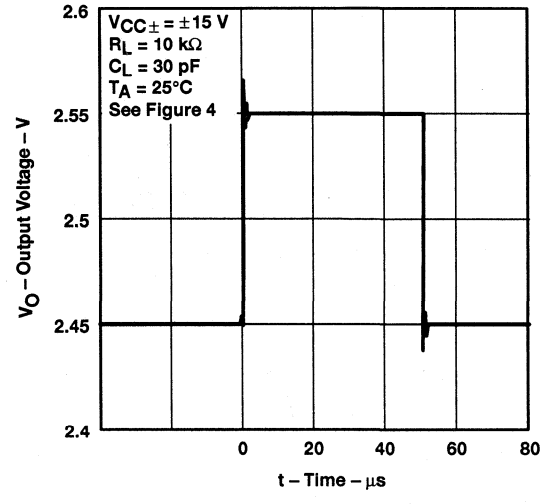


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

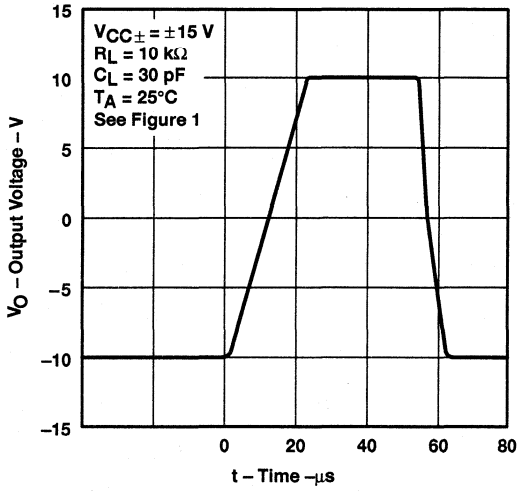


Figure 29

VOLTAGE-FOLLOWER
LARGE-SCALE
PULSE RESPONSE

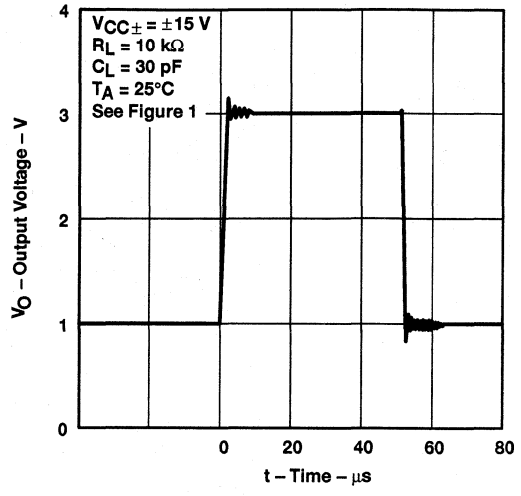


Figure 30

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

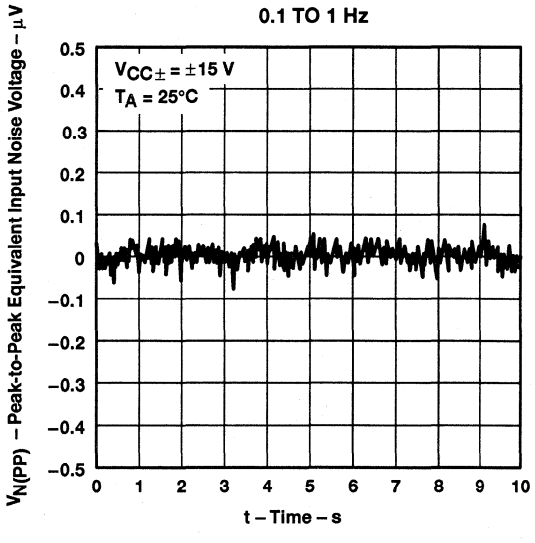


Figure 31

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

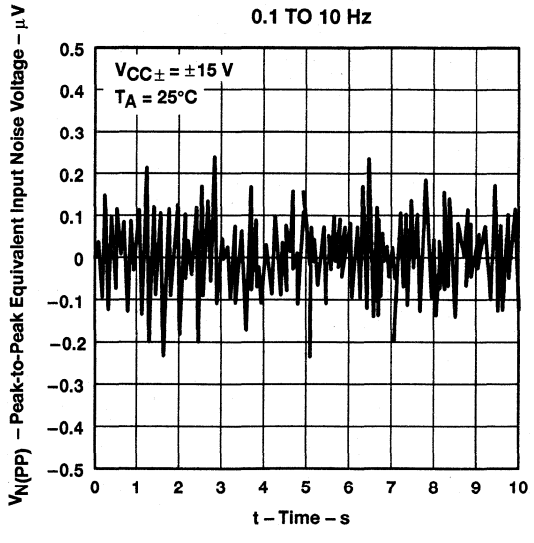


Figure 32

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

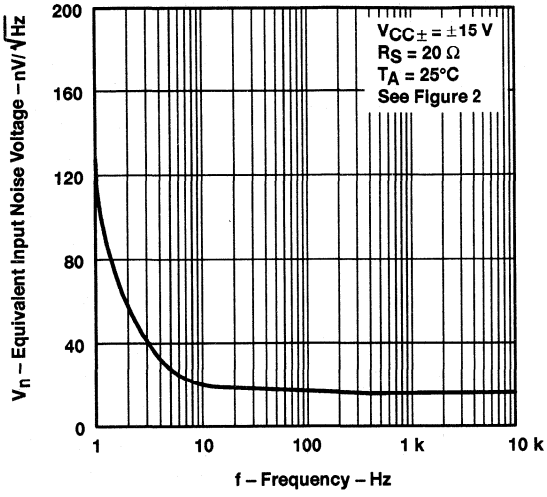


Figure 33

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

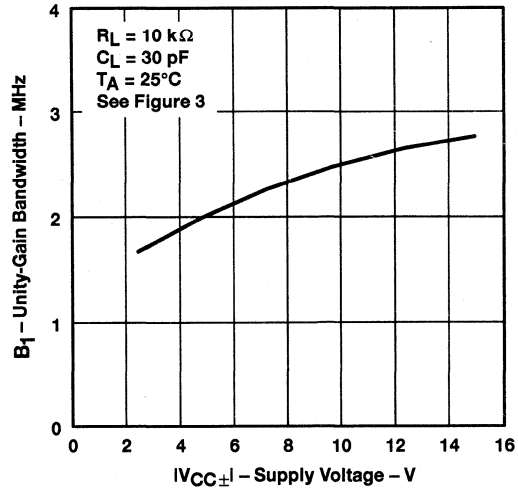


Figure 34

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

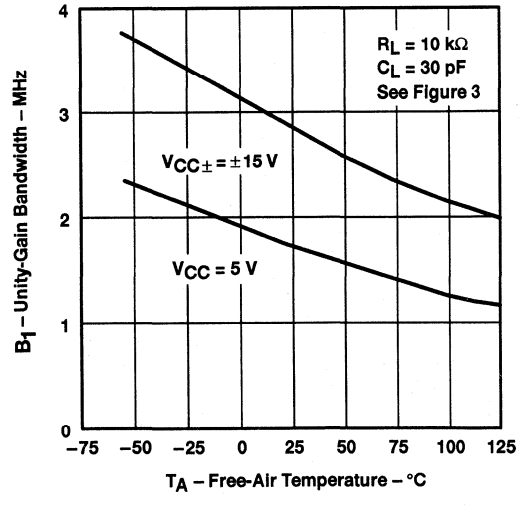


Figure 35

PHASE MARGIN vs SUPPLY VOLTAGE

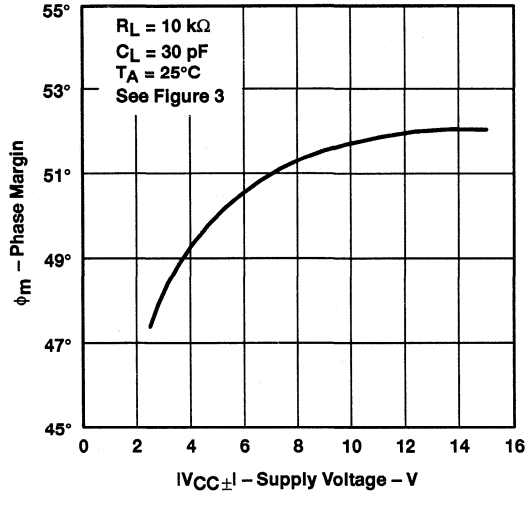


Figure 36

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

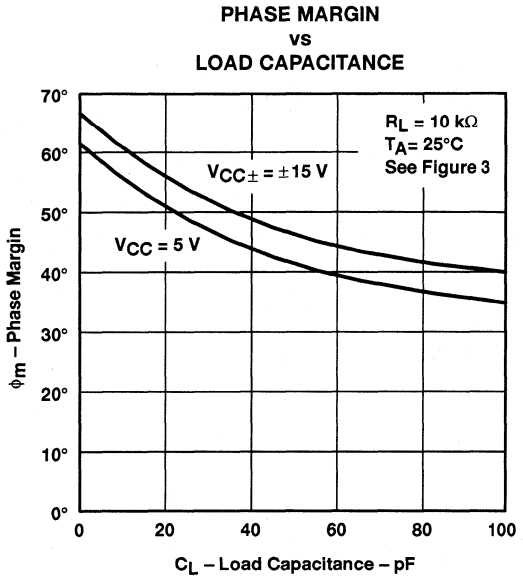


Figure 37

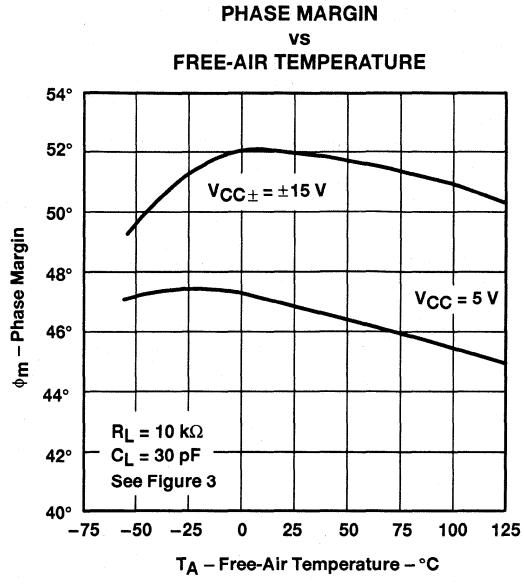


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

The TLE2024 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. This feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 39).

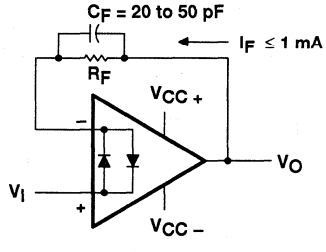


Figure 39. Voltage Follower

Input characteristics

The input of any unused amplifiers should be tied to ground to avoid possible oscillation.

- **Outstanding Combination of DC Precision and AC Performance:**
  - **Unity-Gain Bandwidth . . . 15 MHz Typ**
  - **V_n . . . . 3.3 nV/$\sqrt{Hz}$ at f = 10 Hz Typ, 2.5 nV/$\sqrt{Hz}$ at f = 1 kHz Typ**
  - **V_{IO} . . . . 25 μV Max**
  - **A_{VD} . . . 45 V/μV Typ With R_L = 2 kΩ, 19 V/μV Typ With R_L = 600 Ω**
- **Available in Standard-Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical Information**

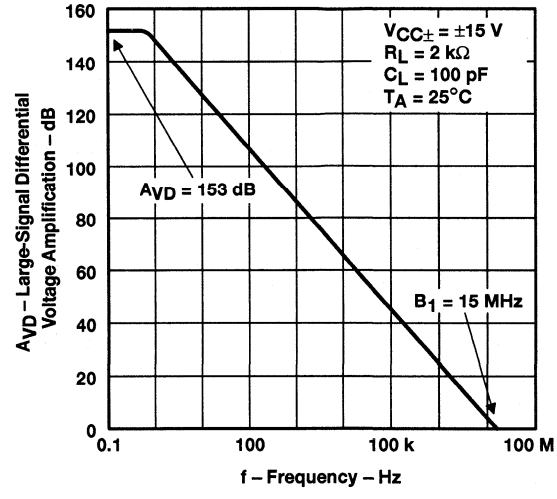
description

The TLE2027 and TLE2027A contain innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Manufactured using Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

In the area of dc precision, the TLE2027 and TLE2027A offer maximum offset voltages of 100 μV and 25 μV, respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/μV (typ).

The ac performance is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/$\sqrt{Hz}$ and 2.5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz and 1 kHz, respectively.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



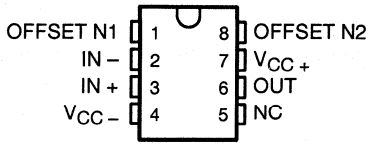
Both the TLE2027 and TLE2027A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 105°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

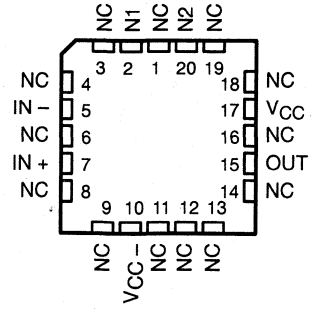
T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	25 μV	TLE2027ACD	—	—	TLE2027ACP
	100 μV	TLE2027CD	—	—	TLE2027CP
–40°C to 105°C	25 μV	TLE2027AID	—	—	TLE2027AIP
	100 μV	TLE2027ID	—	—	TLE2027IP
–55°C to 125°C	25 μV	TLE2027AMD	TLE2027AMFK	TLE2027AMJG	TLE2027AMP
	100 μV	TLE2027MD	TLE2027MFK	TLE2027MJG	TLE2027MP

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2027ACDR).

D, JG, OR P PACKAGE
(TOP VIEW)

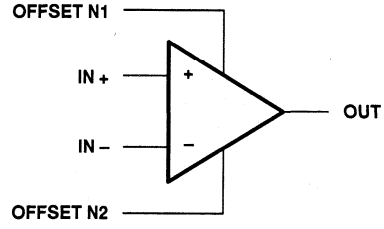


FK PACKAGE
(TOP VIEW)

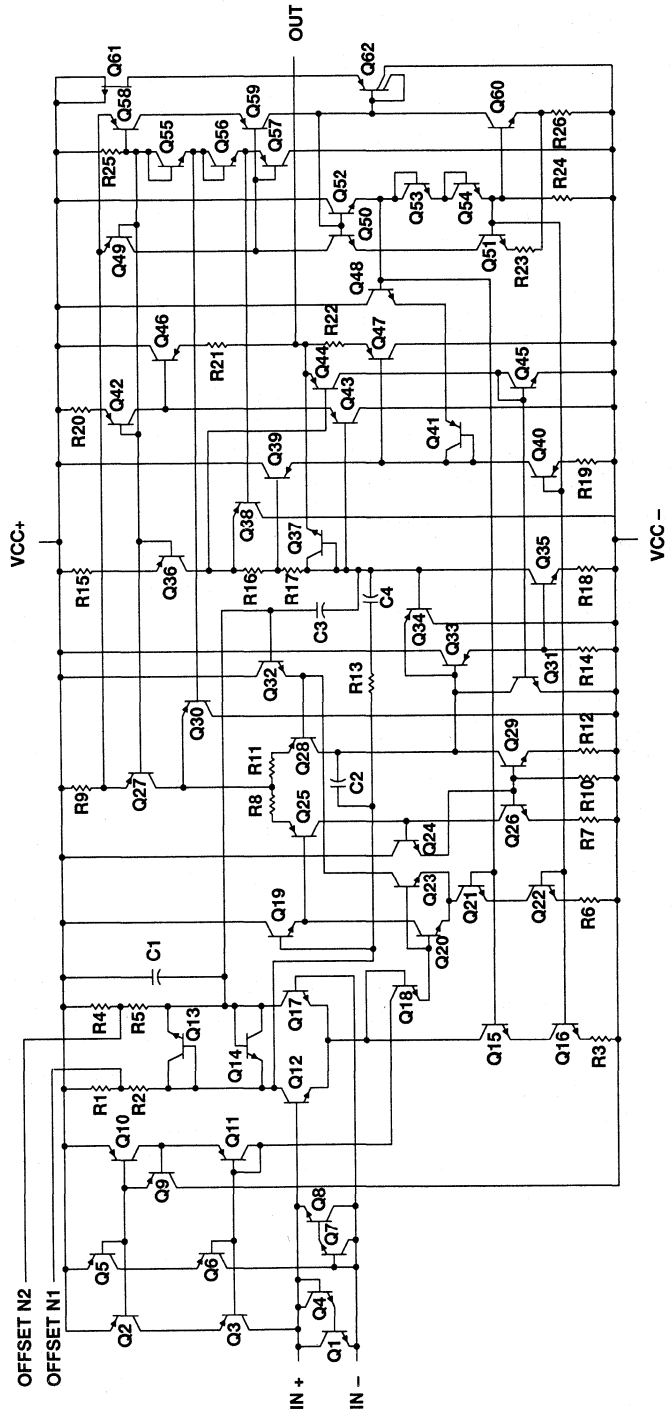


NC – No internal connection

symbol



equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 22 V
Supply voltage, V_{CC-} ..... – 22 V
Differential input voltage, V_{ID} (see Note 2) ..... ±1.2 V
Input voltage range, V_I (any input) ..... $V_{CC\pm}$
Input current, I_I (each Input) ..... ±1 mA
Output current, I_O ..... ± 50 mA
Total current into V_{CC+} ..... 50 mA
Total current out of V_{CC-} ..... 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... – 40°C to 105°C
M suffix ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and /or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±4	±22	±4	±22	±4	±22	V
Common-mode input voltage, V_{IC}	T_A = 25°C	–11	11	–11	11	–11	11	V
	T_A = Full range‡	–10.5	10.5	–10.4	10.4	–10.2	10.2	
Operating free-air temperature, T_A		0	70	–40	105	–55	125	°C

‡ Full range is 0°C to 70°C for C-suffix devices, –40°C to 105°C for I-suffix devices, and –55°C to 125°C for M-suffix devices.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027C			TLE2027AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			145			70	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.5 to 10.5			−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5			10.5			V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2			4			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.5			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			2			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	98			114			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	92			106			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.8	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027C			TLE2027AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/μs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	V_O = +10 V, A_{VD} = 5, See Note 5	25°C		<0.002%			<0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C	7	13		9	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C		55°			55°		

† Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027I			TLE2027AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			180			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.4 to 10.4			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5			10.5			V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2			3.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			1.1			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.9	

† Full range is – 40°C to 105°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027I			TLE2027AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/μs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	V_O = +10 V, A_{VD} = 1, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C	7	13		9	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C		55°			55°		

† Full range is – 40°C to 105°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2027M			TLE2027AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			200			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1*		0.2	1*	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1*		0.006	1*	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.3 to 10.3			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5			10.5			V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12			12			
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2.5			3.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			5	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2027M			TLE2027AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	1.7	2.8		1.7	2.8		V/μs
			Full range	1			1			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8*		3.3	4.5*	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5*		2.5	3.8*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250*		50	130*	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4*		1.5	4*	pA/√Hz
		f = 1 kHz			0.4	0.6*		0.4	0.6*	
THD	Total harmonic distortion	V_O = +10 V, A_{VD} = 1, See Note 5	25°C		< 0.002%			< 0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C	7*	13		9*	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF	25°C		55°			55°		

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION

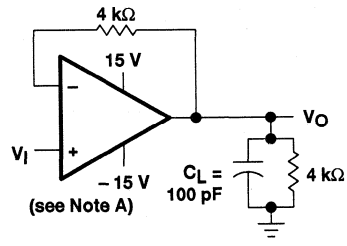


Figure 1. Slew-Rate Test Circuit

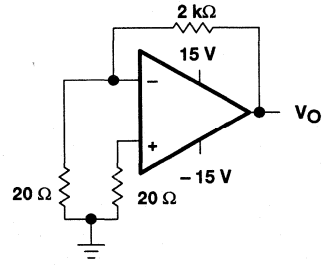


Figure 2. Noise-Voltage Test Circuit

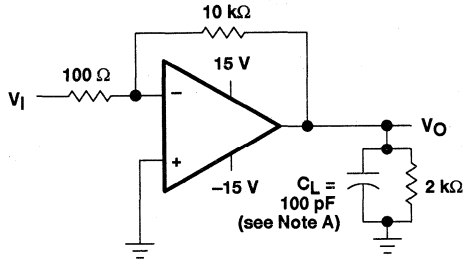


Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

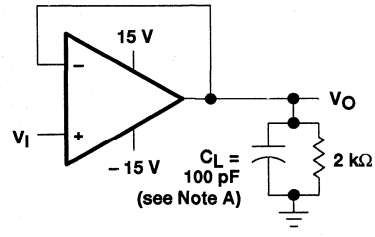


Figure 4. Small-Signal Pulse-Response Test Circuit

NOTE A: C_L includes fixture capacitance.

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

initial estimates of parameter distributions

In the ongoing program of improving data sheets and supplying more information to our customer, Texas Instruments has added an estimate of not only the typical values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from our characterization of the initial wafer lots of this new device type (see Figure 5). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ± 3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 5, there were a total of 835 units from 2 wafer lots. In this case, there is a good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This will always be the case on newly released products since there will only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. While 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

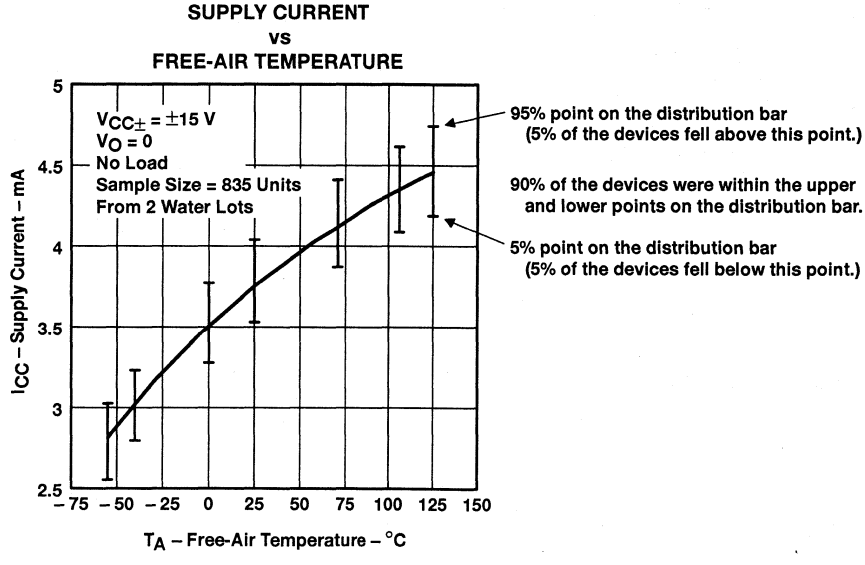


Figure 5. Sample Graph With Distribution Bars

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
ΔV_{IO}	Input offset voltage change	vs Time after power on	7, 8
I_{IO}	Input offset current	vs Free-air temperature	9
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	10 11
I_I	Input current	vs Differential input voltage	12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13
V_{OM}	Maximum peak output voltage	vs Load resistance vs Free-air temperature	14, 15 16, 17
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	18 19 20, 21 22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24
k_{SVR}	Supply voltage rejection ratio	vs Frequency	25
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	26, 27 28, 29 30, 31
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	32 33
	Pulse response	Small signal Large signal	34 35
V_n	Equivalent input noise voltage	vs Frequency	36
	Noise voltage (referred to input)	0.1 to 10 Hz	37
B_1	Unity-gain-bandwidth	vs Supply voltage vs Load capacitance	38 39
SR	Slew rate	vs Free-air temperature	40
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	41 42 43
	Phase shift	vs Frequency	19, 21

TYPICAL CHARACTERISTICS†

TLE2027
DISTRIBUTION
INPUT OFFSET VOLTAGE

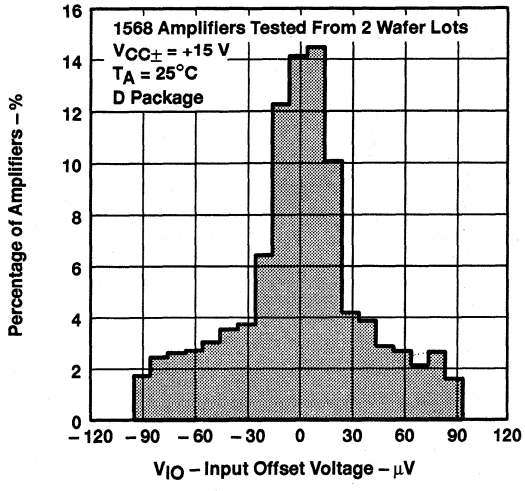


Figure 6

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

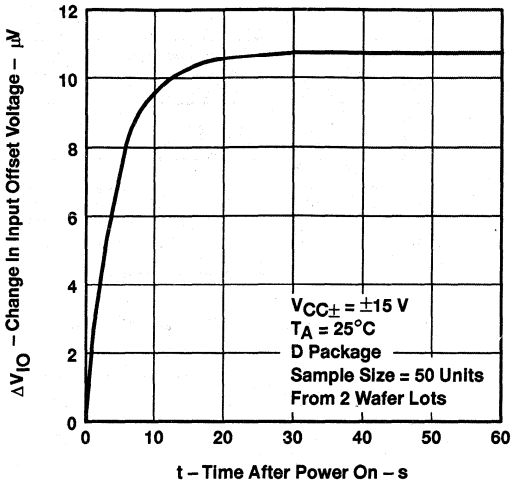


Figure 7

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

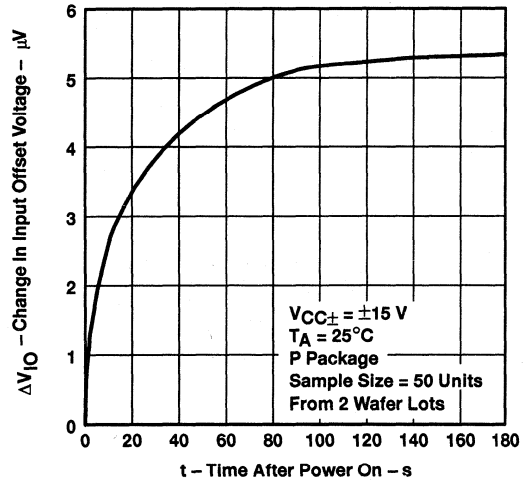


Figure 8

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

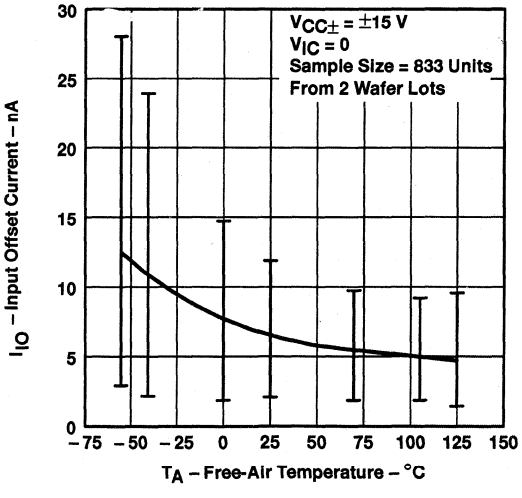


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

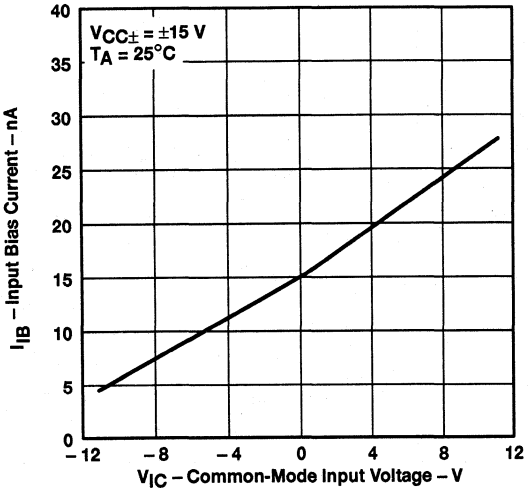


Figure 10

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

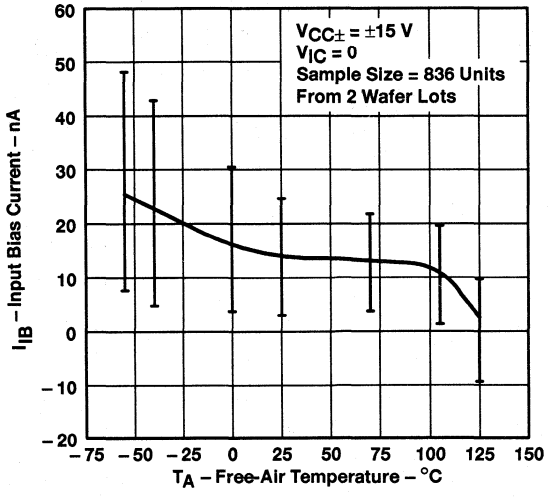


Figure 11

INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

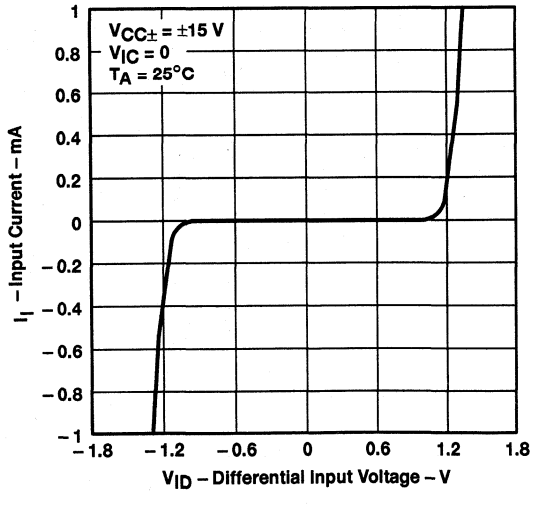


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

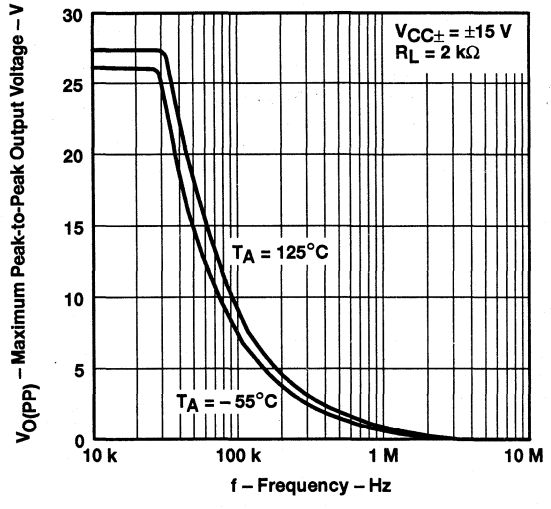


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

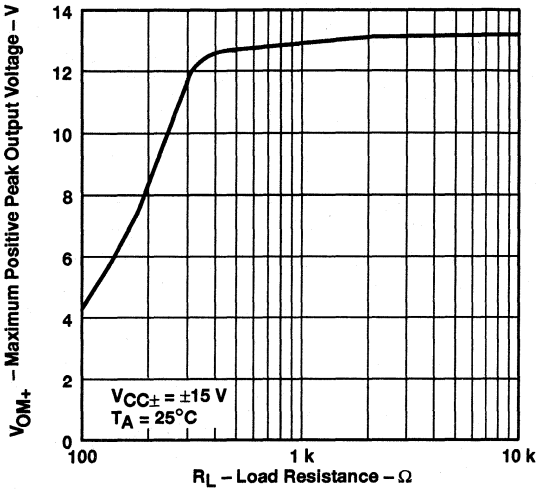


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

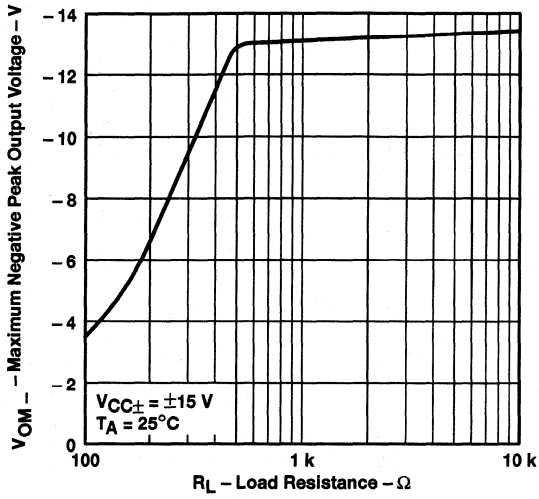


Figure 15

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

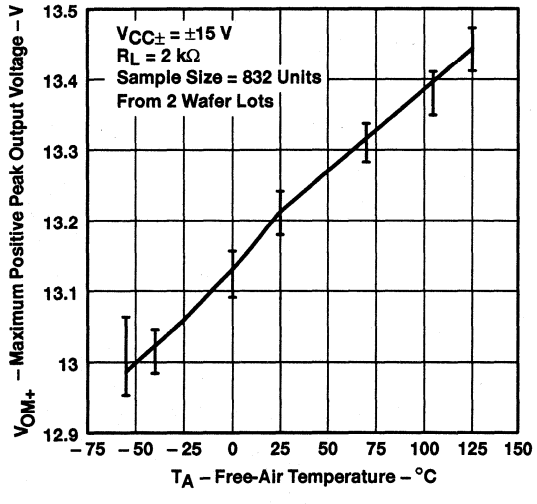


Figure 16

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

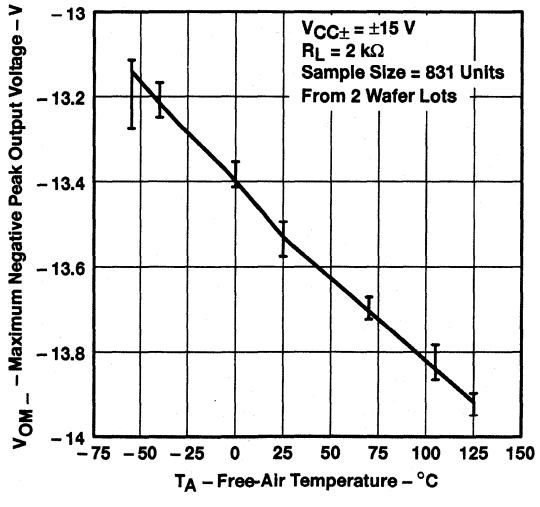


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

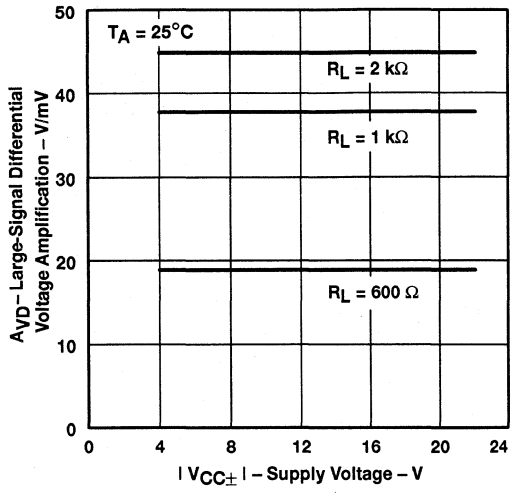


Figure 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

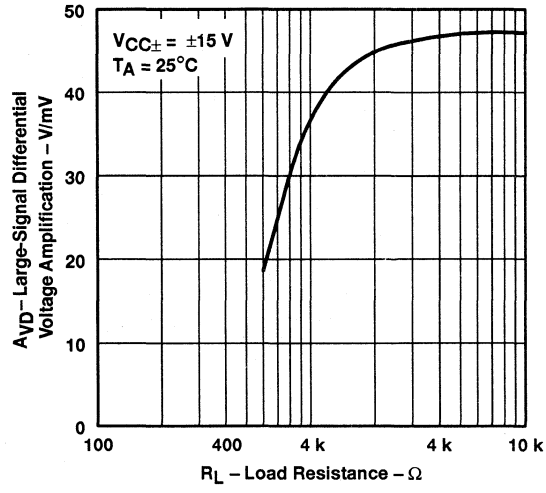


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

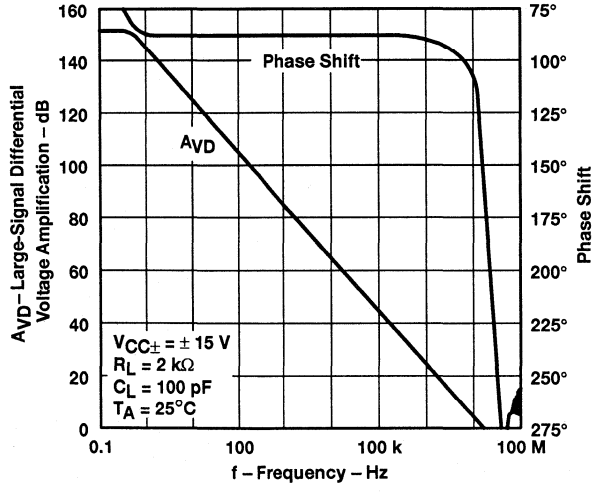


Figure 20

TYPICAL CHARACTERISTICS†

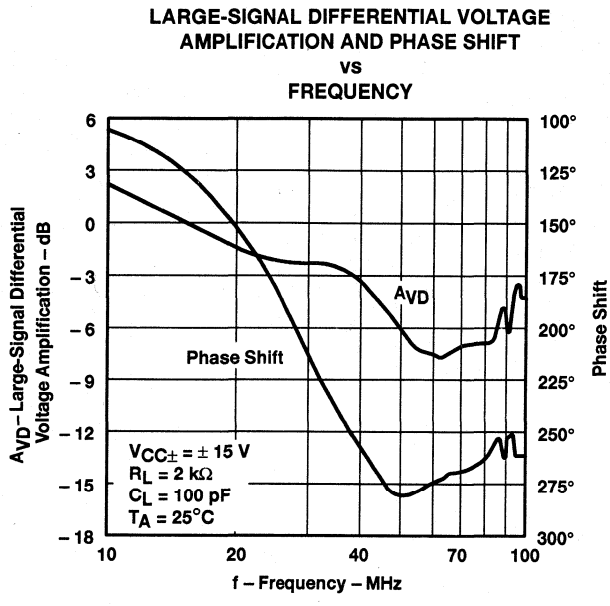


Figure 21

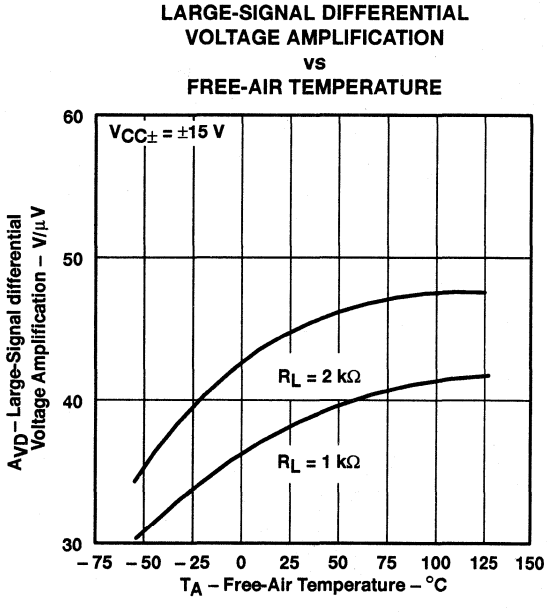


Figure 22

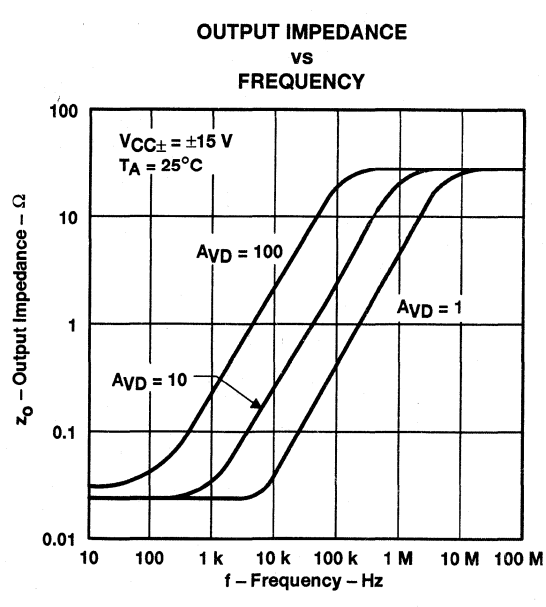


Figure 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

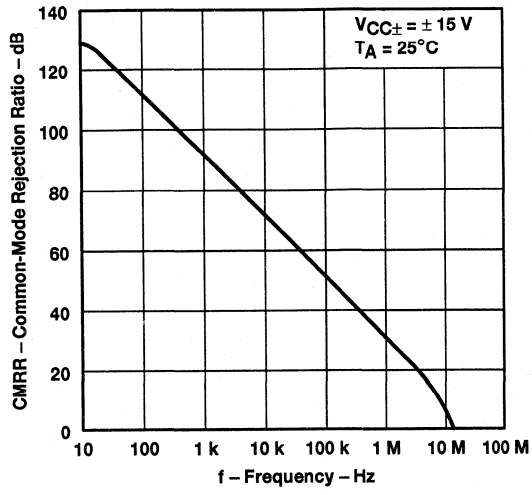


Figure 24

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

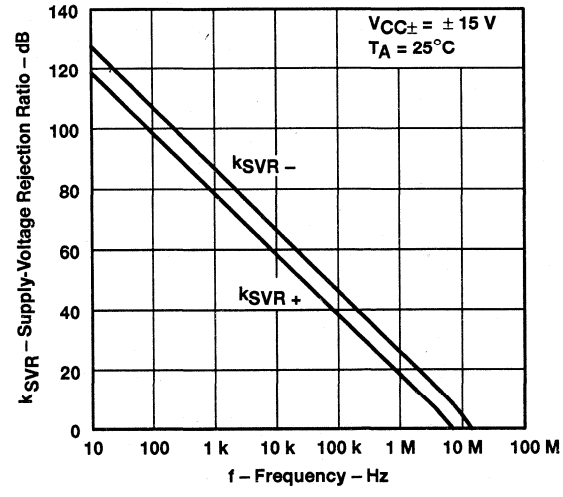


Figure 25

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

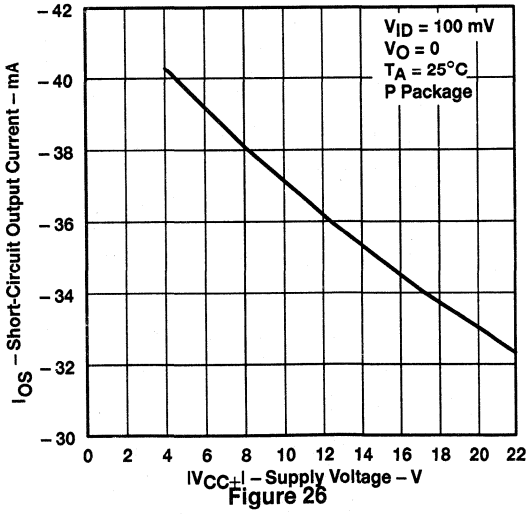


Figure 26

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

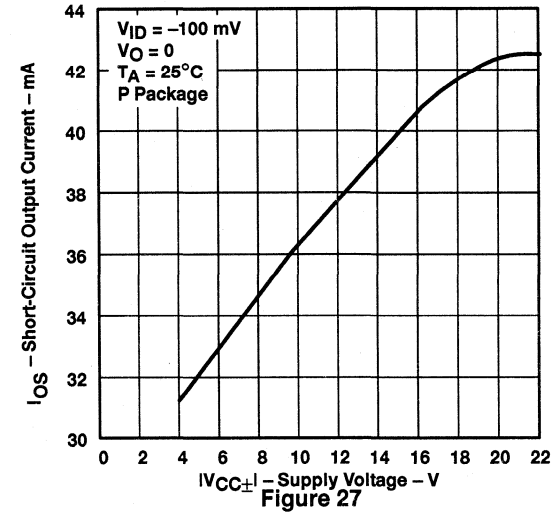


Figure 27

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

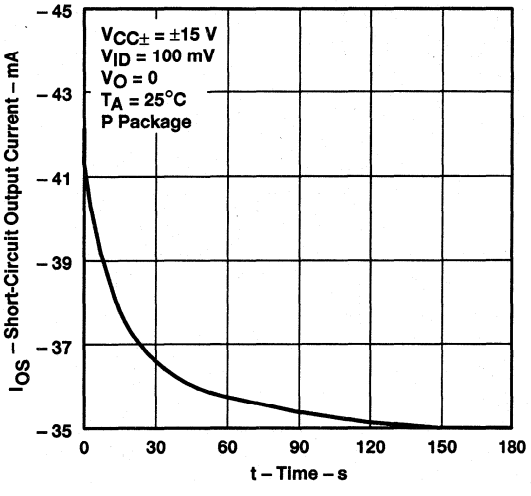


Figure 28

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

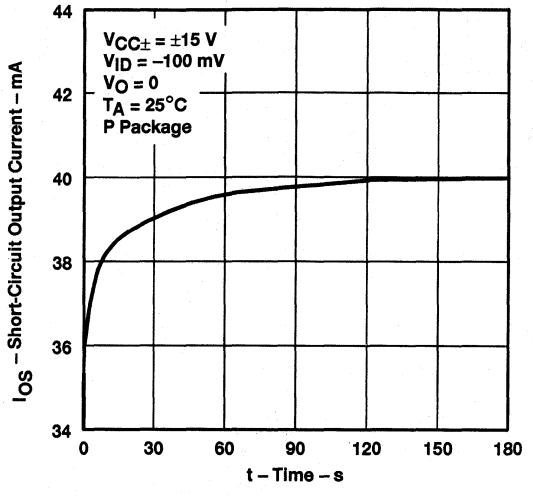


Figure 29

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

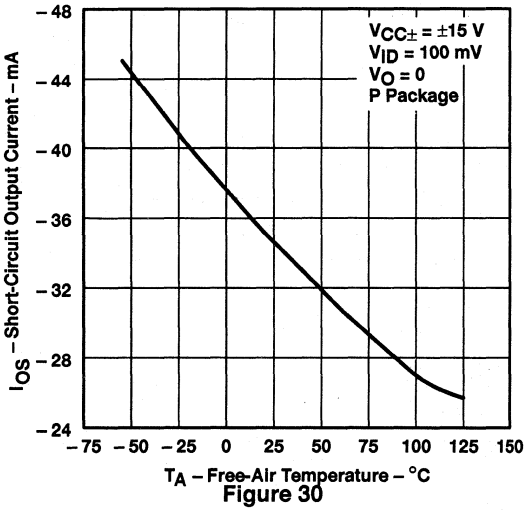


Figure 30

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

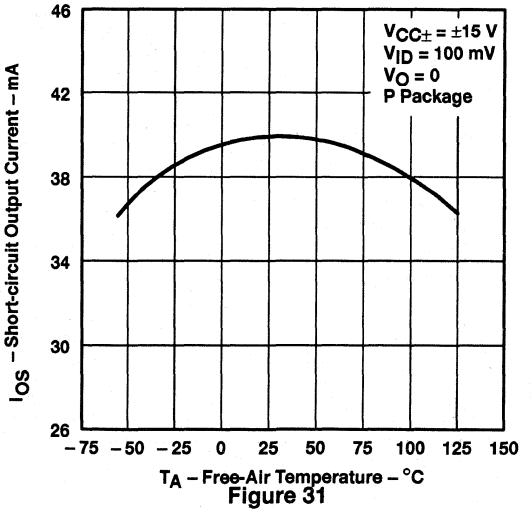


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

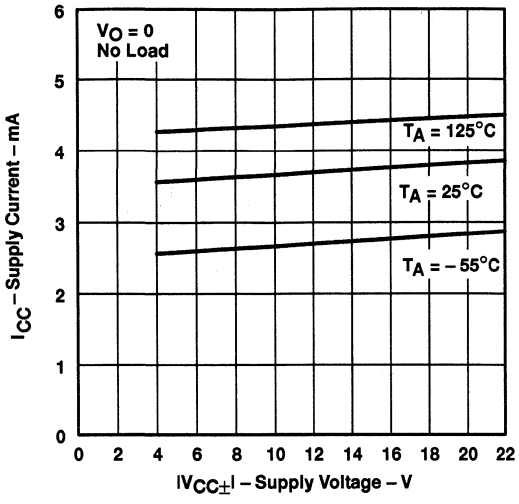


Figure 32

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

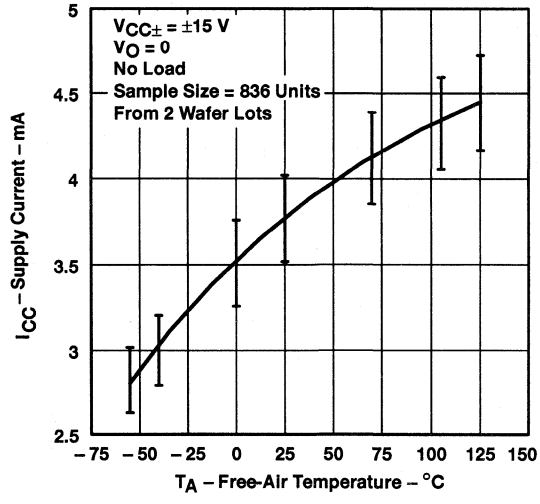


Figure 33

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

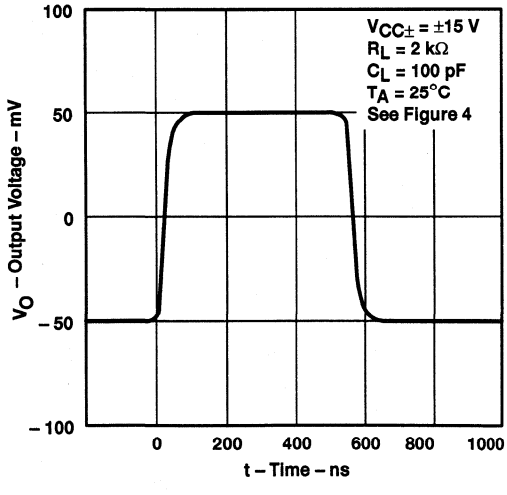


Figure 34

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

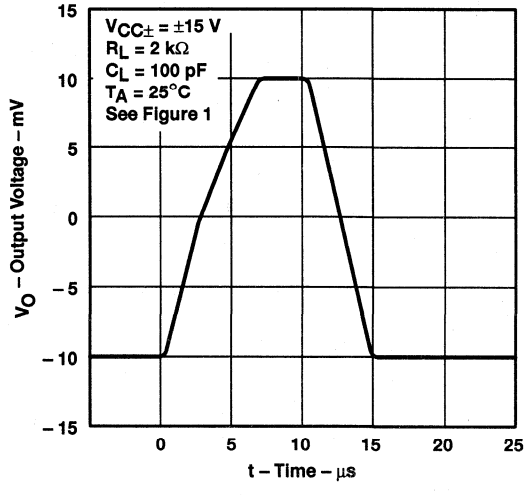


Figure 35

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

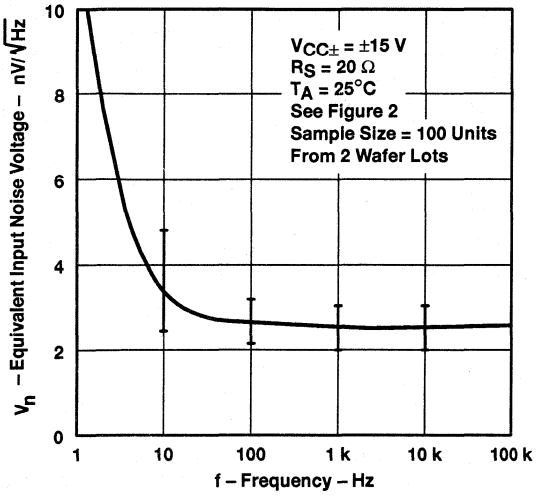


Figure 36

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

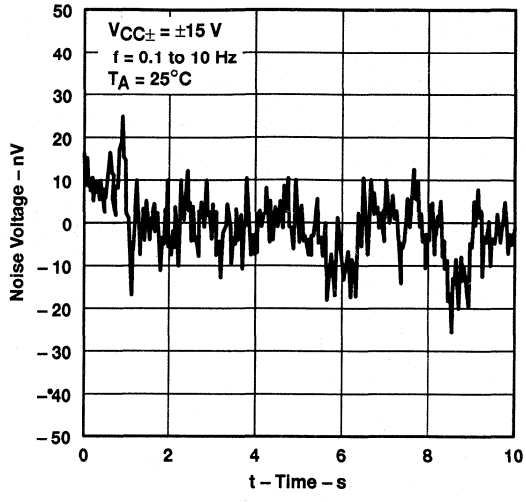


Figure 37

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

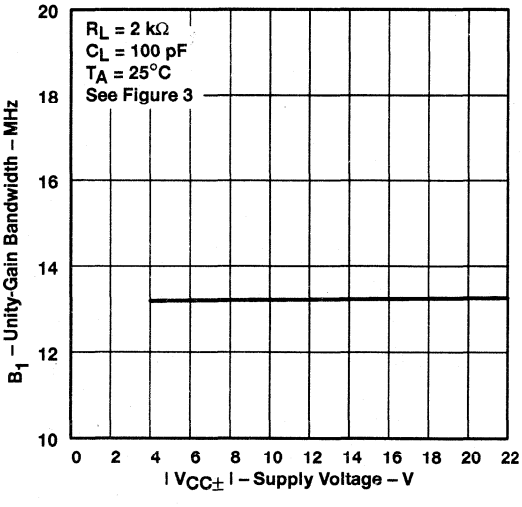


Figure 38

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

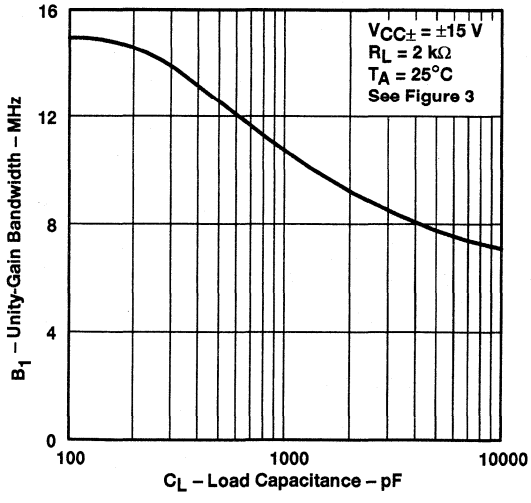


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

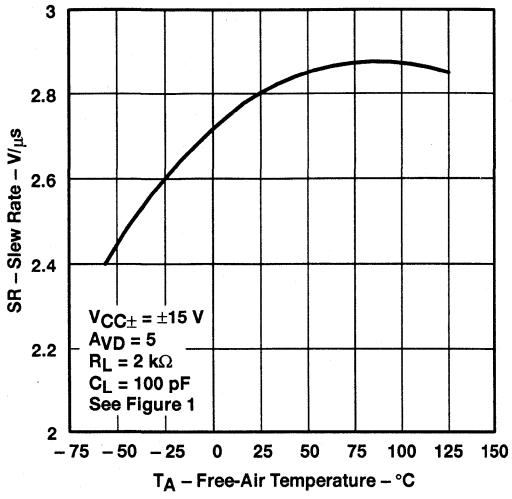


Figure 40

PHASE MARGIN
vs
SUPPLY VOLTAGE

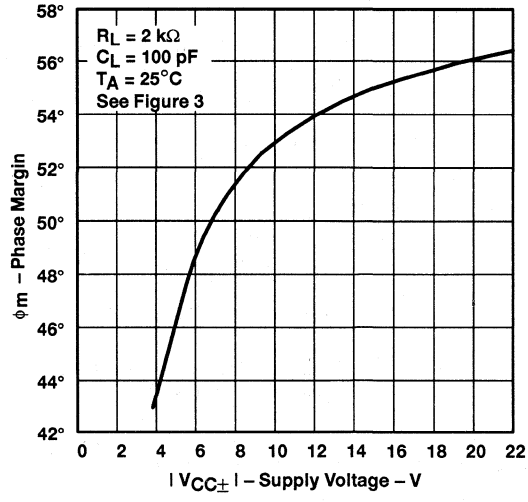


Figure 41

PHASE MARGIN
vs
LOAD CAPACITANCE

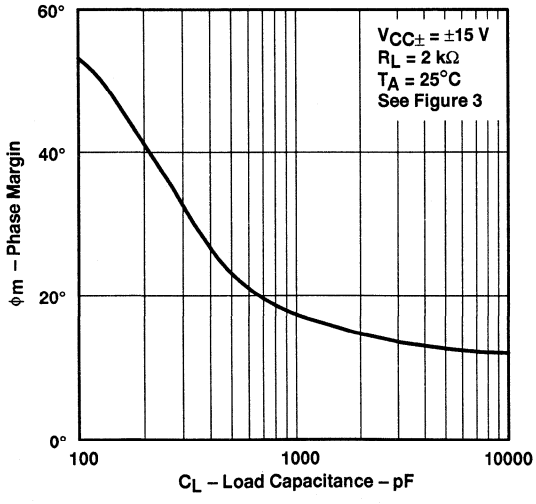


Figure 42

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

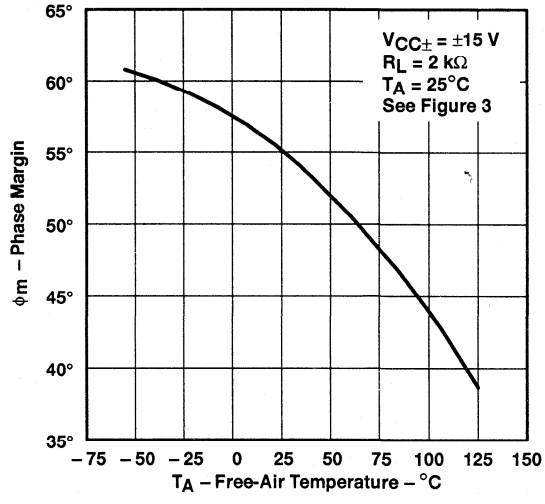


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 44 and 45 were generated using the TLE2027 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

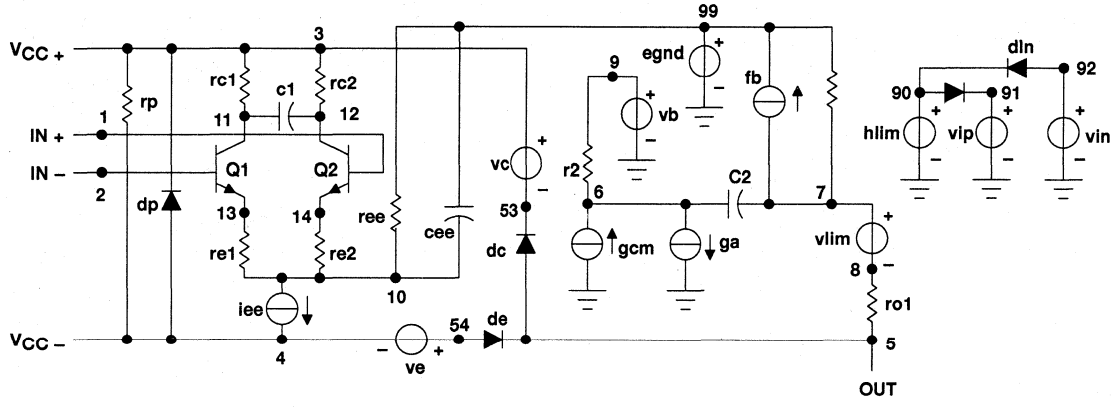


Figure 44. Boyle Macromodel

PSpice and *Parts* are trademarks of MicroSim Corporation.

APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2027 1 2 3 4 5
*
  c1      11   12   4.003E-12
  c2       6    7   20.00E-12
  dc       5   53   dz
  de      54    5   dz
  dlp     90   91   dz
  dln     92   90   dx
  dp       4    3   dz
  egnd    99    0   poly(2) (3,0) (4,0) 0 5 .5
  fb       7   99   poly(5) vb vc ve vlp vln 0 954.8E6 -1E9 1E9 1E9 -1E9
  ga       6    0   11  12   2.062E-3
  gcm      0    6   10  99   531.3E-12
  iee     10    4   dc  56.01E-6
  hlim    90    0   vlim 1K
  q1      11    2   13 qx
  q2      12    1   14 qx
  r2       6    9   100.0E3
  rc1      3   11   530.5
  rc2      3   12   530.5
  re1     13   10   -393.2
  re2     14   10   -393.2
  ree     10   99   3.571E6
  ro1      8    5   25
  ro2      7   99   25
  rp       3    4   8.013E3
  vb       9    0   dc  0
  vc       3   53   dc  2.400
  ve      54    4   dc  2.100
  vlim     7    8   dc  0
  vlp     91    0   dc  40
  vln      0   92   dc  40
.modeldx D(Is=800.0E-18)
.modelqx NPN(Is=800.0E-18 Bf=7.000E3)
.ends
```

Figure 45. Macromodel Subcircuit

APPLICATION INFORMATION

voltage-follower applications

The TLE2027 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 46).

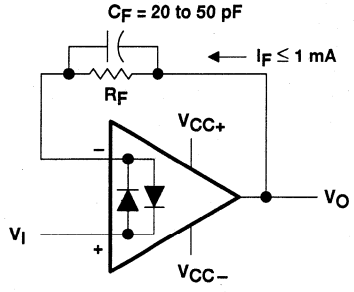
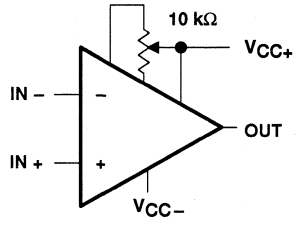


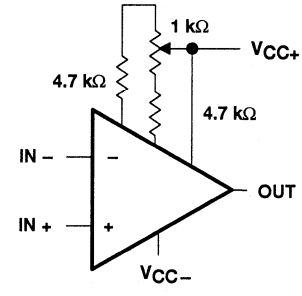
Figure 46. Voltage Follower

Input offset voltage nulling

The TLE2027 series offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 47 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.



(a) STANDARD ADJUSTMENT



(b) ADJUSTMENT WITH IMPROVED SENSITIVITY

Figure 47. Input Offset Voltage Nulling Circuits

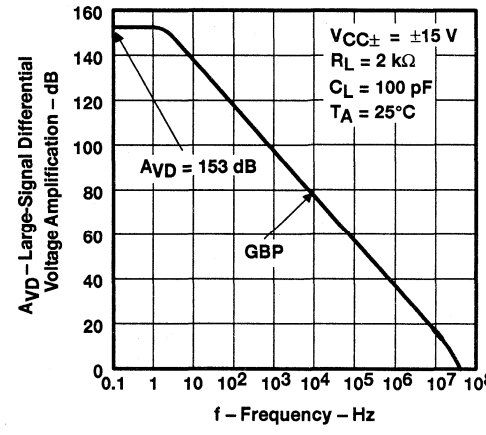
- **Outstanding Combination of DC Precision and AC Performance:**
  - **Gain-Bandwidth Product . . . 50 MHz Typ**
  - **V_n . . . 3.3 nV/√Hz at f = 10 Hz Typ, 2.5 nV/√Hz at f = 1 kHz Typ**
  - **V_{IO} . . . 25 μV Max at T_A = 25°C**
  - **A_{VD} . . . 45 V/μV Typ With R_L = 2 kΩ, 19 V/μV Typ With R_L = 600 Ω**
- **Available in Standard-Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical information Included**

description

The TLE2037 and TLE2037A combine innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Using the Texas Instruments state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

The TLE2037 and TLE2037A are decompensated versions of the TLE2027 and TLE2027A and are stable to a close-loop gain of 5. In the area of dc precision, these parts offer maximum offset voltages of 100 μV and 25 μV, respectively, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/μV (typ).

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



The ac performance is highlighted by a typical gain-bandwidth product specification of 50 MHz, 50° of phase margin, and noise voltage specifications of 3.3 nV/√Hz and 2.5 nV/√Hz at frequencies of 10 Hz and 1 kHz, respectively.

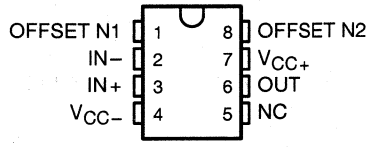
Both the TLE2037 and TLE2037A are available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 105°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

AVAILABLE OPTIONS

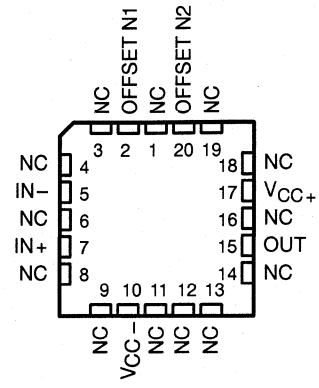
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	25 μV	TLE2037ACD	–	–	TLE2037ACP	TLE2037Y
	100 μV	TLE2037CD			TLE2037CP	–
–40°C to 105°C	25 μV	TLE2037AID	–	–	TLE2037AIP	–
	100 μV	TLE2037ID			TLE2037IP	
–55°C to 125°C	25 μV	TLE2037AMD	TLE2037AMFK	TLE2037AMJG	TLE2037AMP	–
	100 μV	TLE2037MD	TLE2037MFK	TLE2037MJG	TLE2037MP	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2037ACDR). Chips are tested at 25°C.

D, JG, OR P PACKAGE
(TOP VIEW)

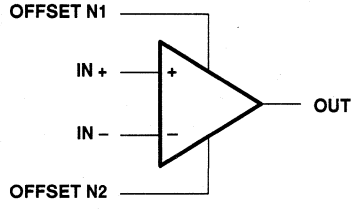


FK PACKAGE
(TOP VIEW)



NC – No internal connection

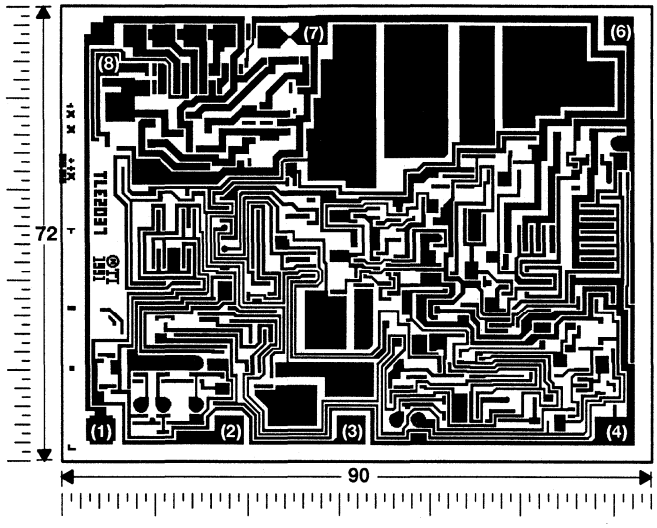
symbol

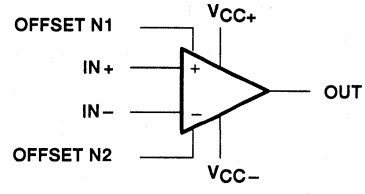


TLE2037 chip information

This chip, when properly assembled, displays characteristics similar to the TLE2037C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

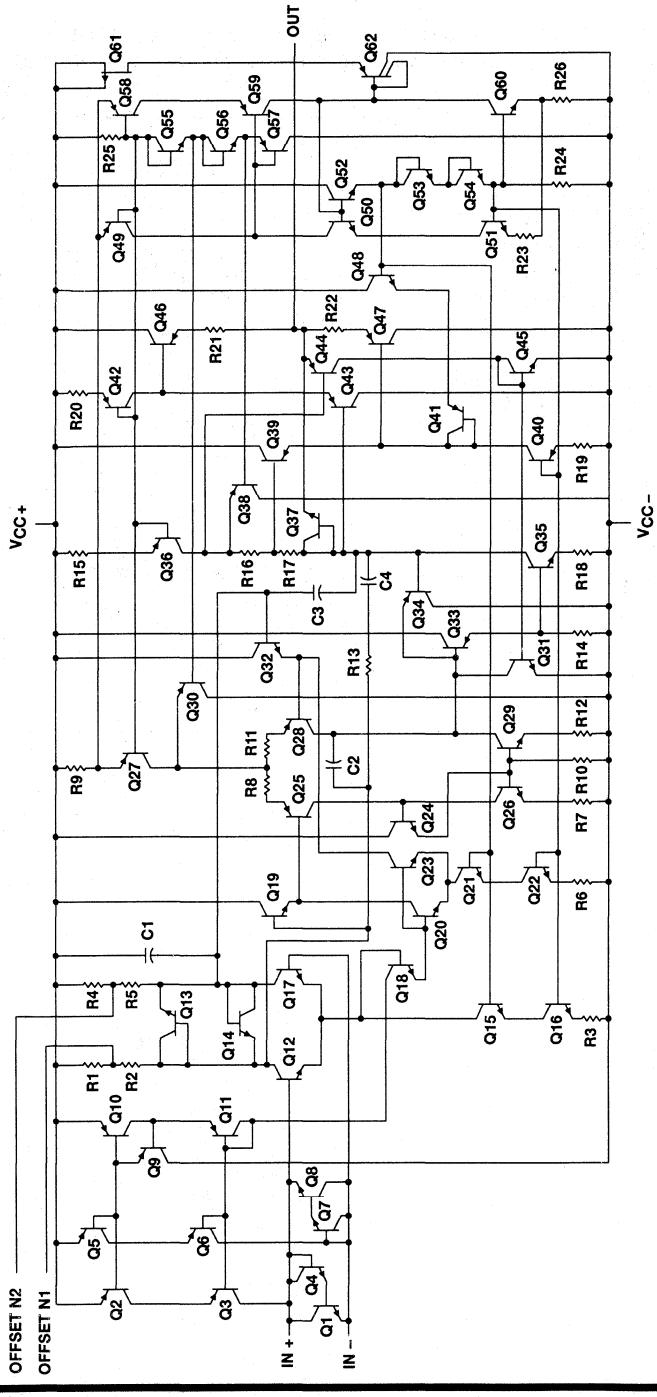
T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT	
Transistors	61
Resistors	26
Capacitors	4
epi FET	1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} ..... –19 V
Differential input voltage, V_{ID} (see Note 2) ..... ±1.2 V
Input voltage range, V_I (any input) ..... $\pm V_{CC}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ± 50 mA
Total current into V_{CC+} ..... 50 mA
Total current out of V_{CC-} ..... 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... –40°C to 105°C
M suffix ..... –55°C to 125°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current will flow if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	7.6 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±4	±19	±4	±19	±4	±19	V
Common-mode input voltage, V_{IC}	T_A = 25°C	–11	11	–11	11	–11	11	V
	T_A = Full range†	–10.5	10.5	–10.4	10.4	–10.2	10.2	
Operating free-air temperature, T_A		0	70	–40	105	–55	125	°C

† Full range is 0°C to 70°C for C-suffix devices, –40°C to 105°C for the I-suffix devices, and –55°C to 125°C for the M-suffix devices.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037C			TLE2037AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	µV
			Full range			145			70	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.5 to 10.5			−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	11			11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/µV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2			4			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1			2.5			
		V_O = ±10 V, R_L = 600 kΩ	25°C	2	19		5	19		
			Full range	0.5			2			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	98			114			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	92			106			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.8	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037C			TLE2037AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	6	7.5		6	7.5		V/μs
			Full range	5			5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 5, See Note 5	25°C		< 0.002%			< 0.002%		
	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	35	50		35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		50°			50°		

† Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037I			TLE2037AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	µV
			Full range			180			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1		0.2	1	µV/°C
	Input bias voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	µV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.4 to 10.4			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/µV
		V_O = ±10 V R_L = 2 kΩ	Full range	2.5			3.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
			Full range	0.5			1.1			
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			4.9	

† Full range is −40°C to 105°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037I			TLE2037AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	6	7.5		6	7.5		V/μs
			Full range	4.7			4.7			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8		3.3	4.5	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5		2.5	3.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250		50	130	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6		0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 5, See Note 5	25°C		< 0.002%			< 0.002%		
	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	35	50		35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		50°			50°		

† Full range is −40°C to 105°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2037M			TLE2037AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100		10	25	μV
			Full range			200			105	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.4	1*		0.2	1*	μV/°C
	Input bias voltage long-term drift (see Note 4)		25°C		0.006	1		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		6	90		6	90	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		15	90		15	90	nA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		−11 to 11	−13 to 13		V
			Full range	−10.3 to 10.3			−10.4 to 10.4			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		10.5	12.9		V
			Full range	10			10			
		R_L = 2 kΩ	25°C	12	13.2		12	13.2		
			Full range	11			11			
		R_L = 1 kΩ	−55°C	10			10			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	−10.5	−13		−10.5	−13		V
			Full range	−10			−10			
		R_L = 2 kΩ	25°C	−12	−13.5		−12	−13.5		
			Full range	−11			−11			
		R_L = 1 kΩ	−55°C	−10			−10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		10	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2.5			3.5			
		V_O = ±10 V R_L = 1 kΩ	25°C	3.5	38		8	38		
			Full range	1.8			2.2			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		5	19		
c_i	Input capacitance		25°C		8			8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		117	131		dB
			Full range	96			113			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		110	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			105			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3		3.8	4.7	mA
			Full range			5.6			5	

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is − 55°C to 125°C.
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2037M			TLE2037AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, R_L = 2 kΩ, C_L = 100 pF, See Figure 1	25°C	6*	7.5		6*	7.5		V/μs
			Full range	4.4*			4.4*			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8*		3.3	4.5*	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5*		2.5	3.8*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250*		50	130*	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4*		1.5	4*	pA/√Hz
		f = 1 kHz			0.4	0.6*		0.4	0.6*	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 5, See Note 5	25°C		< 0.002%			<0.002%		
	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	35	50		35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80			80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		50°			50°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is – 55°C to 125°C.
NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2037Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		20	100	μV
	Input offset voltage long-term drift (see Note 4)				0.006	1	μV/mo
I_{IO}	Input offset current				6	90	nA
I_{IB}	Input bias current				15	90	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−11 to 11	−13 to 13		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω		10.5	12.9		V
		R_L = 2 kΩ		12	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω		−10.5	−13		V
		R_L = 2 kΩ		−12	−13.5		
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V,	R_L = 2 kΩ	5	45		V/μV
		V_O = ±10 V,	R_L = 1 kΩ	3.5	38		
		V_O = ±10 V,	R_L = 600 Ω	2	19		
C_i	Input capacitance				8		pF
z_o	Open-loop output impdance	I_O = 0			50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	100	131		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 4 V to ± 18 V,	R_S = 50 Ω	94	144		dB
I_{CC}	Supply current	V_O = 0,	No load		3.8	5.3	mA

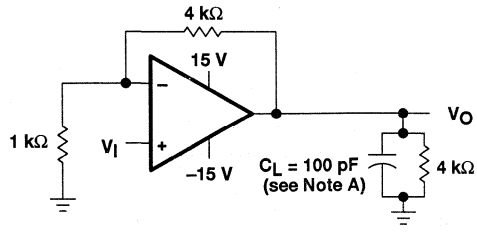
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLE3027Y			UNIT
					MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, See Figure 1	R_L = 2 kΩ,	C_L = 100 pF,	6	7.5		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω,	f = 10 Hz			3.3	8	nV/√Hz
		R_S = 20 Ω,	f = 1 kHz			2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz				50	250	nV
I_n	Equivalent input noise current	f = 10 Hz				1.5	4	pA/√Hz
		f = 1 kHz				0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V,	A_{VD} = 5,	See Note 5		< 0.002%		
	Gain-bandwidth product	f = 100 kHz,	R_L = 2 kΩ,	C_L = 100 pF	35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ				80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ,	C_L = 100 pF			50°		

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

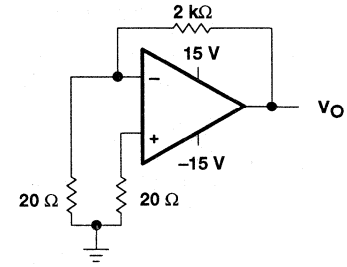


Figure 2. Noise-Voltage Test Circuit

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

initial estimates of parameter distributions

In the on-going program of improving data sheets and supplying more information to our customer, Texas Instruments has added an estimate of not only the typical values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from our characterization of the initial wafer lots of this new device type (see Figure 3). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ±3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 3, there were a total of 835 units from 2 wafer lots. In this case, there is a very good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This will always be the case on newly released products, since there will only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. And, while 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

PARAMETER MEASUREMENT INFORMATION

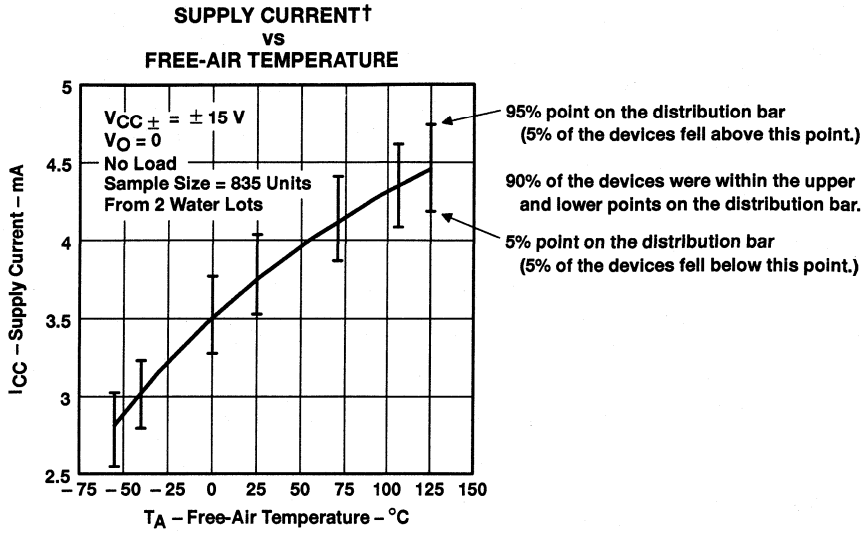


Figure 3. Sample Graph With Distribution Bars

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
ΔV_{IO}	Input offset voltage change	vs Time after power on	5,6
I_{IO}	Input offset current	vs Free-air temperature	7
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	8 9
I_I	Input current	vs Differential input voltage	10
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OM}	Maximum peak output voltage	vs Load resistance vs Free-air temperature	12,13 14,15
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	16 17 18,19 20
z_o	Output impedance	vs Frequency	21
CMRR	Common-mode rejection ratio	vs Frequency	22
k_{SVR}	Supply voltage rejection ratio	vs Frequency	23
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	24, 25 26, 27 28, 29
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	30 31
	Pulse response	Small signal Large signal	32 33
V_n	Equivalent input noise voltage	vs Frequency	34
	Noise voltage (referred to input)	0.1 to 10 Hz	35
	Gain-bandwidth product	vs Supply voltage vs Load capacitance	36 37
SR	Slew rate	vs Free-air temperature	38
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	39 40 41
	Phase shift	vs Frequency	18, 19

TYPICAL CHARACTERISTICS†

TLE2037
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

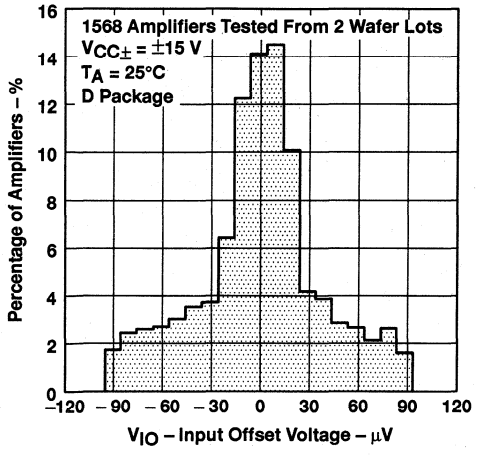


Figure 4

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

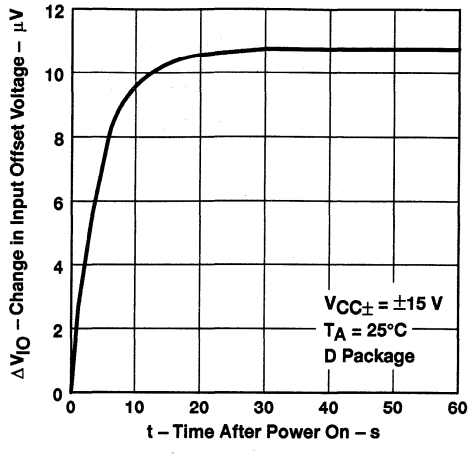


Figure 5

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

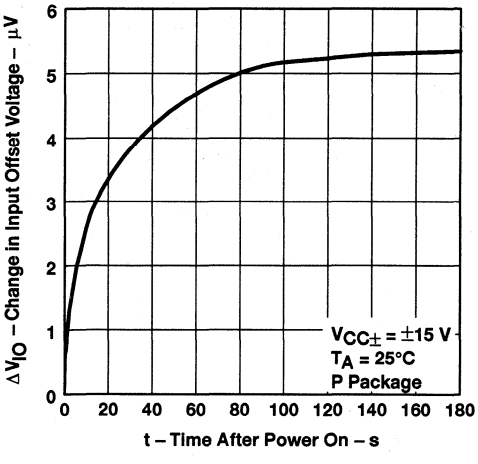


Figure 6

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

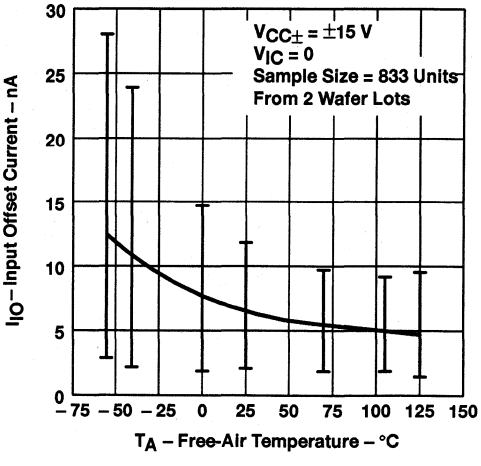


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

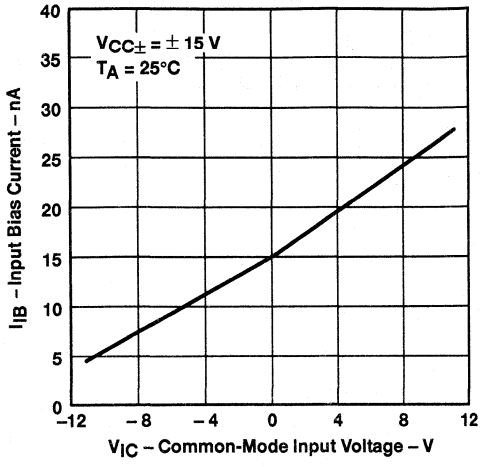


Figure 8

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

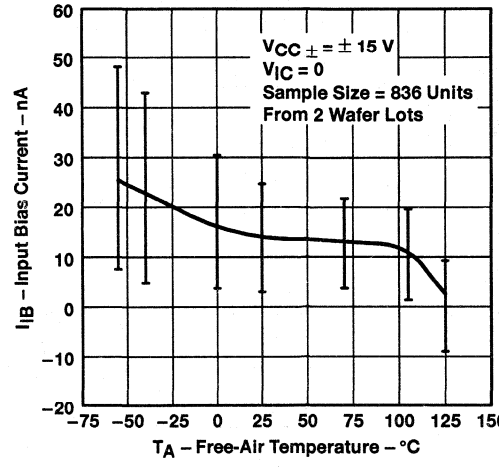


Figure 9

INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

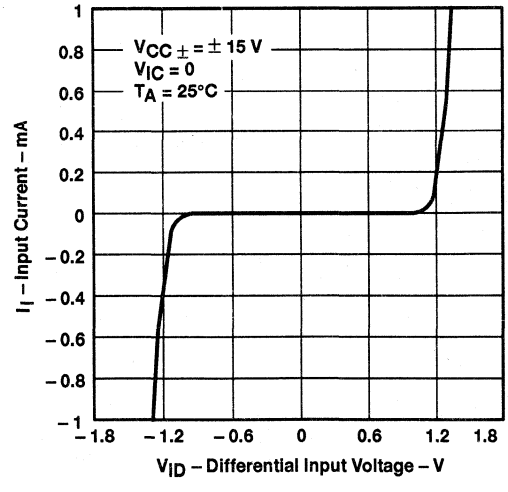


Figure 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

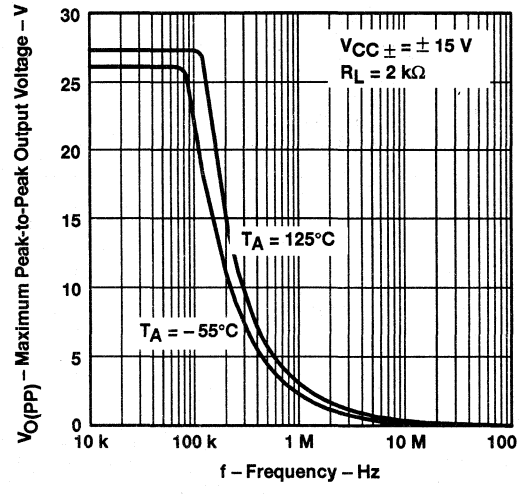


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE VS LOAD RESISTANCE

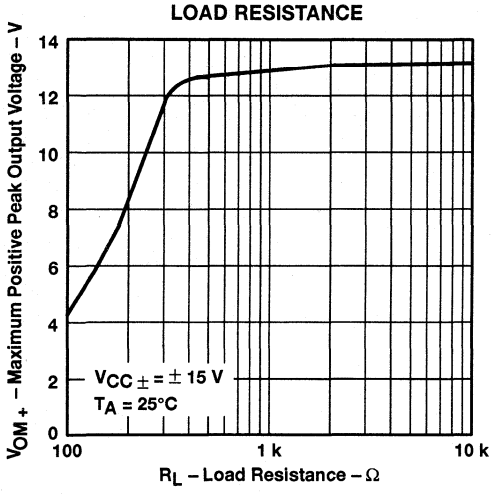


Figure 12

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE VS LOAD RESISTANCE

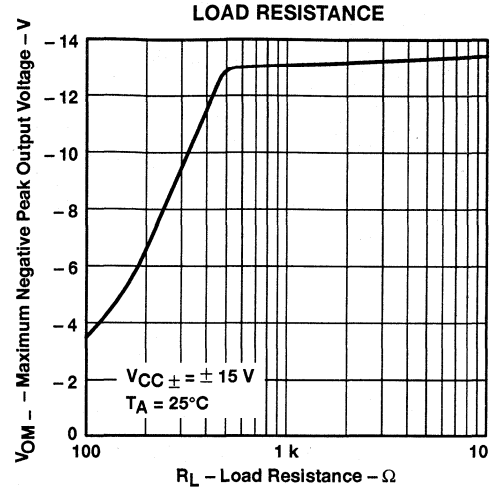


Figure 13

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE VS FREE-AIR TEMPERATURE

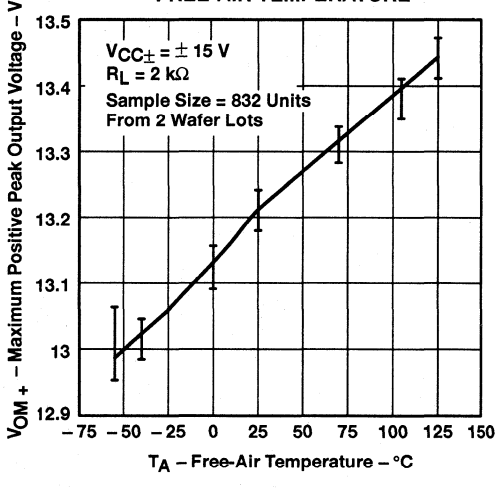


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE VS FREE-AIR TEMPERATURE

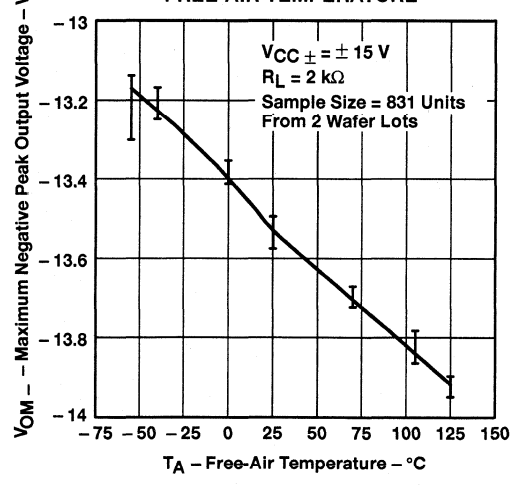


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

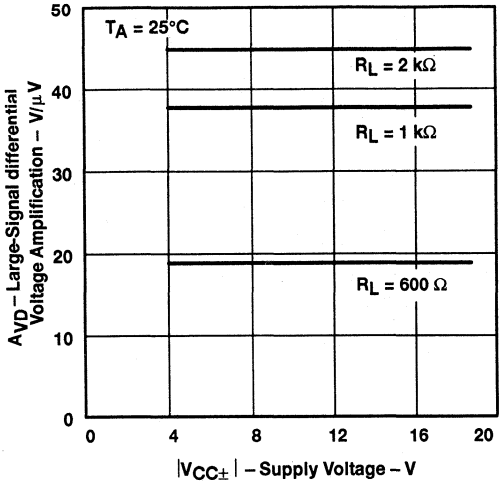


Figure 16

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

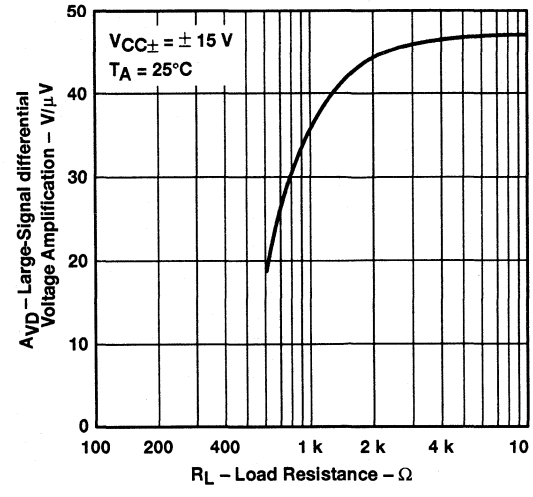


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

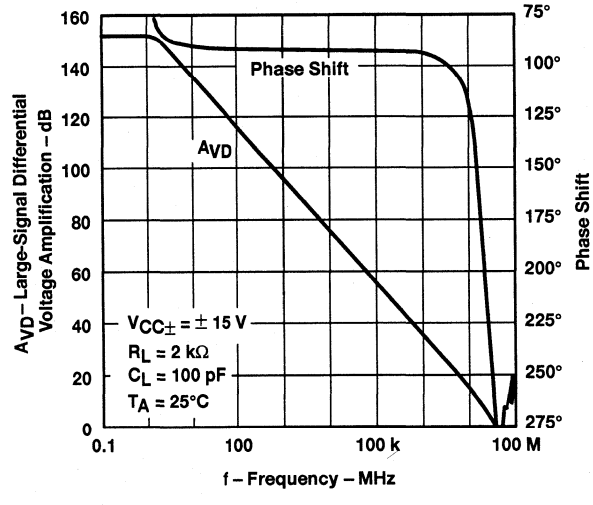


Figure 18

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

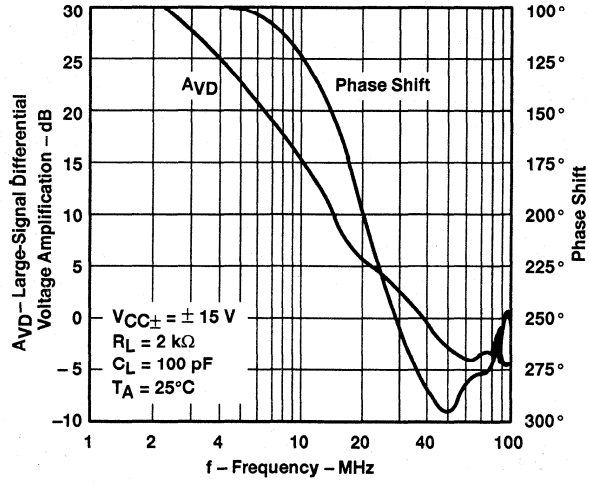


Figure 19

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

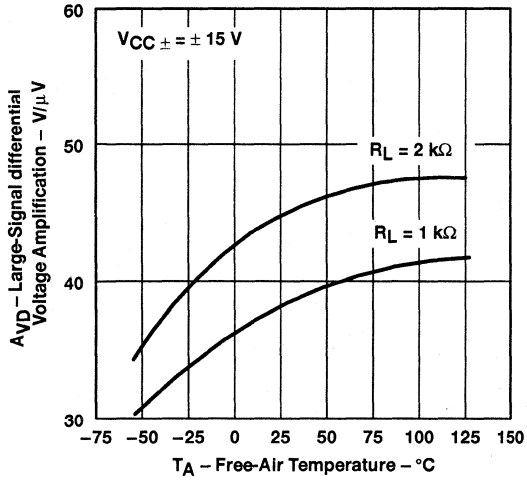


Figure 20

OUTPUT IMPEDANCE
vs
FREQUENCY

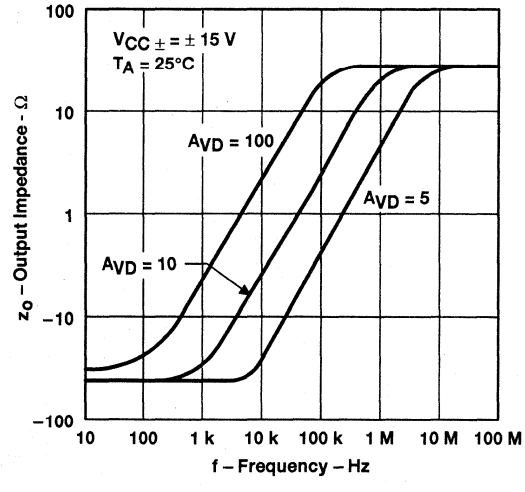


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

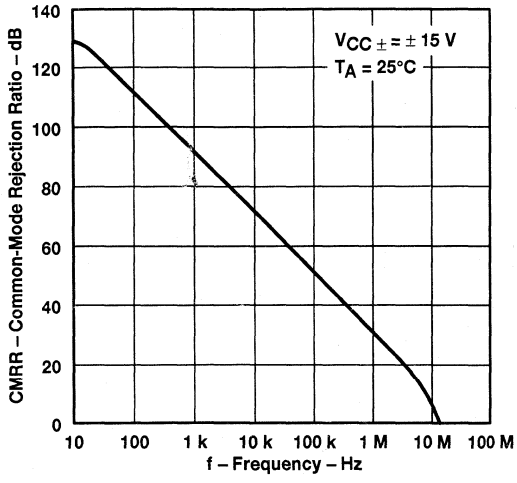


Figure 22

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

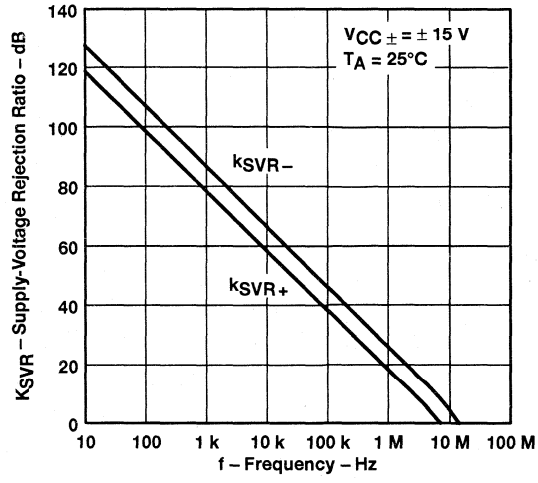


Figure 23

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

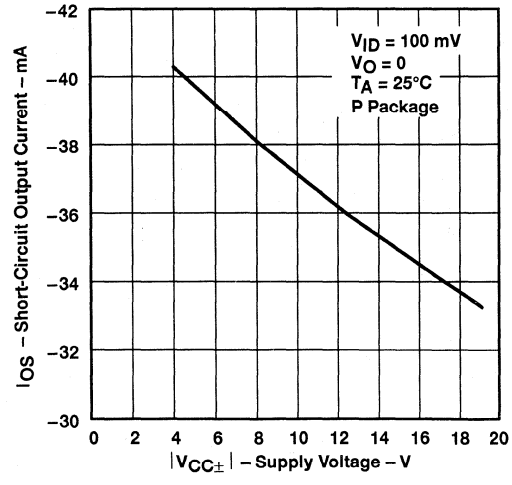


Figure 24

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

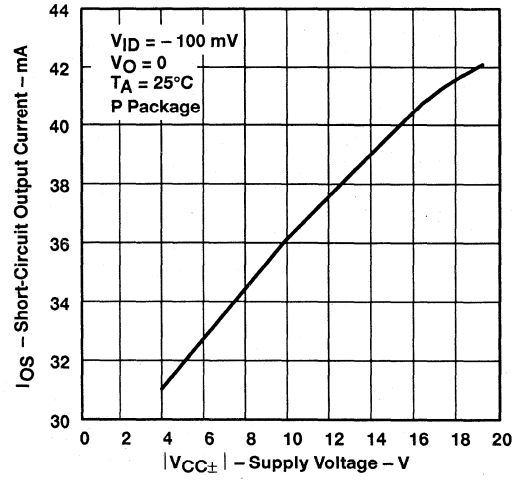


Figure 25

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

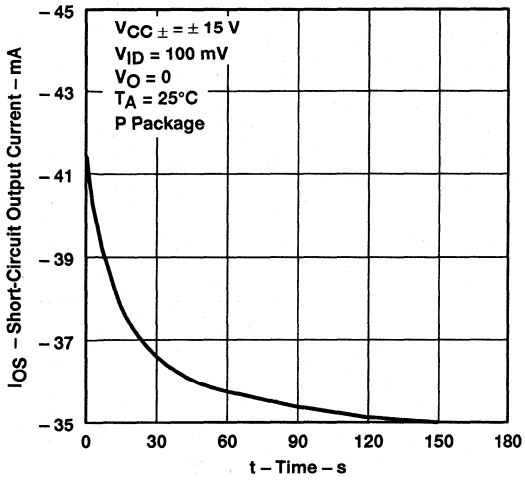


Figure 26

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

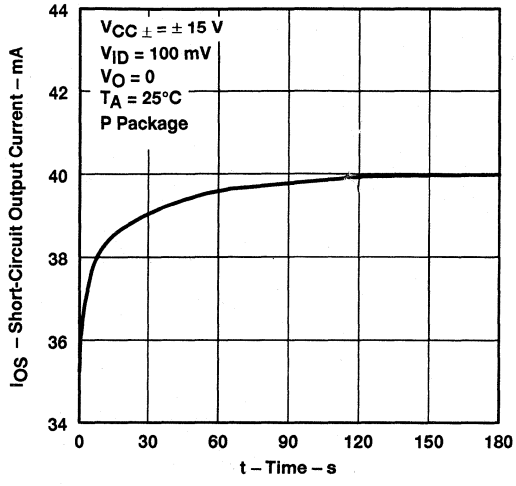


Figure 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

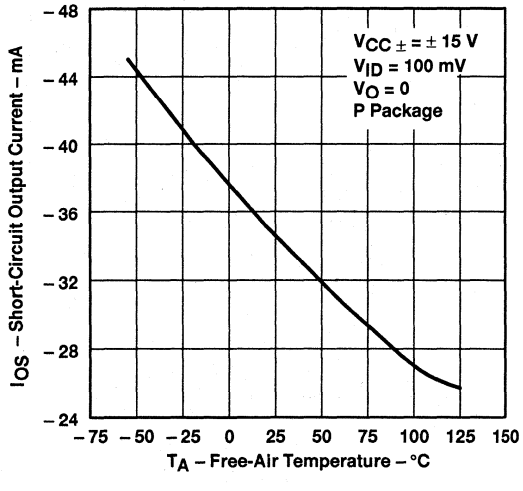


Figure 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

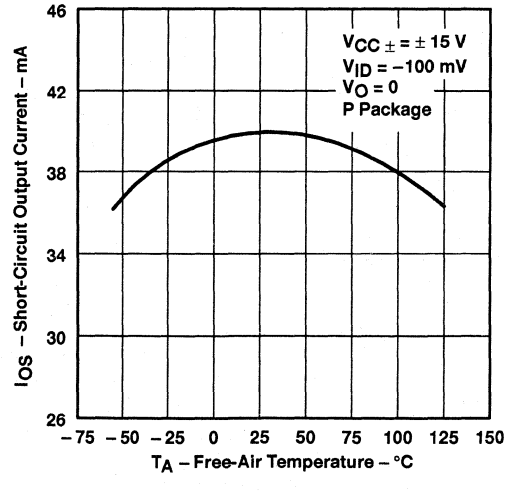


Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

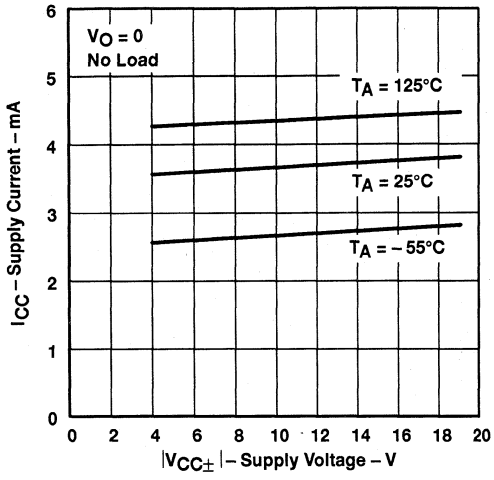


Figure 30

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

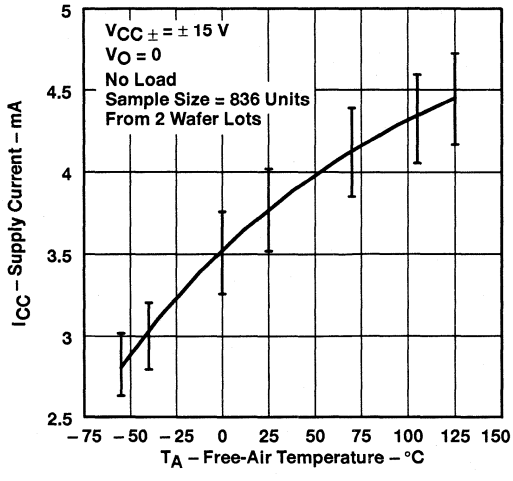


Figure 31

SMALL-SIGNAL
PULSE RESPONSE

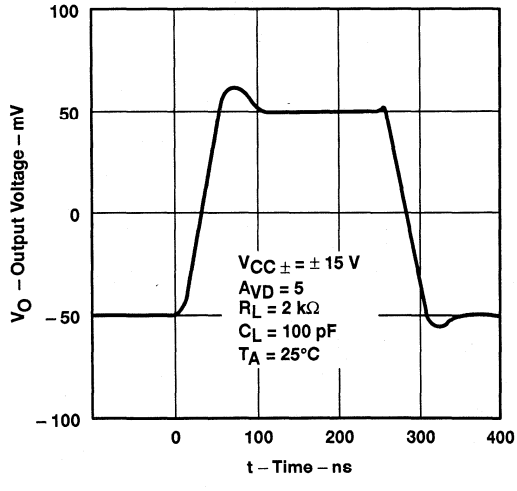


Figure 32

LARGE-SIGNAL
PULSE RESPONSE

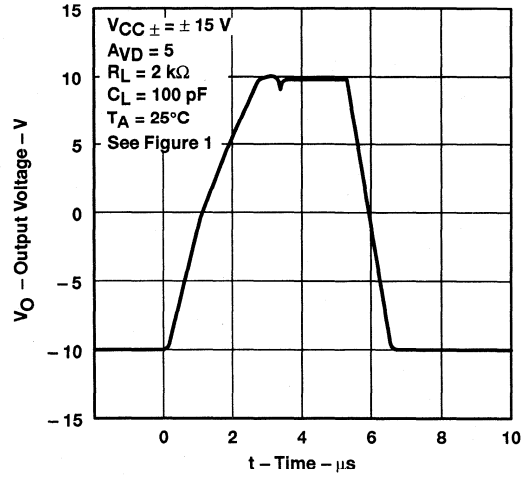


Figure 33

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

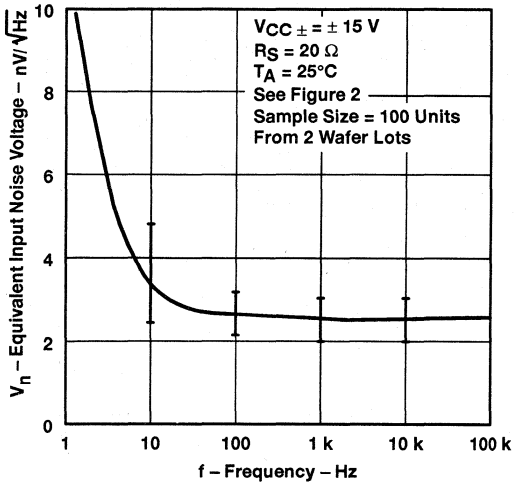


Figure 34

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

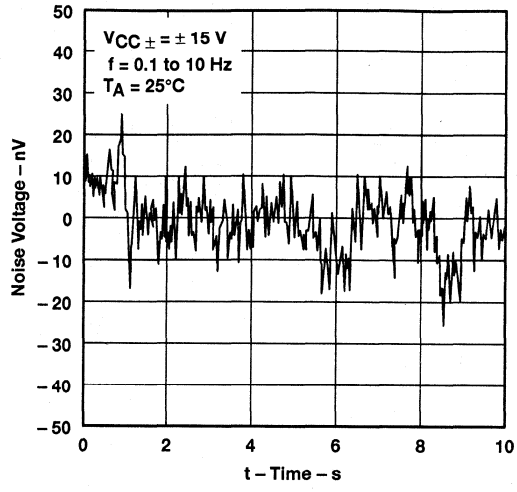


Figure 35

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

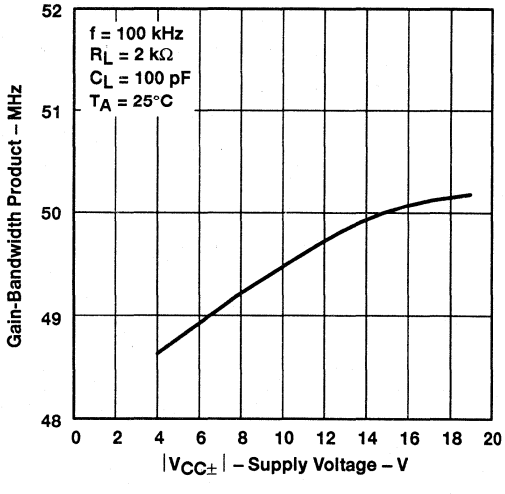


Figure 36

GAIN-BANDWIDTH PRODUCT
vs
LOAD CAPACITANCE

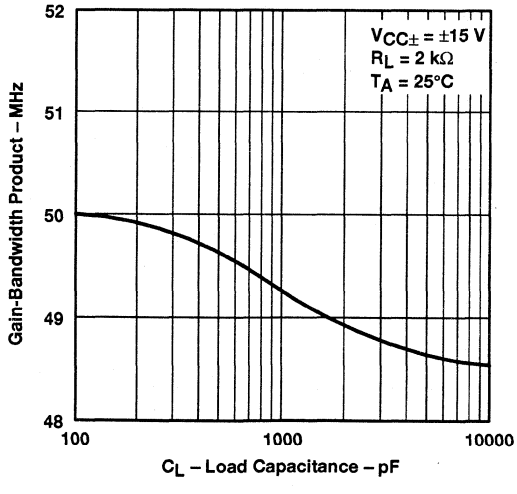


Figure 37

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs FREE-AIR TEMPERATURE

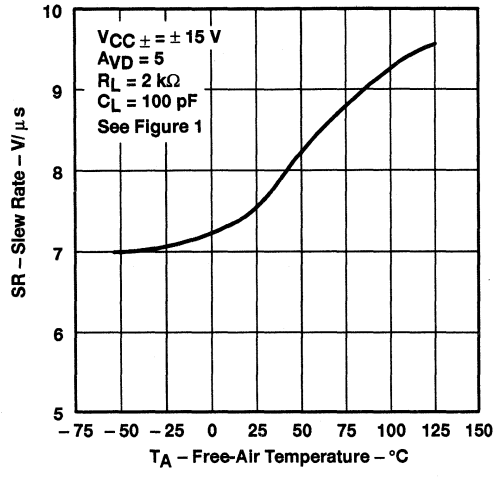


Figure 38

PHASE MARGIN vs SUPPLY VOLTAGE

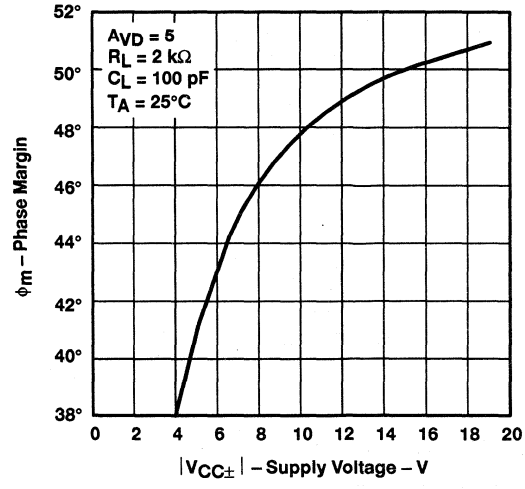


Figure 39

PHASE MARGIN vs LOAD CAPACITANCE

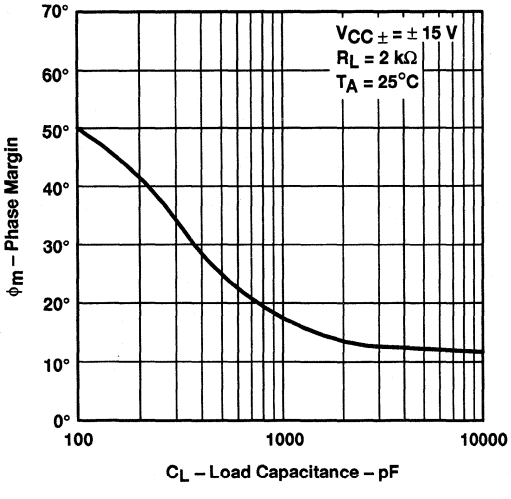


Figure 40

PHASE MARGIN vs FREE-AIR TEMPERATURE

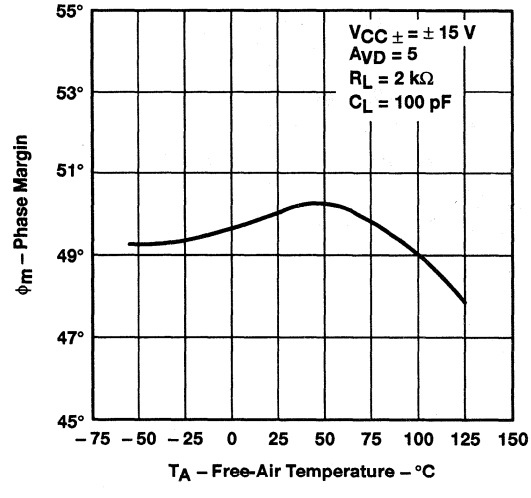


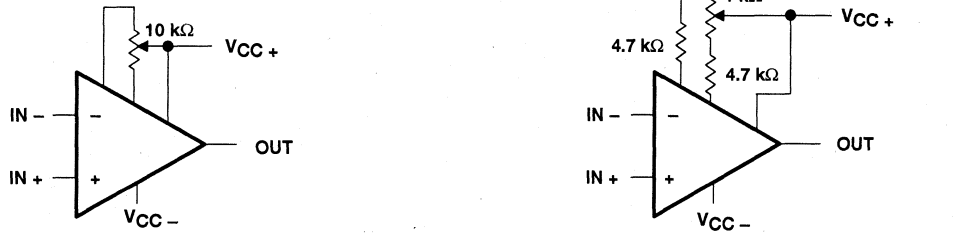
Figure 41

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input offset voltage nulling

The TLE2037 series offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 42 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.



(a) STANDARD ADJUSTMENT

(b) ADJUSTMENT WITH IMPROVED SENSITIVITY

Figure 42. Input Offset Voltage Nulling Circuits

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 42 and 43 were generated using the TLE2037 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)

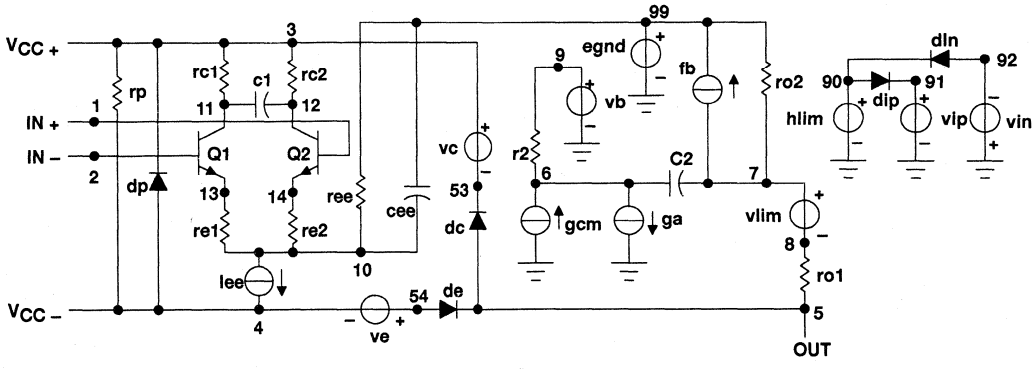


Figure 43. Boyle Macromodel

```
.subckt TLE2037 1 2 3 4 5
*
  c1          11   12 4.003E-12
  c2           6    7 7.500E-12
  dc           5   53 dz
  de          54    5 dz
  dlp         90   91 dz
  dln         92   90 dx
  dp           4    3 dz
  egnd        99    0 poly(2)  (3,0)   (4,0)   0  .5   .5
  fb           7   99 poly(5) vb vc ve vip vln 0 923.4E6 A800E6 800E6 800E6 A800E6
  ga           6    0 11 12 2.121E-3
  gcm          0    6 10 99 597.7E-12
  iee         10    4 dc 56.26E-6
  hlim        90    0 vlim 1K
  q1          11    2 13 qx
  q2          12    1 14 qz
  r2           6    9 100.0E3
  rc1          3   11 471.5
  rc2          3   12 471.5
  re1         13   10 A448
  re2         14   10 A448
  ree         10   99 3.555E6
  ro1          8    5 25
  ro2          7   99 25
  rp           3    4 8.013E3
  vb           9    0 dc 0
  vc           3   53 dc  2.400
  ve          54    4 dc  2.100
  vlim         7    8 dc  0
  vlp         91    0 dc  40
  vln          0   92 dc  40
.model        dx D(Is=800.0E-18)
.model        qx NPN(Is=800.0E-18 Bf=7.031E3)
.ends
```

Figure 44. Macromodel Subcircuit

- **Excellent Output Drive Capability**
  V_O = ±2.5 V Min at R_L = 100 Ω,
  $V_{CC±}$ = ±5 V
  V_O = ±12.5 V Min at R_L = 600 Ω,
  V_{CC} = ±15 V
- **Low Supply Current . . . 280 μA Typ**
- **High Unity-Gain Bandwidth**
  1.8 MHz Typ
- **High Slew Rate . . . 3.4 V/μs Typ**
- **Macromodels Included**
- **Wide Operating Supply Voltage Range**
  $V_{CC±}$ = ±3.5 V to ±19 V
- **High Open-Loop Gain . . . 230 V/mV Typ**
- **Low Offset Voltage . . . 500 μV Max**
- **Low Offset Voltage Drift With Time**
  0.04 μV/mo Typ
- **Low Input Bias Current . . . 4 pA Typ**

description

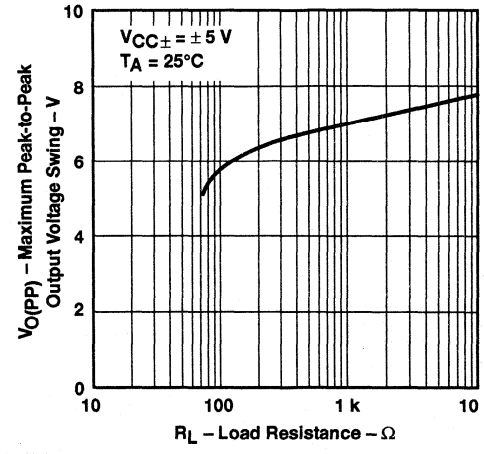
The TLE2061, TLE2061A, TLE2061B, and TLE2061Y are JFET-input, low-power, precision operational amplifiers manufactured using Texas Instruments Excalibur process. These devices combine outstanding output drive capability with low power consumption, excellent dc precision, and wide bandwidth.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a precision device remaining precise even with changes in temperature and over years of use.

The TLE2061, TLE2061A, and TLE2061B are ideal choices for any application requiring excellent dc precision, high output drive, wide bandwidth, and low power consumption.

A variety of available package options includes small-outline (D) and chip-carrier (FK) versions for high-density system applications.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



AVAILABLE OPTIONS

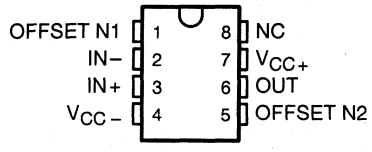
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES SMALL OUTLINE (D)	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°C	500 μV	—	—	—	—	—	—	TLE2061Y
	1.5 μV	TLE2061ACD	—	—	—	TLE2061ACP	—	
	3 mV	TLE2061CD	TLE2061CDBLE	—	—	TLE2061CP	TLE2061CPWLE	
−40°C to 85°C	500 μV	—	—	—	—	—	—	—
	1.5 μV	TLE2061AID	—	—	—	TLE2061AIP	—	
	3 mV	TLE2061ID	—	—	—	TLE2061IP	—	
−55°C to 125°C	500 μV	—	—	—	—	—	—	—
	1.5 μV	TLE2061AMD	—	TLE2061AMFK	TLE2061AMJG	TLE2061AMP	—	
	3 mV	TLE2061MD	—	TLE2061MFK	TLE2061MJG	TLE2061MP	—	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2061ACDR). The DB and PW packages are available left-end taped and reeled (indicated by the LE suffix on the device type (e.g., TLE2061CDBLE). Chips are tested at 25°C.

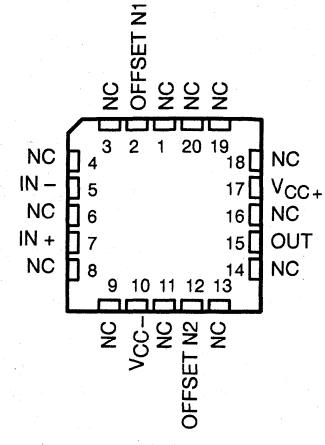
description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



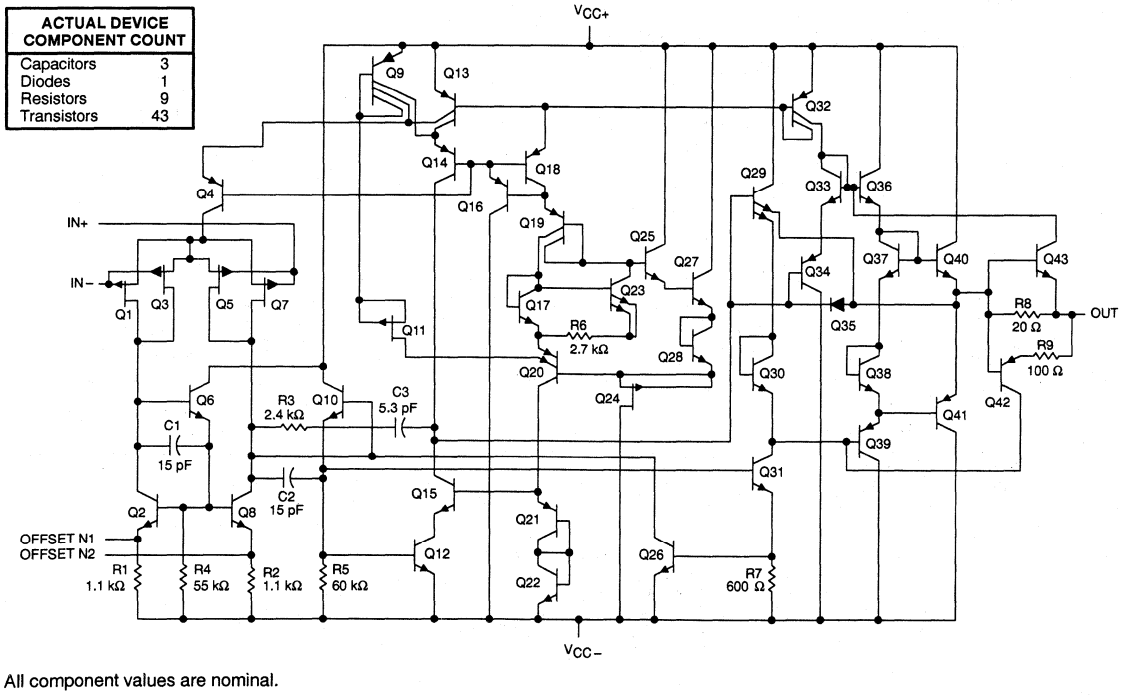
FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic

ACTUAL DEVICE COMPONENT COUNT	
Capacitors	3
Diodes	1
Resistors	9
Transistors	43

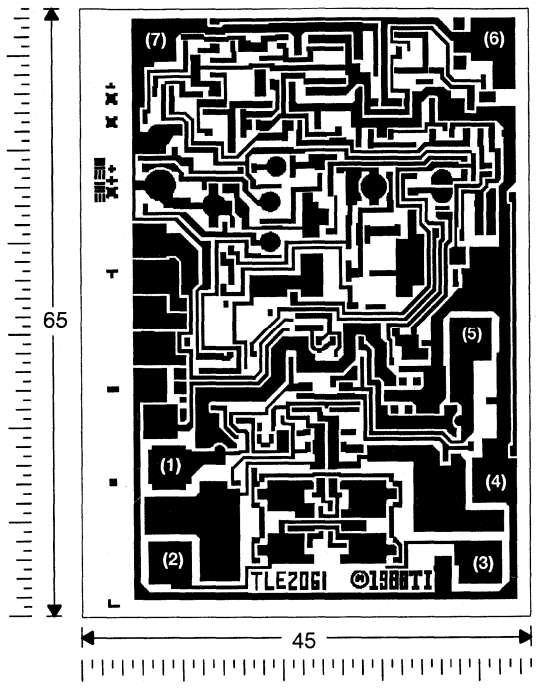


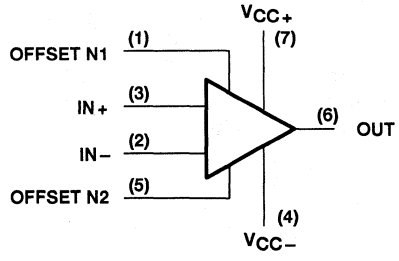
All component values are nominal.

TLE2061Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2061. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 X 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ± 10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} ..... −19 V
Differential input voltage, V_{ID} (see Note 2) ..... ±38 V
Input voltage range, V_I (any input) ..... $\pm V_{CC}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±80 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... −80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW/°C	336 mW	—	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	336 mW	—	—

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	±3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	−1.6	4	−1.6	4	−1.6	4	V
	$V_{CC\pm} = \pm 15$ V	−11	13	−11	13	−11	13	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061C	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			4	
		TLE2061AC		25°C		0.6	2.6	
				Full range			3.5	
		TLE2061BC		25°C		0.5	1.9	
				Full range			2.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.3			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		29		μA

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.2	3.4		V/μs
			Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, f = 10 kHz, $V_{O(PP)}$ = 2 V, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω, C_L = 100 pF			1.3		
t_s	Settling time	0.1%	25°C		5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		58°		
		R_L = 100 Ω, C_L = 100 pF			75°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061C, TLE2061AC, TLE2061BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061C	V_{IC} = 0, R_S = 50 kΩ	25°C		0.6	3	mV
				Full range			3.9	
		TLE2061AC		25°C		0.5	1.5	
				Full range			2.5	
		TLE2061BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		290	350	μA
			Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		34		μA

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061I	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			4.4	
		TLE2061AI		25°C		0.6	2.6	
				Full range			3.9	
		TLE2061BI		25°C		0.5	1.9	
				Full range			2.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.1			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.1			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		29		μA

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061I	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			4.3	
		TLE2061AI		25°C		0.5	1.5	
				Full range			2.9	
		TLE2061BI		25°C		0.3	0.5	
				Full range			1.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	01			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		290	350	μA
			Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		34		μA

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061M, TLE2061AM, TLE2061BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061M	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			6	
		TLE2061AM		25°C		0.6	2.6	
				Full range			4.6	
		TLE2061BM		25°C		0.5	1.9	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
			R_L = 600 Ω	25°C	2.5	3.6		
				Full range	2			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.5	−3.9		V
				Full range	−3			
		FK and JG packages	R_L = 600 Ω	25°C	−2.5	−3.5		
				Full range	−2			
		D and P packages	R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to −2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			
		D and P packages	V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061M TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	V_O = 0, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		39		μA

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061M TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		59		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		1.8		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.3		
t_s	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		58°		
		R_L = 600 Ω,	C_L = 100 pF		75°		

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061M TLE2061AM TLE2061BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061M	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			6	
		TLE2061AM		25°C		0.5	1.5	
				Full range			3.6	
		TLE2061BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13	13.7		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13	−13.7		V
				Full range	−12.5			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	7			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061M TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		290	350	μA
			Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		46		μA

† Full range is –55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061M TLE2061AM TLE2061BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is –55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

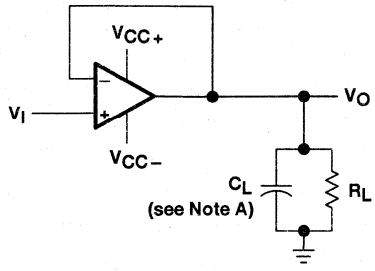
PARAMETER		TEST CONDITIONS	TLE2061Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		0.6	3	mV
α_{VIO}	Input offset voltage long-term drift (see Note 4)			0.04		μV/mo
I_{IO}	Input offset current			2		pA
I_{IB}	Input bias current			4		pA
V_{ICR}	Common-mode input voltage range		−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	13.2	13.7		V
		R_L = 600 Ω	12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ	−13.2	−13.7		V
		R_L = 600 Ω	−12.5	−13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V, R_L = 600 Ω	25	100		
		V_O = 0 to −8 V, R_L = 600 Ω	3	25		
r_i	Input resistance			10^{12}		Ω
c_i	Input capacitance			4		pF
z_o	Open-loop output impedance	I_O = 0		280		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, V_{IC} = V_{ICR}min	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	75	93		dB
I_{CC}	Supply current	V_O = 0, No load		290	350	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2061Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 100 pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω		70		nV/√Hz
		f = 1 kHz, R_S = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		1.1		μV
I_n	Equivalent input noise current	f = 1 Hz		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, f = 10 kHz, $V_{O(PP)}$ = 2 V, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF		2		MHz
		R_L = 600 Ω, C_L = 100 pF		1.5		
t_s	Settling time	0.1%		5		μs
		0.01%		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF		60°		
		R_L = 600 Ω, C_L = 100 pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

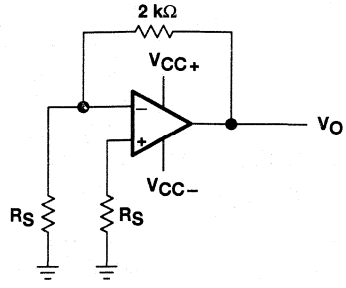
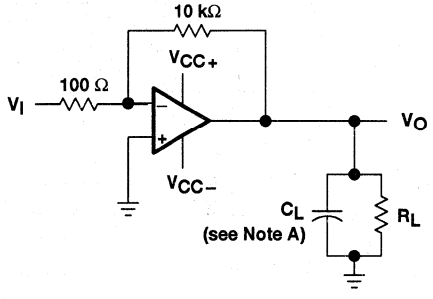


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2061, TLE2061A, and TLE2061B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted mathematically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5 6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{ICR}	Common-mode input voltage range limits	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage	vs Output current vs Supply voltage	8, 9 10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	15 16
I_{OS}	Short-circuit output current	vs Time vs Free-air temperature	17 18
z_o	Output impedance	vs Frequency	19
CMRR	Common-mode rejection ratio	vs Frequency	20
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	21 22
	Pulse response	Small signal Large signal	23, 24 25, 26
	Noise voltage (referred to input)	0.1 to 10 Hz	27
V_n	Equivalent input noise voltage	vs Frequency	28
THD	Total harmonic distortion	vs Frequency	29, 30
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	31 32
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	33 34 35
	Phase shift	vs Frequency	15

TYPICAL CHARACTERISTICS†

TLE2061
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

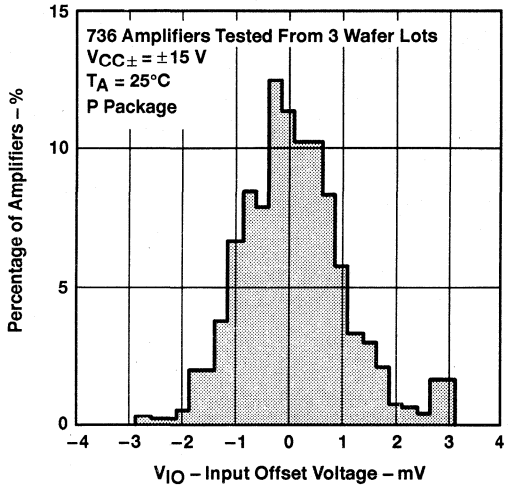


Figure 4

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

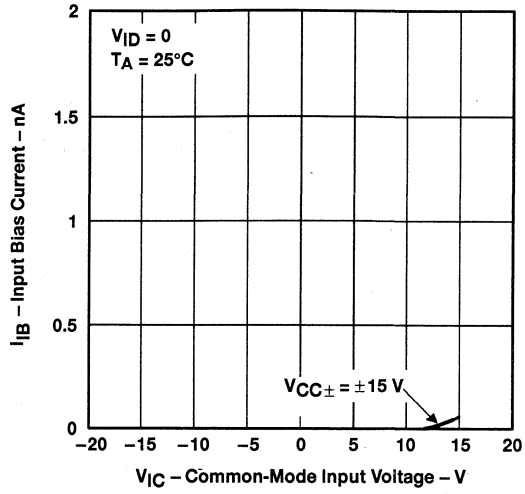


Figure 5

INPUT BIAS CURRENT
AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

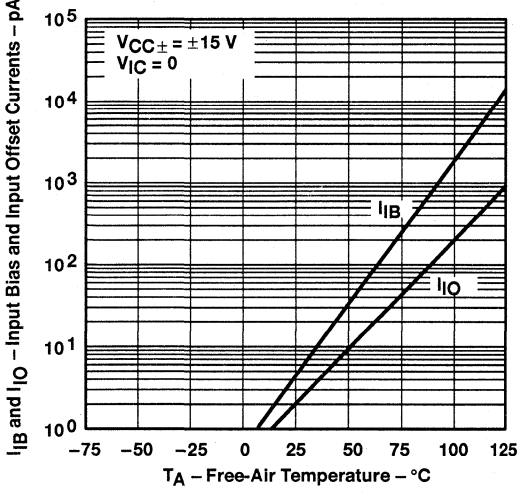


Figure 6

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

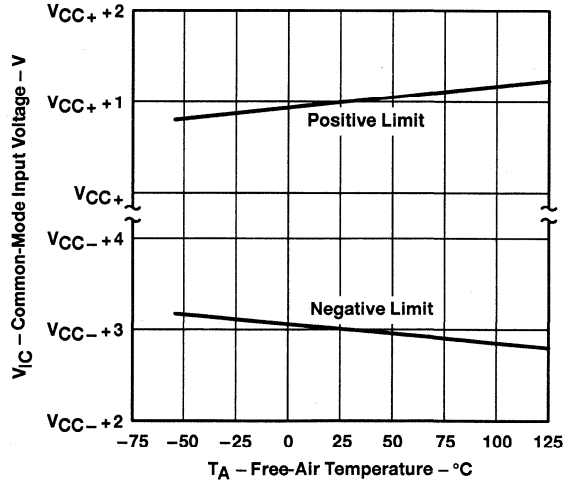


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

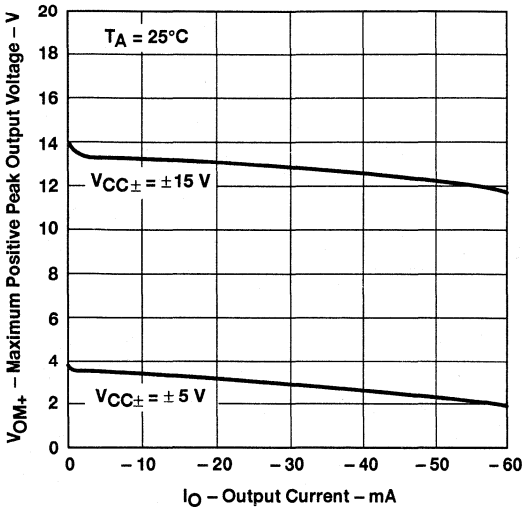


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

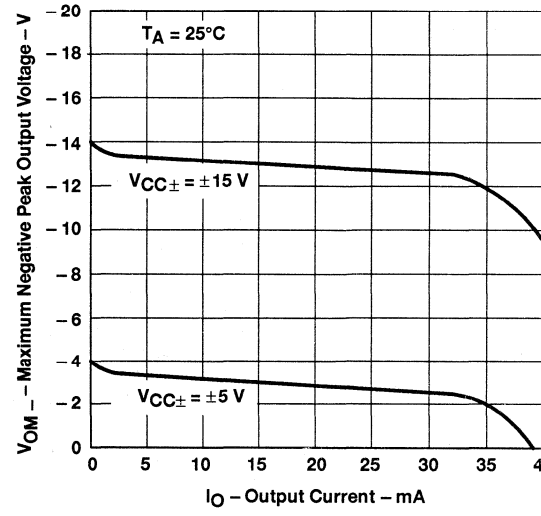


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

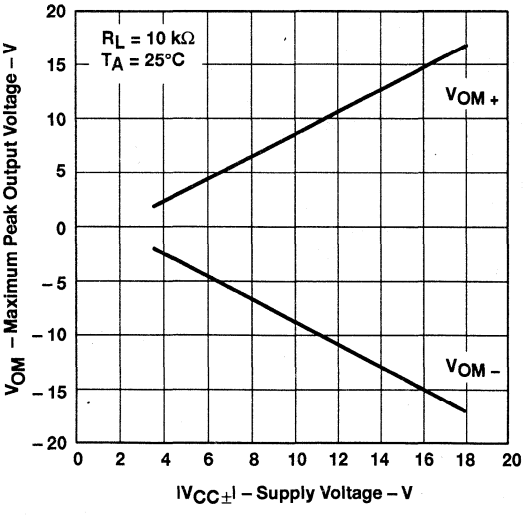


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

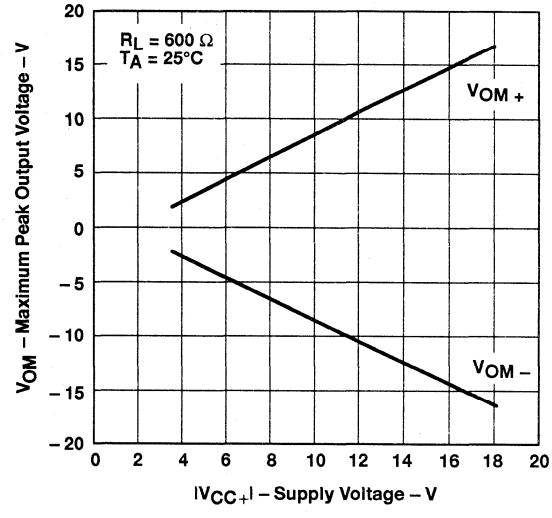


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

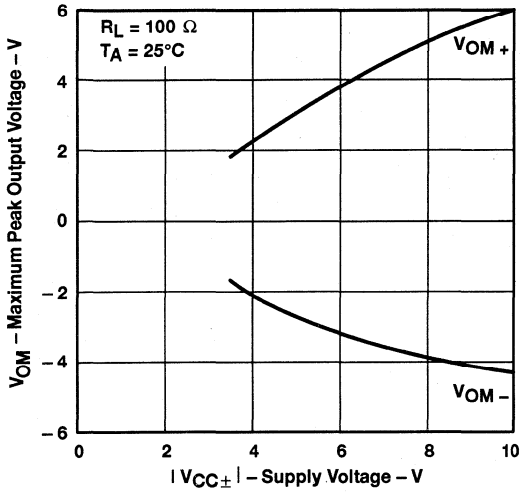


Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

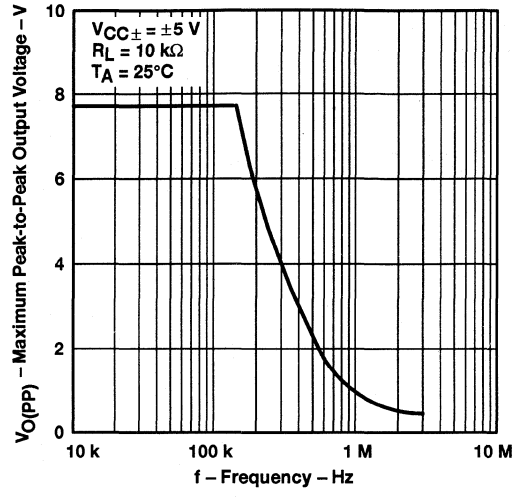


Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

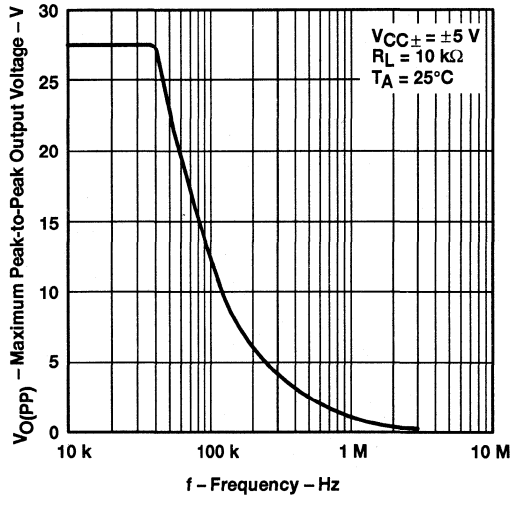


Figure 14

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

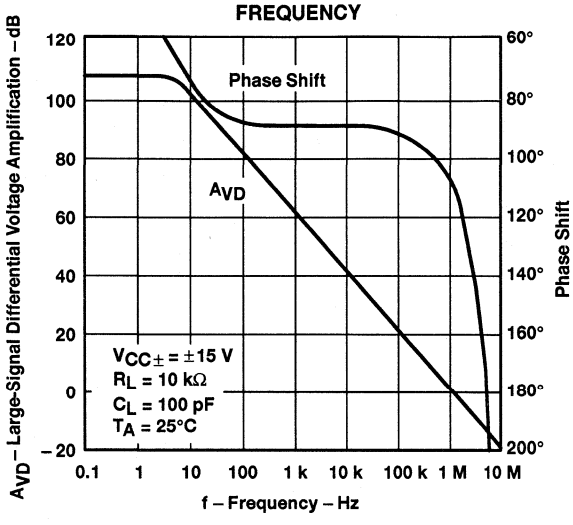


Figure 15

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

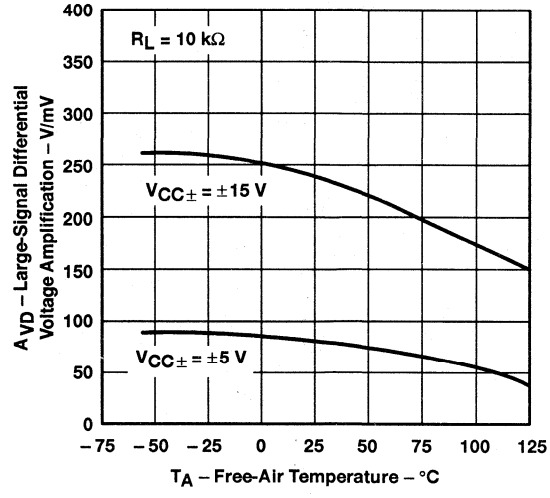


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

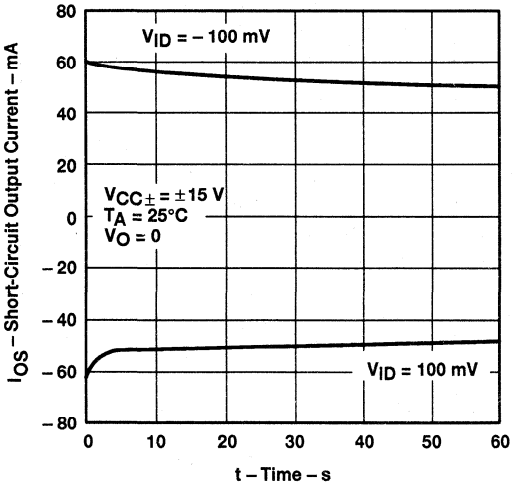


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

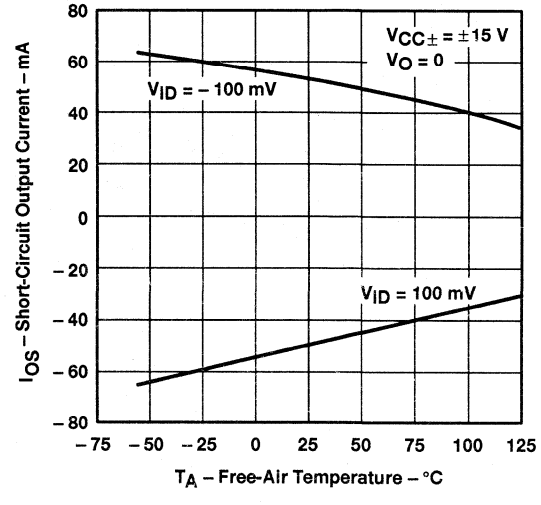


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE vs FREQUENCY

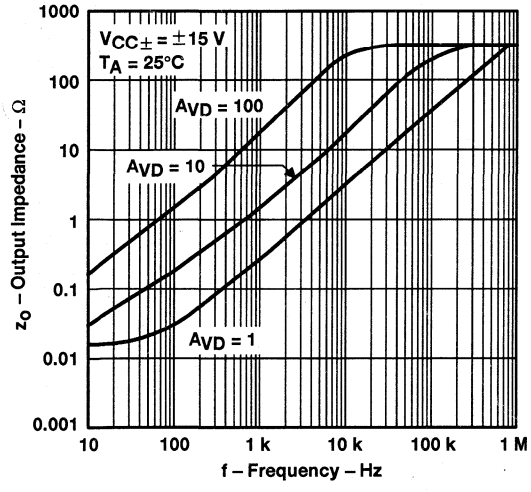


Figure 19

COMMON-MODE REJECTION RATIO vs FREQUENCY

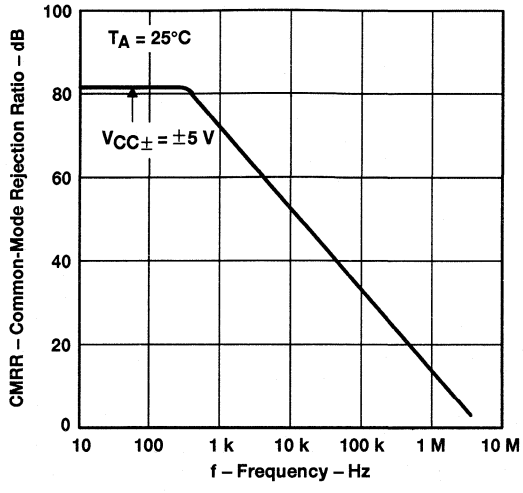


Figure 20

SUPPLY CURRENT vs SUPPLY VOLTAGE

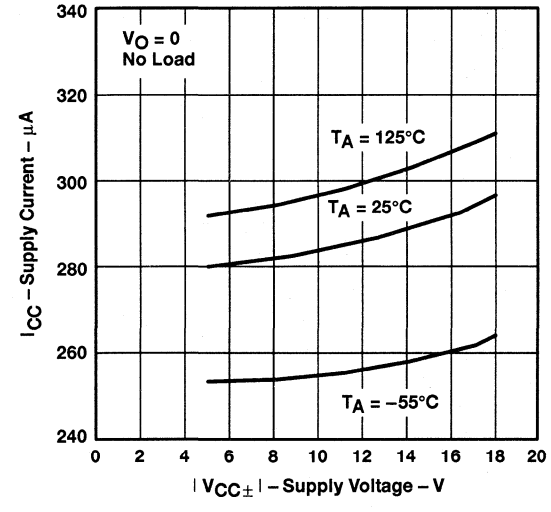


Figure 21

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

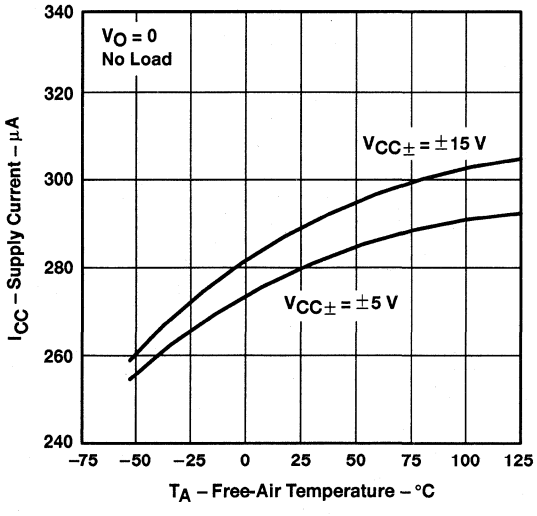


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

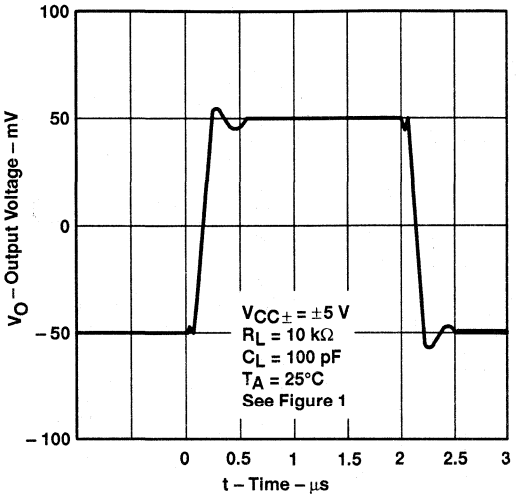


Figure 23

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

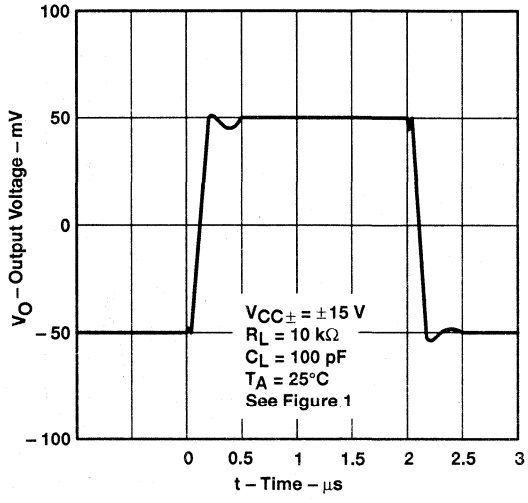


Figure 24

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

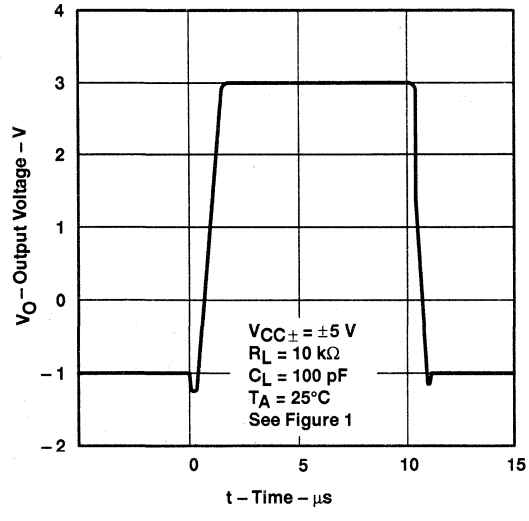


Figure 25

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

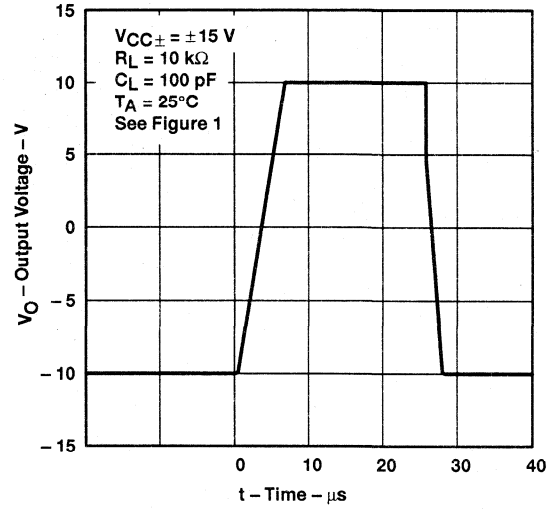


Figure 26

TYPICAL CHARACTERISTICS

NOISE VOLTAGE (REFERRED TO INPUT) OVER A 10-SECOND INTERVAL

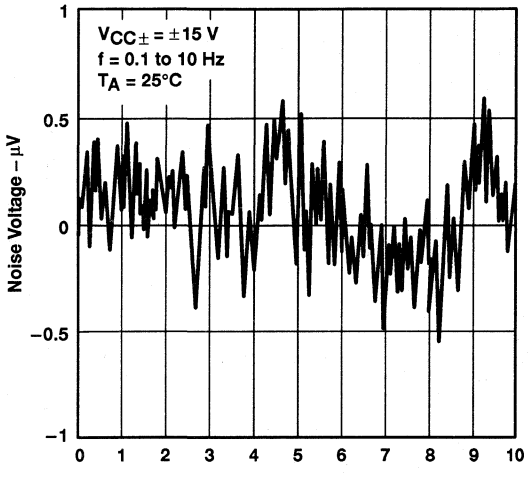


Figure 27

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

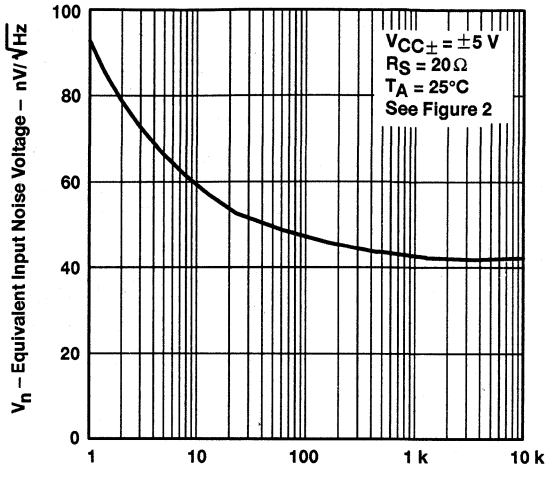


Figure 28

TOTAL HARMONIC DISTORTION vs FREQUENCY

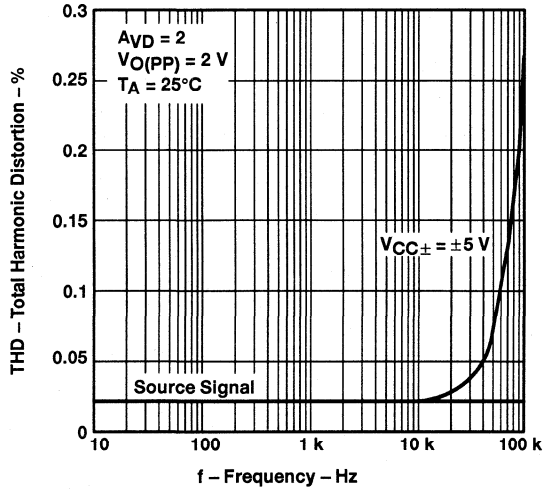


Figure 29

TOTAL HARMONIC DISTORTION vs FREQUENCY

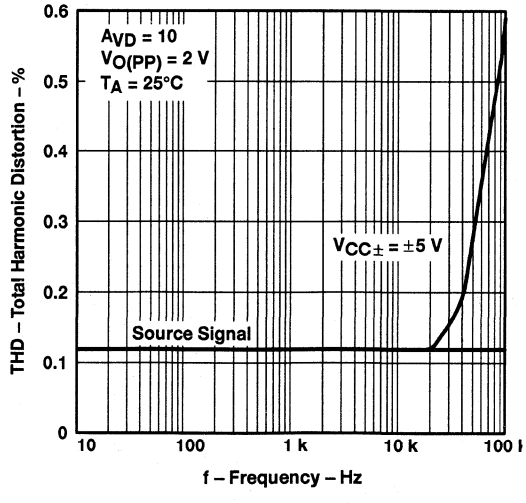


Figure 30

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

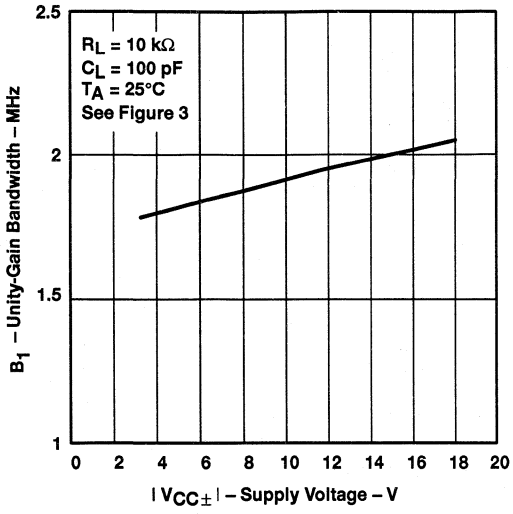


Figure 31

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

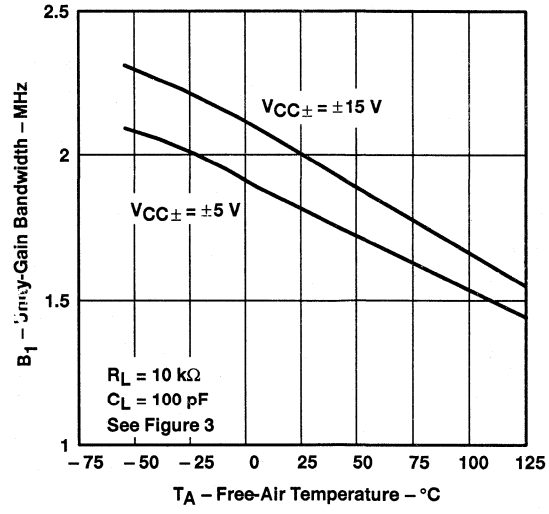


Figure 32

PHASE MARGIN
vs
SUPPLY VOLTAGE

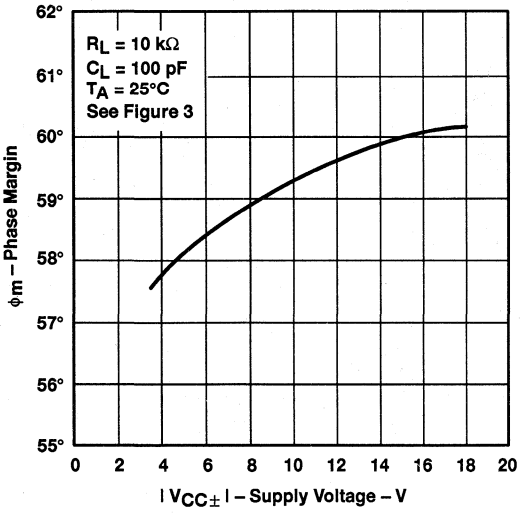


Figure 33

PHASE MARGIN
vs
LOAD CAPACITANCE

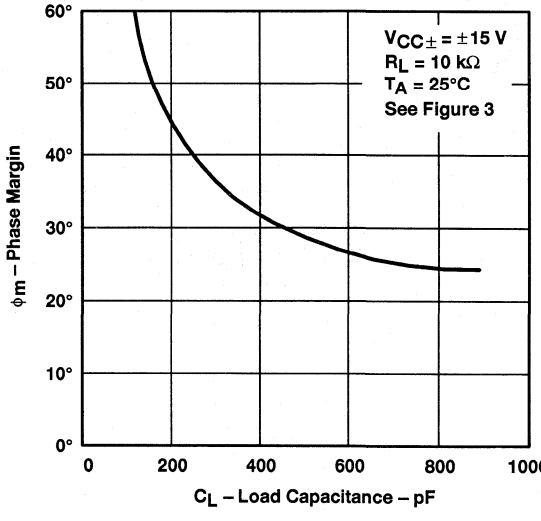


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

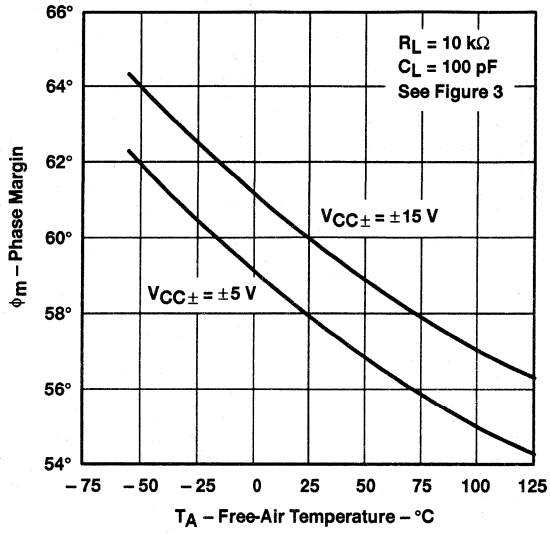


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 36 are generated using the TLE2061 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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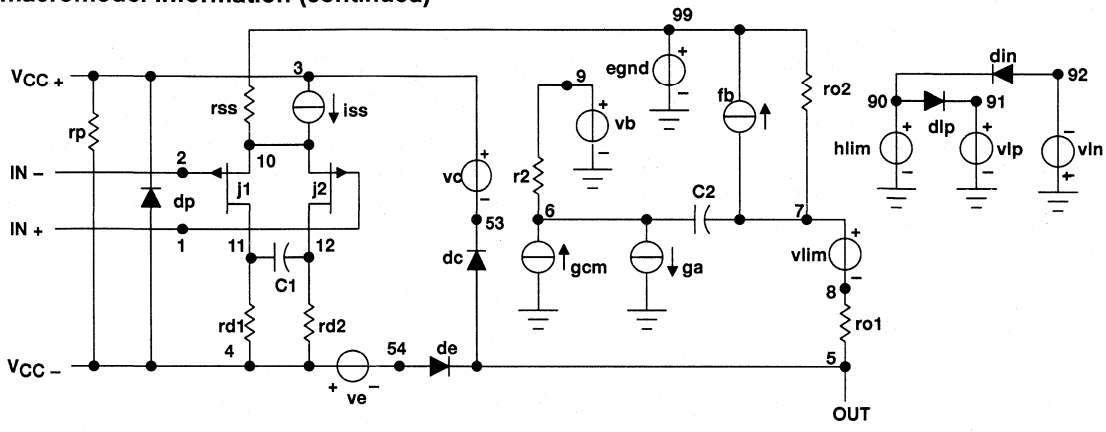
APPLICATION INFORMATION

macromodel information (continued)




```
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  c1   11   12  1.457E-12
  c2    6    7  15.00E-12
  dc    5   53  dx
  de   54    5  dx
  dlp  90   91  dx
  dln  92   90  dx
  dp    4    3  dx
  egnd 99    0  poly(2) (3,0) (4,0) 0 .5 .5
  fb    7   99  poly(5) vb vc ve vlp vln 0 4.357E6  -4E6 4E6 4E6 -4E6
  ga    6    0  11 12 188.5E-6
  gcm   0    6  10 99 3.352E-9
  iss   3   10  dc 51.00E-6
  hlim 90    0  vlim 1K
  j1   11    2  10 jx
  j2   12    1  10 jx
  r2    6    9  100.0E3
  rd1   4   11  5.305E3
  rd2   4   12  5.305E3
  ro1   8    5  280
  ro2   7   99  280
  rp    3    4  113.2E3
  rss  10   99  3.922E6
  vb    9    0  dc 0
  vc    3   53  dc 2
  ve   54    4  dc 2
  vlim  7    8  dc 0
  vlp  91    0  dc 50
  vln   0   92  dc 50
.model dx D(Is=800.0E-18)
.model jx PJF(Is=2.000E-12 Beta=423E-6 Vto=-1)
.ends
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Figure 36. Boyle Macromodel and Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2061, TLE2061A, and TLE2061B are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction. Because of the extremely high input impedance and resulting low bias current requirements, the TLE2061, TLE2061A, and TLE2061B are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 37). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

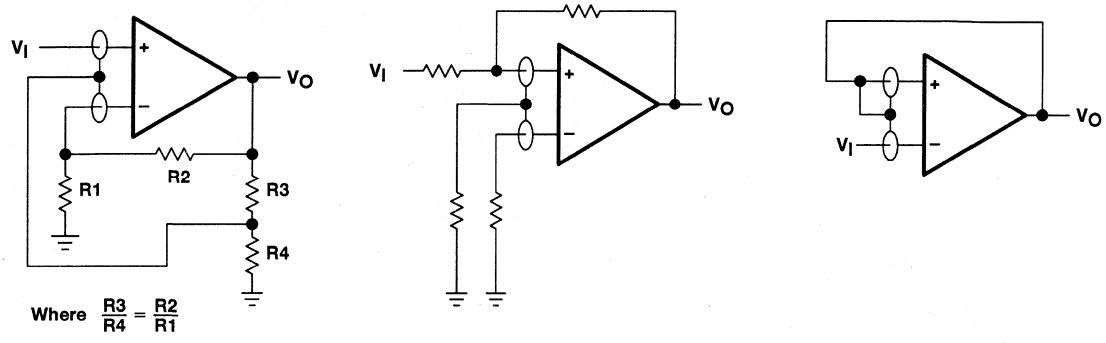


Figure 37. Use of Guard Rings

input offset voltage nulling

The TLE2061 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 38 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left unconnected.

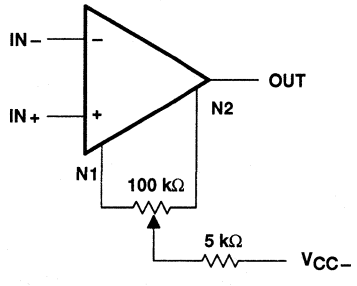


Figure 38. Input Offset Voltage Nulling

- **Excellent Output Drive Capability**
  V_O = ±2.5 V Min at R_L = 100 Ω,
  $V_{CC±}$ = ±5 V
  V_O = ±12.5 V Min at R_L = 600 Ω,
  $V_{CC±}$ = ±15 V
- **Low Supply Current**
  280 μA Typ Per Amplifier
- **High Unity-Gain Bandwidth . . . 2 MHz Typ**
- **High Slew Rate . . . 3.4 V/μs Typ**
- **Macromodels Included**
- **Wide Operating Supply Voltage Range**
  $V_{CC±}$ = ±3.5 V to ±19 V
- **High Open-Loop Gain . . . 230 V/mV Typ**
- **Low Offset Voltage . . . 1 mV Max**
- **Low Offset Voltage Drift With Time**
  0.04 μV/mo Typ
- **Low Input Bias Current . . . 4 pA Typ**

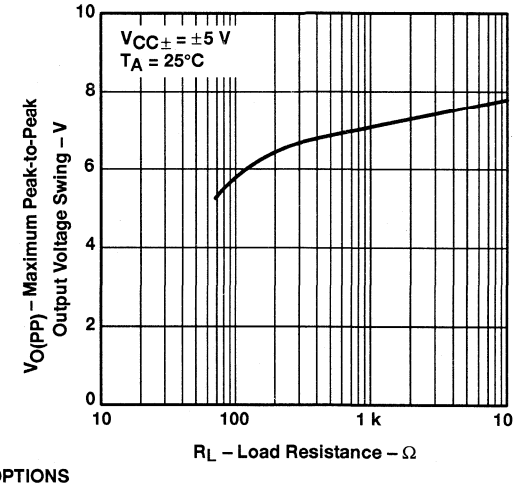
description

The TLE2062, TLE2062A, TLE2062B, and TLE2062Y are JFET-input, low power, precision dual operational amplifiers manufactured using Texas Instruments Excalibur process. These devices combine outstanding output drive capability with low power consumption, excellent dc precision, and wide bandwidth.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a precision device remaining precise even with changes in temperature and over years of use.

The TLE2062, TLE2062A, and TLE2062B are ideal choices for any application requiring excellent dc precision, high output drive, wide bandwidth, and low power consumption.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CHIP FORM (Y)
0°C	1 mV	TLE2062BCD	—	—	TLE2062BCP	—
to	2 mV	TLE2062ACD	—	—	TLE2062ACP	—
70°C	4 mV	TLE2062CD	—	—	TLE2062CP	TLE2062Y
−40°C	1 mV	TLE2062BID	—	—	TLE2062BIP	—
to	2 mV	TLE2062AID	—	—	TLE2062AIP	—
85°C	4 mV	TLE2062ID	—	—	TLE2062IP	—
−55°C	1 mV	TLE2062BMD	TLE2062BMFK	TLE2062BMJG	TLE2062BMP	—
to	2 mV	TLE2062AMD	TLE2062AMFK	TLE2062AMJG	TLE2062AMP	—
125°C	4 mV	TLE2062MD	TLE2062MFK	TLE2062BMJG	TLE2062BMP	—

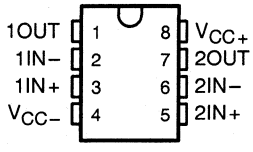
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2062ACDR). Chips are tested at 25°C.

description (continued)

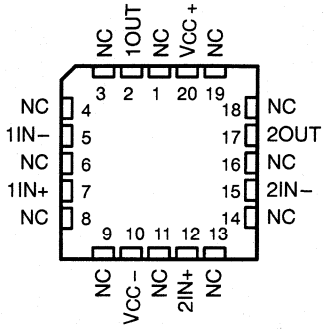
A variety of available package options includes small-outline and chip-carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

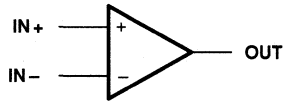


FK PACKAGE
(TOP VIEW)

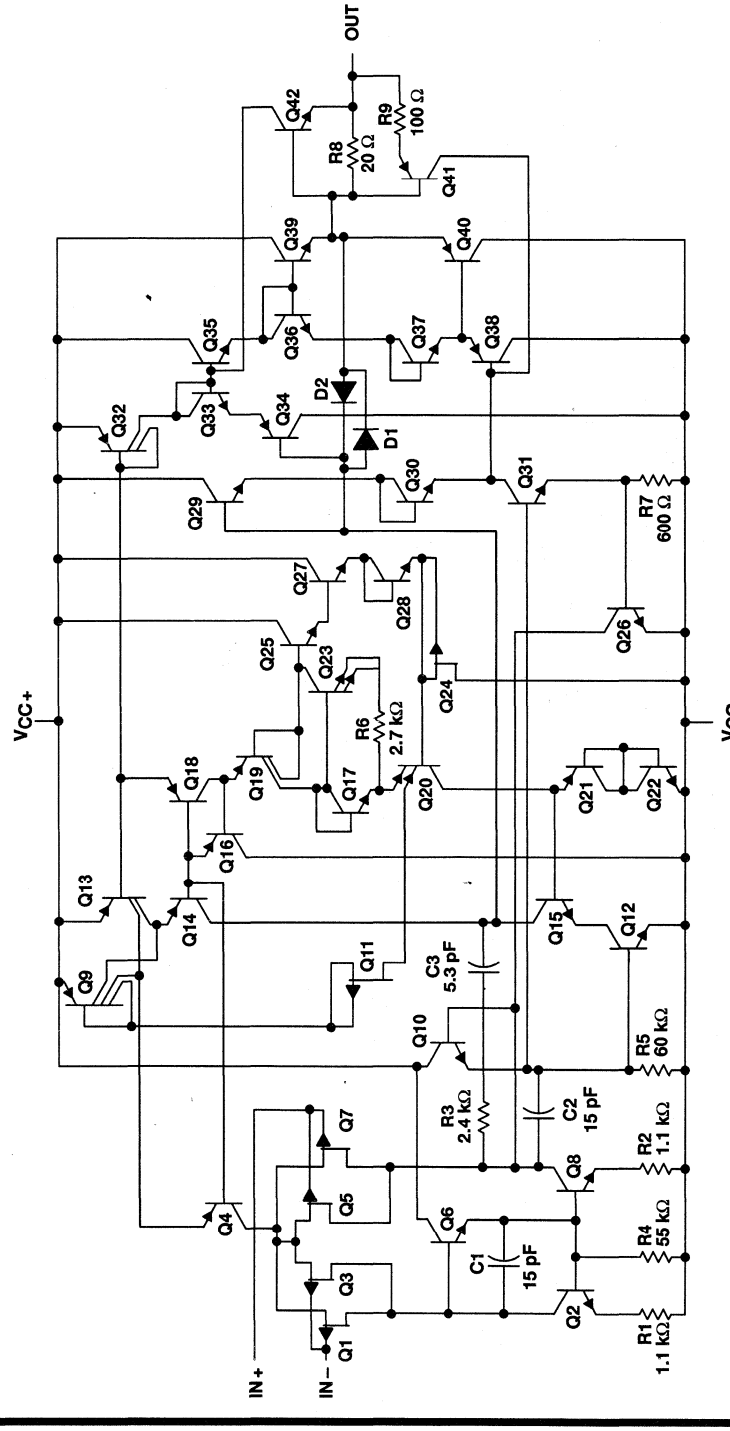


NC – No internal connection

symbol



equivalent schematic (each channel)



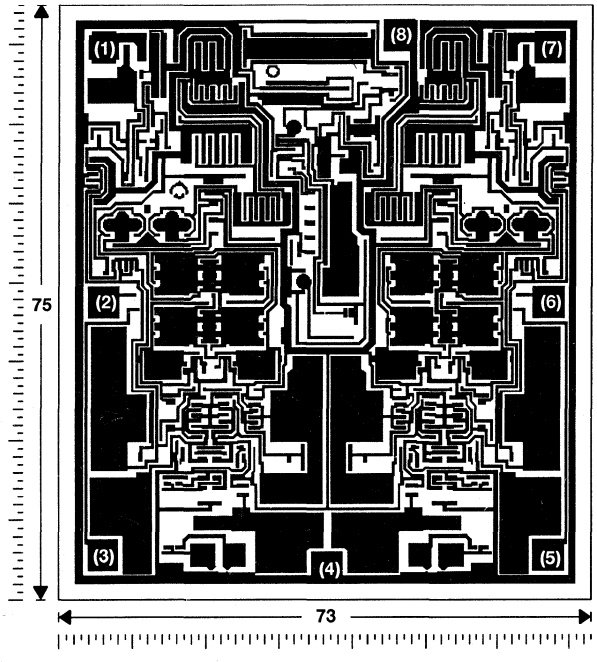
ACTUAL DEVICE COMPONENT COUNT	
Transistors	42
Resistors	9
Diodes	2
Capacitors	3

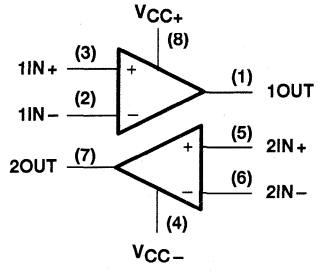
Component values are nominal.

TLE2062Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2062. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} ..... −19 V
Differential input voltage, V_{ID} (see Note 2) ..... ±38 V
Input voltage, V_I (any input) ..... $\pm V_{CC}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	±3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	−1.6	4	−1.6	4	−1.6	4	V
	$V_{CC\pm} = \pm 15$ V	−11	13	−11	13	−11	13	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062C, TLE2062AC, TLE2062BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062C	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			5.9	
		TLE2062AC		25°C		0.9	4	
				Full range			4.9	
		TLE2062BC		25°C		0.7	3	
				Full range			3.9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.3			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		560	620	μA
			Full range			635	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		26		μA

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.2	3.4		V/μs
			Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, A_{VD} = 2, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω, C_L = 100 pF	25°C		1.3		
	Settling time	0.1%	25°C		5		μs
		0.01%	25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		58°		
		R_L = 100 Ω, C_L = 100 pF	25°C		75°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062C	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			4.9	
		TLE2062AC		25°C		0.8	2	
				Full range			2.9	
		TLE2062BC		25°C		0.5	1	
				Full range			1.9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0 V, No load	25°C		625	690	μA
			Full range			715	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		36		μA

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 10 0 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062I	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			6.3	
		TLE2062AI		25°C		0.9	4	
				Full range			5.3	
		TLE2062BI		25°C		0.7	3	
				Full range			4.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.1			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.1			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		560	620	μA
			Full range			640	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		54		μA

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.2	3.4		V/μs
			Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, A_{VD} = 2, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω, C_L = 100 pF	25°C		1.3		
	Settling time	0.1%	25°C		5		μs
		0.01%	25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		58°		
		R_L = 100 Ω, C_L = 100 pF	25°C		75°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062I	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			5.3	
		TLE2062AI		25°C		0.8	2	
				Full range			3.3	
		TLE2062BI		25°C		0.5	1	
				Full range			2.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		625	690	μA
			Full range			720	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		74		μA

† Full range is –40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is –40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER			TEST CONDITIONS	T_A†	TLE2062M, TLE2062AM, TLE2062BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			7	
		TLE2062AM		25°C		0.9	4	
				Full range			6	
		TLE2062BM		25°C		0.7	3	
				Full range			5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
		FK and JG packages	R_L = 600 Ω	25°C	2.5	3.6		
				Full range	2			
		D and P packages	R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.5	−3.9		V
				Full range	−3			
		FK and JG packages	R_L = 600 Ω	25°C	−2.5	−3.5		
				Full range	−2			
		D and P packages	R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to −2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			
		D and P packages	V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω,	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current (two amplifiers)	V_O = 0, No load	25°C		560	620	μA
			Full range			650	
ΔI_{CC}	Supply-current change over operating temperature range (two amplifiers)		Full range		72		μA

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, T_A = 25°C, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		59		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		1.8		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.3		
	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		58°		
		R_L = 600 Ω,	C_L = 100 pF		75°		

† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062M, TLE2062AM, TLE2062BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			6	
		TLE2062AM		25°C		0.8	2	
				Full range			4	
		TLE2062BM		25°C		0.5	1	
				Full range			3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13	13.7		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	11			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13	−13.7		V
				Full range	−12.5			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−11			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	7			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		625	690	μA
			Full range			730	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		97		μA

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is −55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

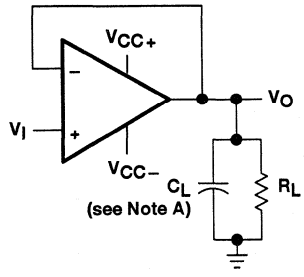
PARAMETER		TEST CONDITIONS		TLE2062Y MIN	TLE2062Y TYP	TLE2062Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.9	4	mV
α_{VIO}	Input offset voltage long-term drift (see Note 4)				0.04		μV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		−13.2	−13.7		V
		R_L = 600 Ω		−12.5	−13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V,	R_L = 600 Ω	25	100		
		V_O = 0 to −8 V,	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			560		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		625	690	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2062Y MIN	TLE2062Y TYP	TLE2062Y MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ,	C_L = 100 pF	2.6	3.4	4	V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		2		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.5		
	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		60°		
		R_L = 600 Ω,	C_L = 100 pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

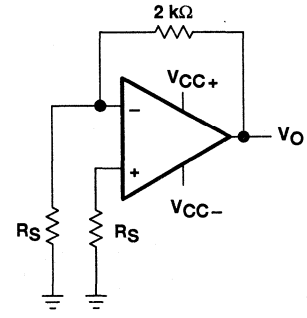
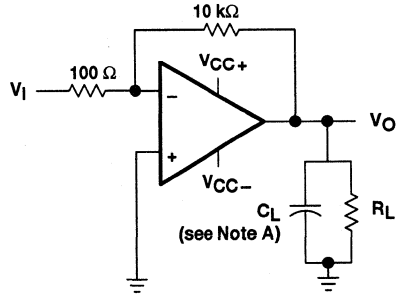


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias offset current

At the picoamp bias current level typical of the TLE2062, TLE2062A, and TLE2062B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode voltage vs Free-air temperature	5 6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{ICR}	Common-mode input voltage range	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage swing	vs Output current vs Supply voltage	8,9 10,11,12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13,14
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	15 16
I_{OS}	Short-circuit output current	vs Time vs Free-air temperature	17 18
z_o	Output impedance	vs Frequency	19
CMRR	Common-mode rejection ratio	vs Frequency	20
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	21 22
	Pulse response	Small signal Large signal	23,24 25,26
	Noise voltage (referred to input)	0.1 to 10 Hz	27
V_n	Equivalent input noise voltage	vs Frequency	28
THD	Total harmonic distortion	vs Frequency	29,30
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	31 32
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	33 34 35
	Phase shift	vs Frequency	15

TYPICAL CHARACTERISTICS†

**TLE2062
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

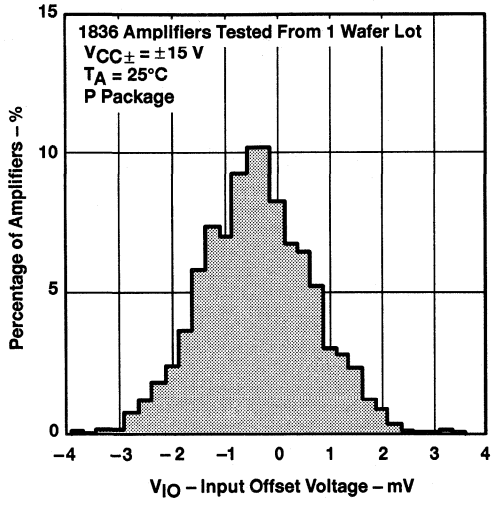


Figure 4

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

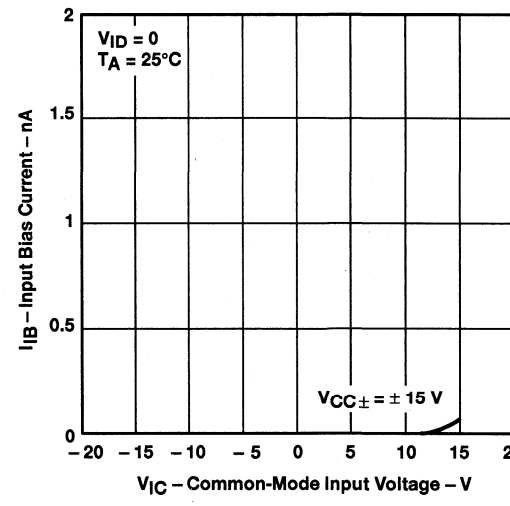


Figure 5

**INPUT BIAS CURRENT
AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

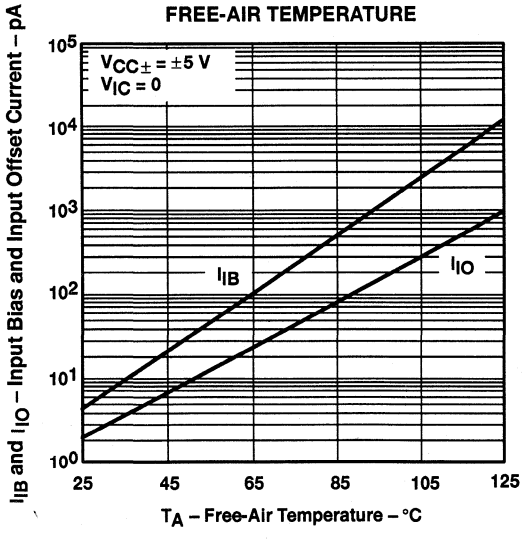


Figure 6

**COMMON-MODE INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

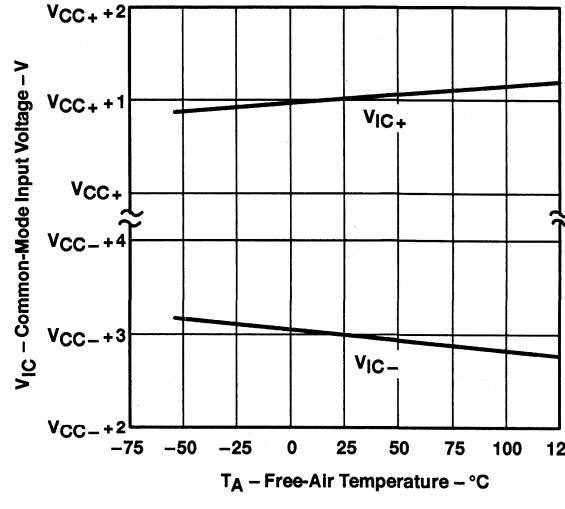


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

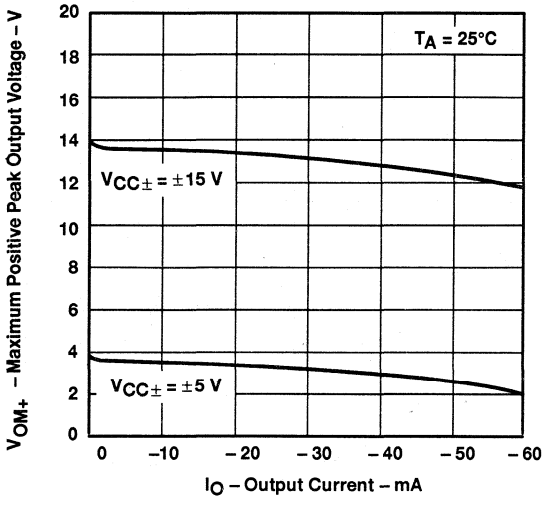


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

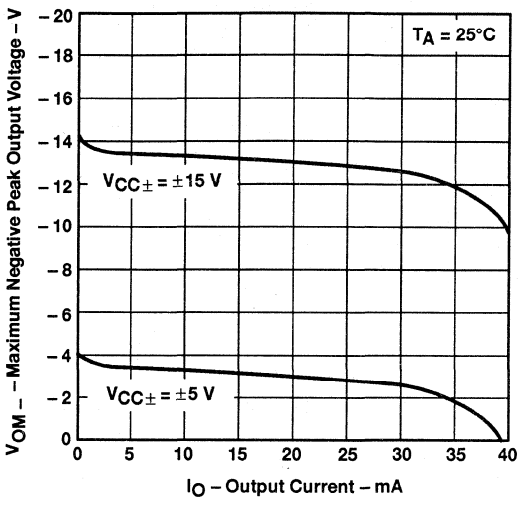


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

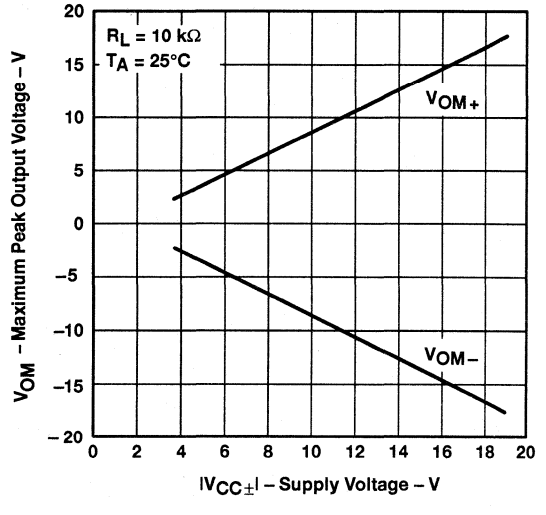


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

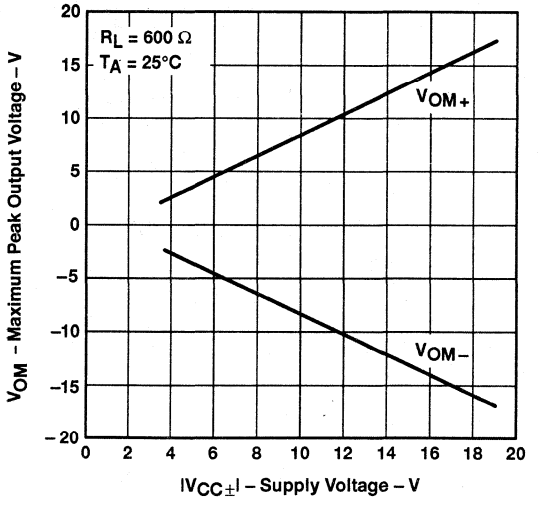


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

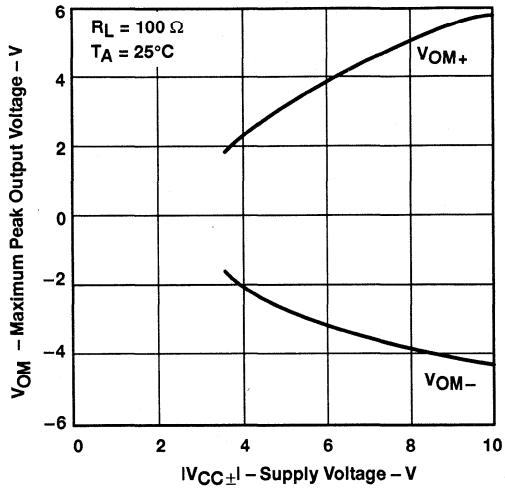


Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

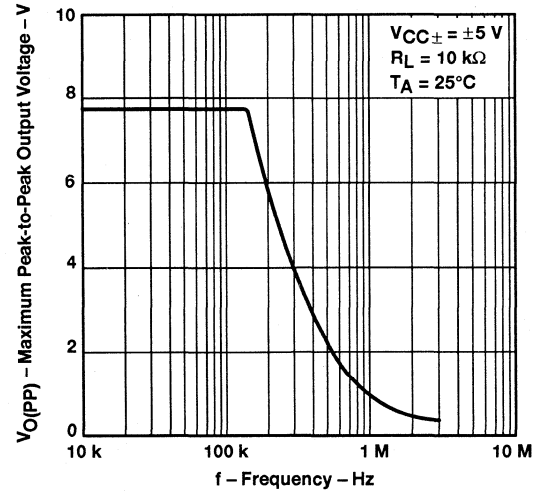


Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

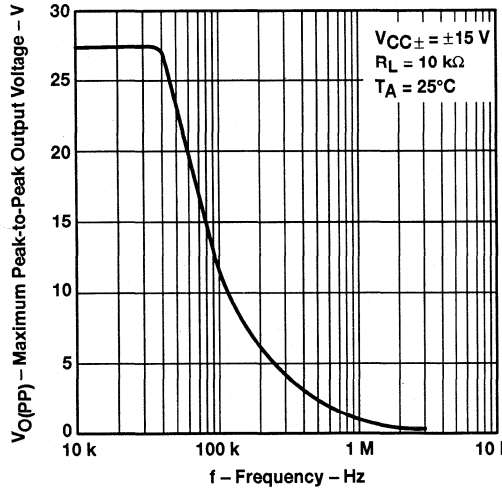


Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

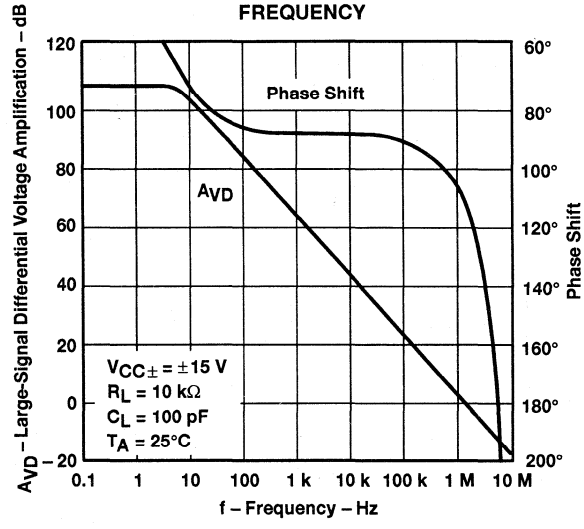


Figure 15

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

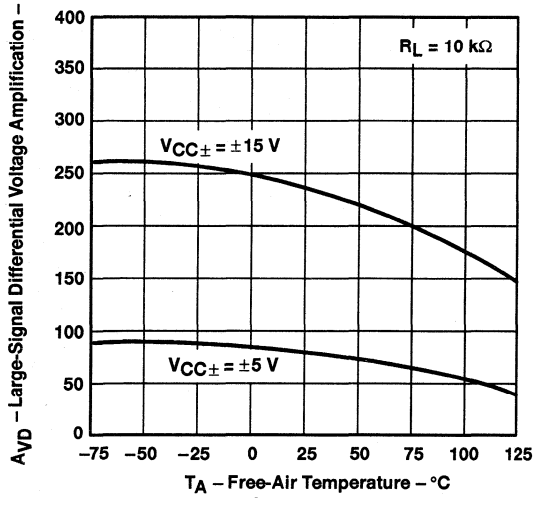


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

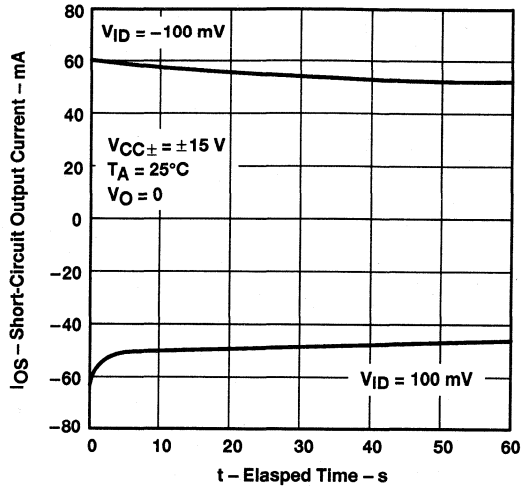


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

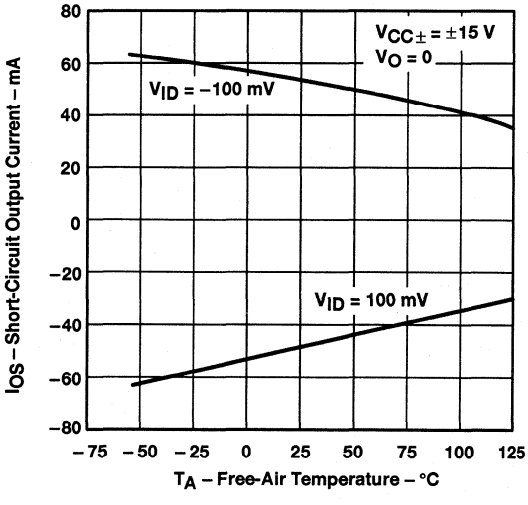


Figure 18

OUTPUT IMPEDANCE vs FREQUENCY

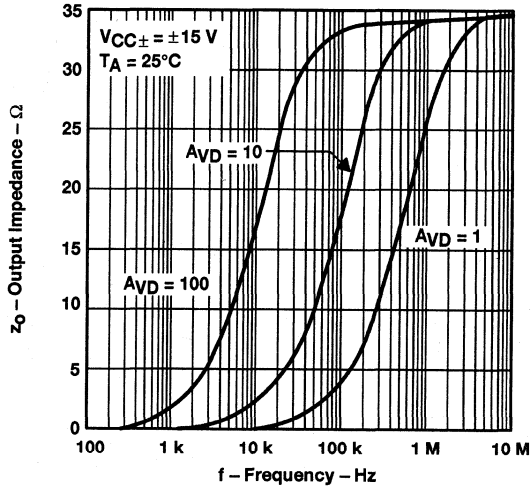


Figure 19

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

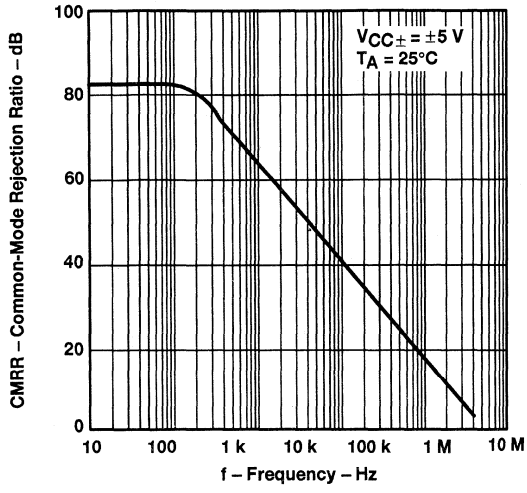


Figure 20

SUPPLY CURRENT vs SUPPLY VOLTAGE

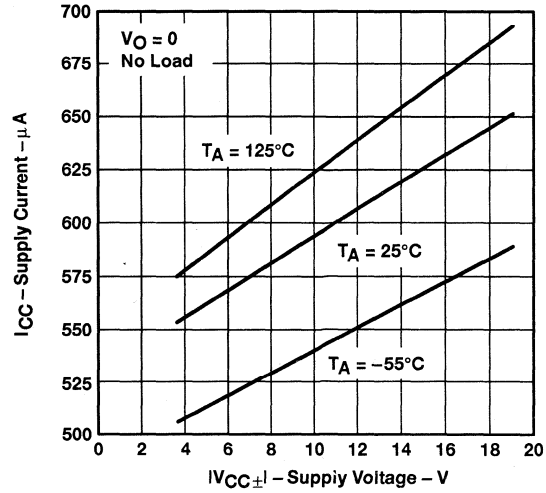


Figure 21

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

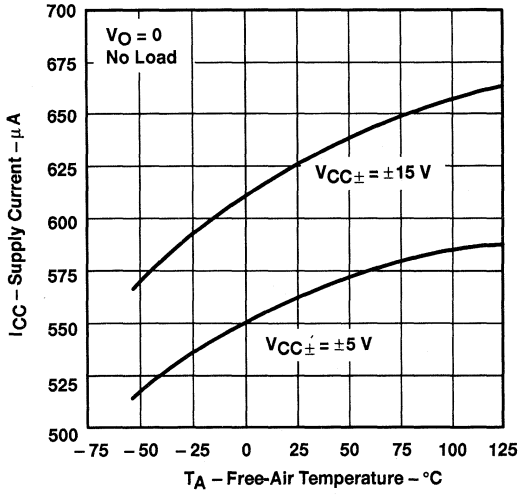


Figure 22

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

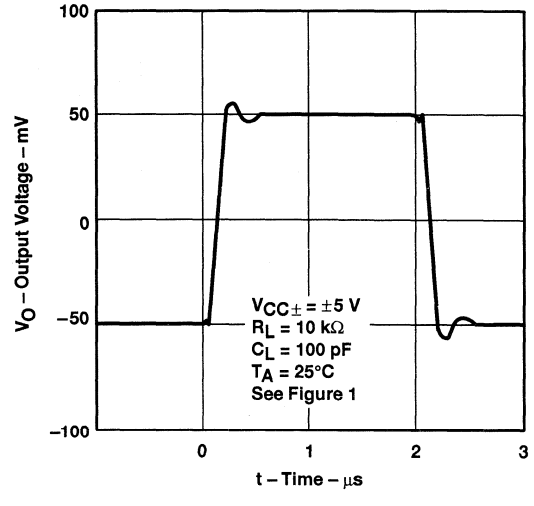


Figure 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

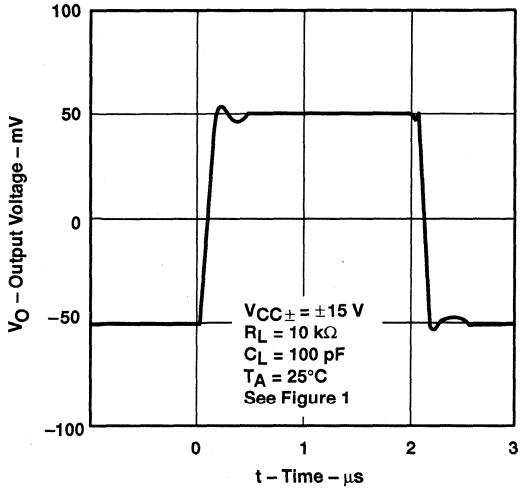


Figure 24

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

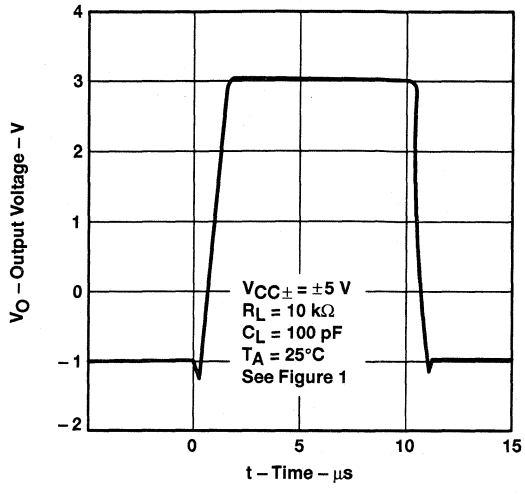


Figure 25

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

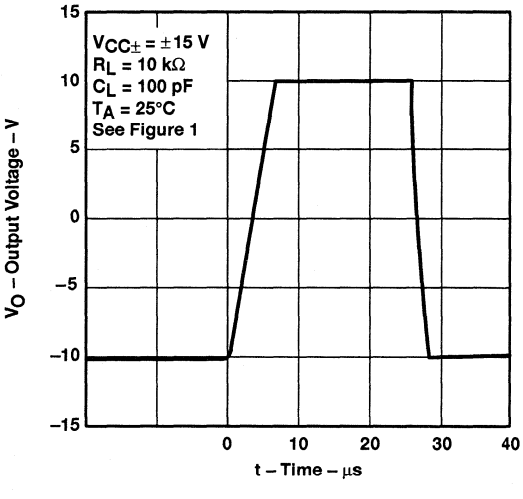


Figure 26

NOISE VOLTAGE
(REFERRED TO INPUT)
0.1 TO 10 Hz

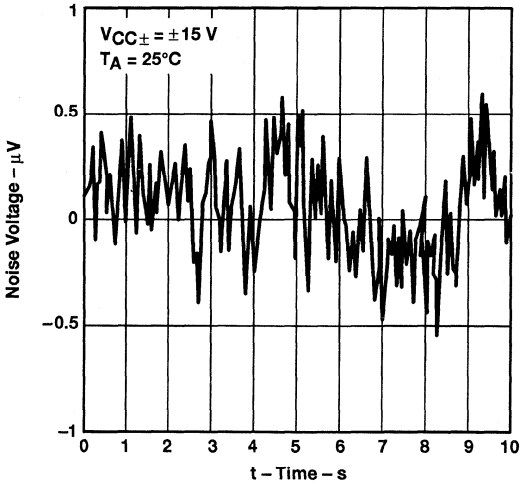


Figure 27

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

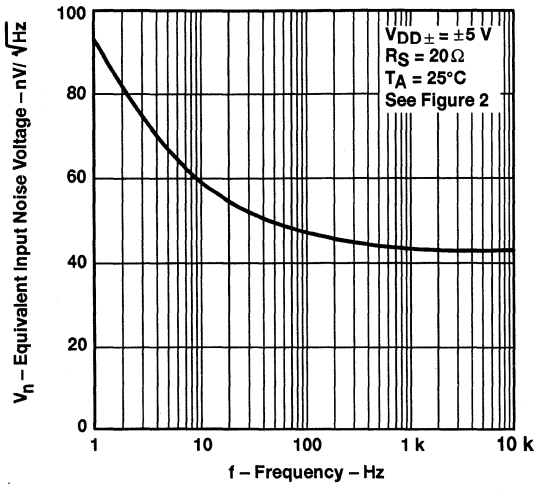


Figure 28

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

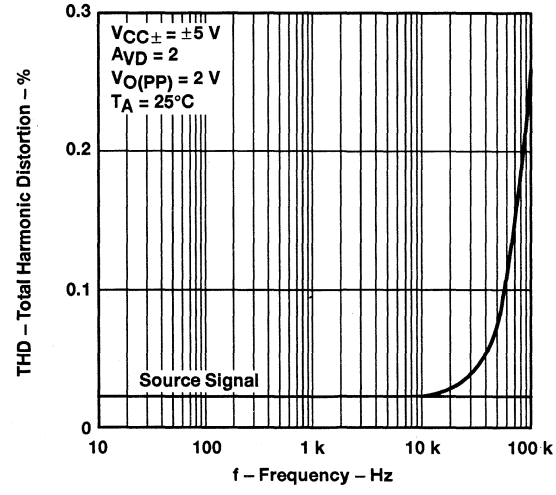


Figure 29

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

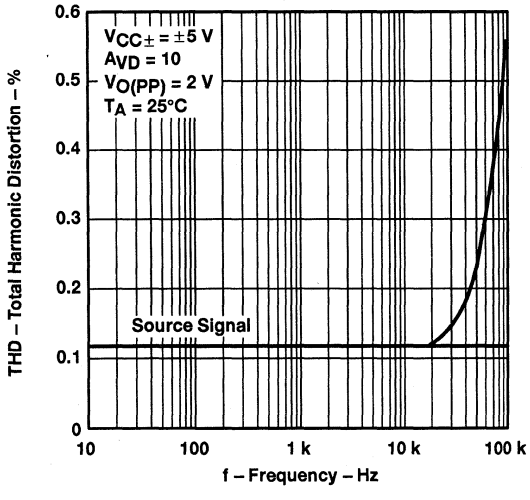


Figure 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

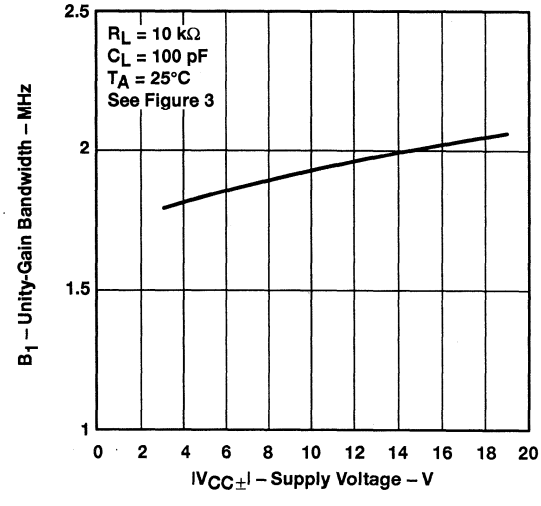


Figure 31

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

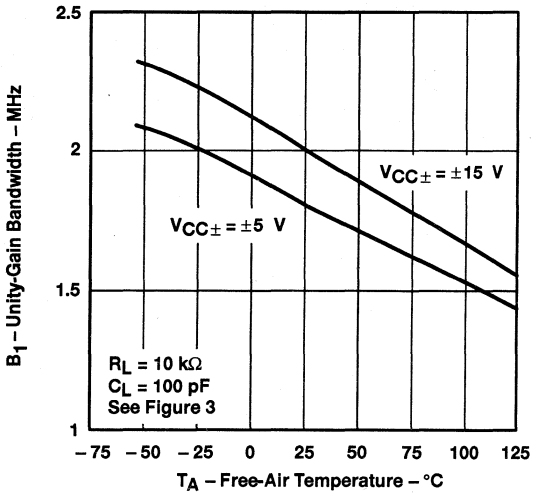


Figure 32

PHASE MARGIN vs SUPPLY VOLTAGE

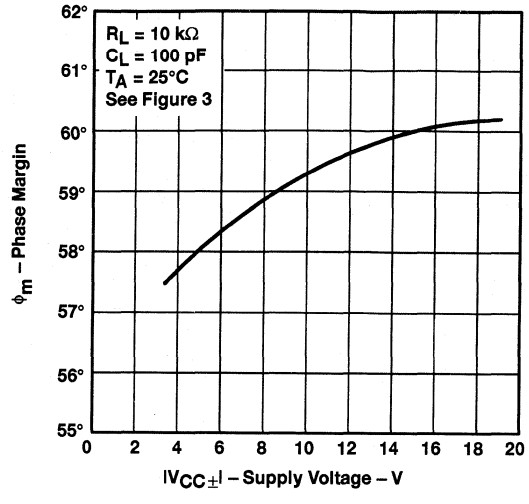


Figure 33

PHASE MARGIN vs LOAD CAPACITANCE

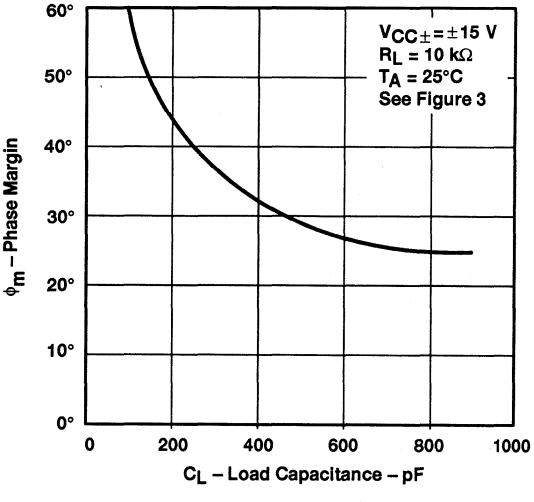


Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

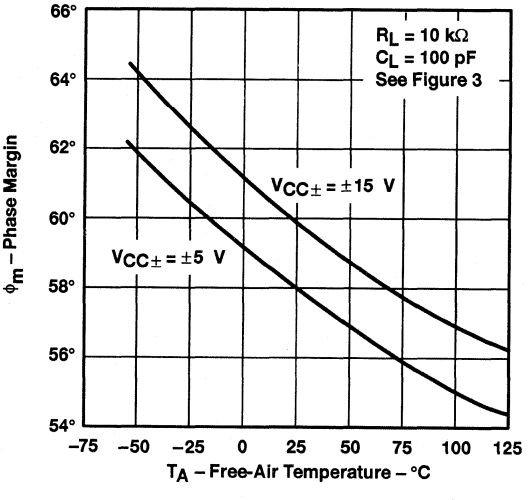


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input characteristics

The TLE2062, TLE2062A, and TLE2062B are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TLE2062, TLE2062A, and TLE2062B are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

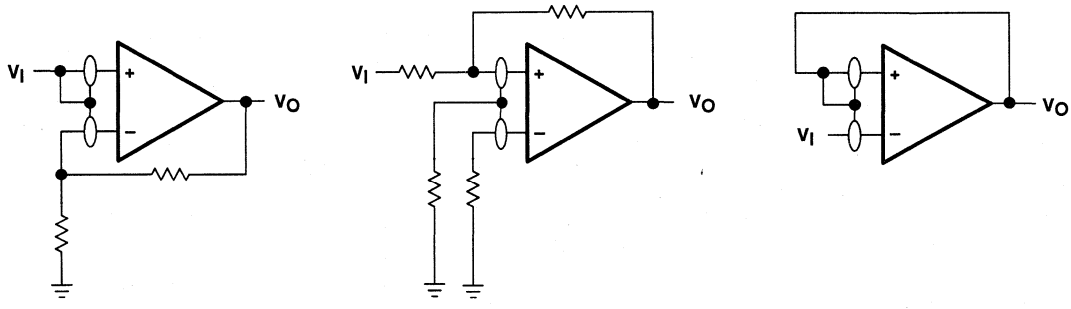


Figure 36. Use of Guard Rings

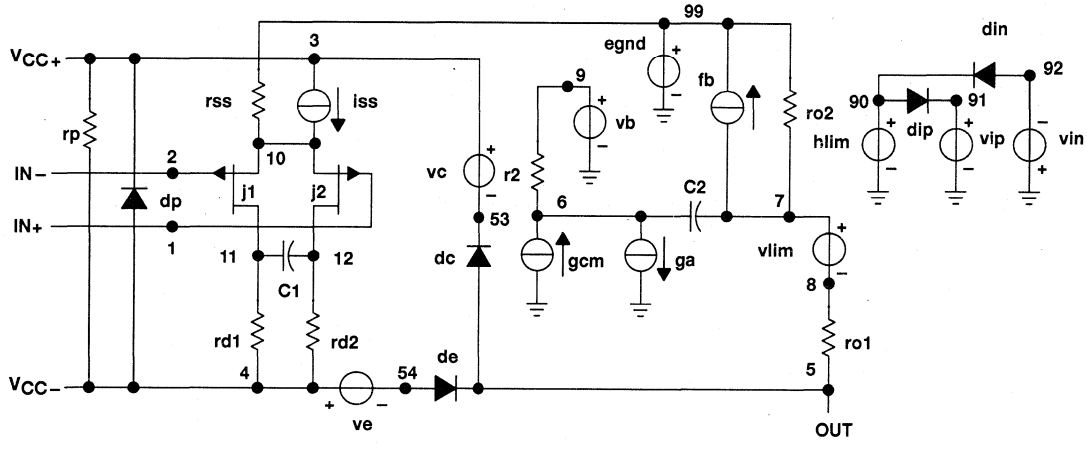
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 37 were generated using the TLE2062 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.subckt TLE2062 1 2 3 4 5
  c1   11  12 1.457E-12
  c2    6   7 15.00E-12
  dc    5  53 dx
  de   54   5 dx
  dlp  90  91 dx
  dln  92  90 dx
  dp    4   3 dx
  egnd 99   0 poly (2) (3,0) (4,0) 0 .5 .5
  fb    7  99 poly (5) vb vc ve vlp
+  vln 0 4.357E6 -4E6 4E6 4E6 -4E6
  ga    6   0 11 12 188.5E-6
  gcm   0   6 10 99 3.352E-9
  iss   3  10 dc 51.00E-6
  hlim 90   0 vlim 1k
  j1   11   2 10 jx
  j2   12   1 10 jx
  r2    6   9 100.0E3
  rd1   4  11 5.305E3
  rd2   4  12 5.305E3
  r01   8   5 280
  r02   7  99 280
  rp    3   4 113.2E3
  rss  10  99 3.922E6
  vb    9   0 dc 0
  vc    3  53 dc 2
  ve   54   4 dc 2
  vlim  7   8 dc 0
  vlp  91   0 dc 50
  vln   0  92 dc 50
.model dx  D(Is=800.0E-18)
.model jx  PJF(Is=2.000E-12 Beta = 423E-6
+ Vto = -1)
.ends
```

Figure 37. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation

- **Excellent Output Drive Capability**
  V_O = ±2.5 V Min at R_L = 100 Ω,
  $V_{CC±}$ = ±5 V
  V_O = ±12.5 V Min at R_L = 600 Ω,
  $V_{CC±}$ = ±15 V
- **Low Supply Current . . . 280 μA Typ Per Amplifier**
- **High Unity-Gain Bandwidth . . . 2 MHz Typ**
- **High Slew Rate . . . 3.4 V/μs Typ**
- **Macromodels Included**
- **Wide Operating Supply Voltage Range**
  $V_{CC±}$ = ± 3.5 V to ±19 V
- **High Open-Loop Gain . . . 230 V/mV Typ**
- **Low Offset Voltage . . . 2 mV Max**
- **Low Offset Voltage Drift With Time**
  0.04 μV/mo Typ
- **Low Input Bias Current . . . 4 pA Typ**

description

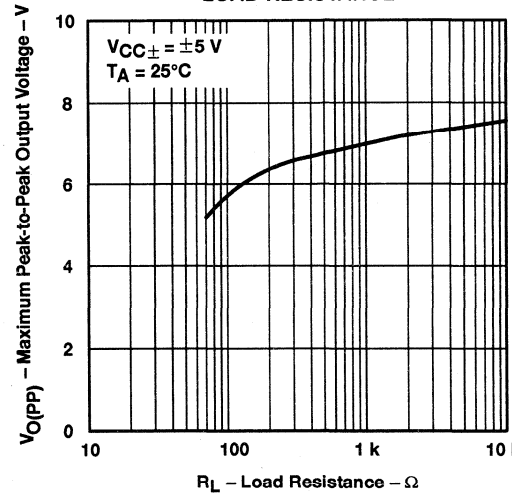
The TLE2064, TLE2064A, and TLE2064B are JFET-input, low-power, precision operational amplifiers manufactured using Texas Instruments Excalibur process. These devices combine outstanding output drive capability with low power consumption, excellent dc precision, and wide bandwidth.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a precision device remaining precise even with changes in temperature and over years of use.

The TLE2064, TLE2064A, and TLE2064B are ideal choices for any application requiring excellent dc precision, high output drive, wide bandwidth, and low power consumption.

A variety of available package options includes small-outline and chip-carrier versions for high-density system applications.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE



AVAILABLE OPTIONS

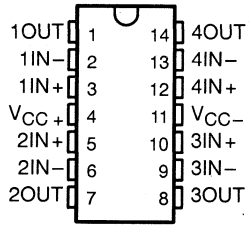
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	CHIP FORM (Y)
0°C to 70°C	2 mV	—	—	—	TLE2064BCN	—
	4 mV	TLE2064ACD			TLE2064ACN	
	6 mV	TLE2064CD			TLE2064CN	
−40°C to 85°C	2 mV	—	—	—	TLE2064BIN	TLE2064Y
	4 mV	TLE2064AID			TLE2064AIN	
	6 mV	TLE2064ID			TLE2064IN	
−55°C to 125°C	2 mV	—	—	TLE2064BMJ	TLE2064BMN	—
	4 mV	TLE2064AMD	TLE2064AMFK	TLE2064AMJ	TLE2064AMN	
	6 mV	TLE2064MD	TLE2064MFK	TLE2064MJ	TLE2064MN	

The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLE2064ACDR).

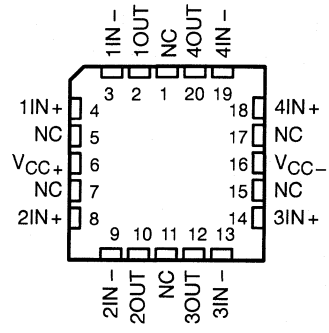
description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

D, J, OR N PACKAGE
(TOP VIEW)

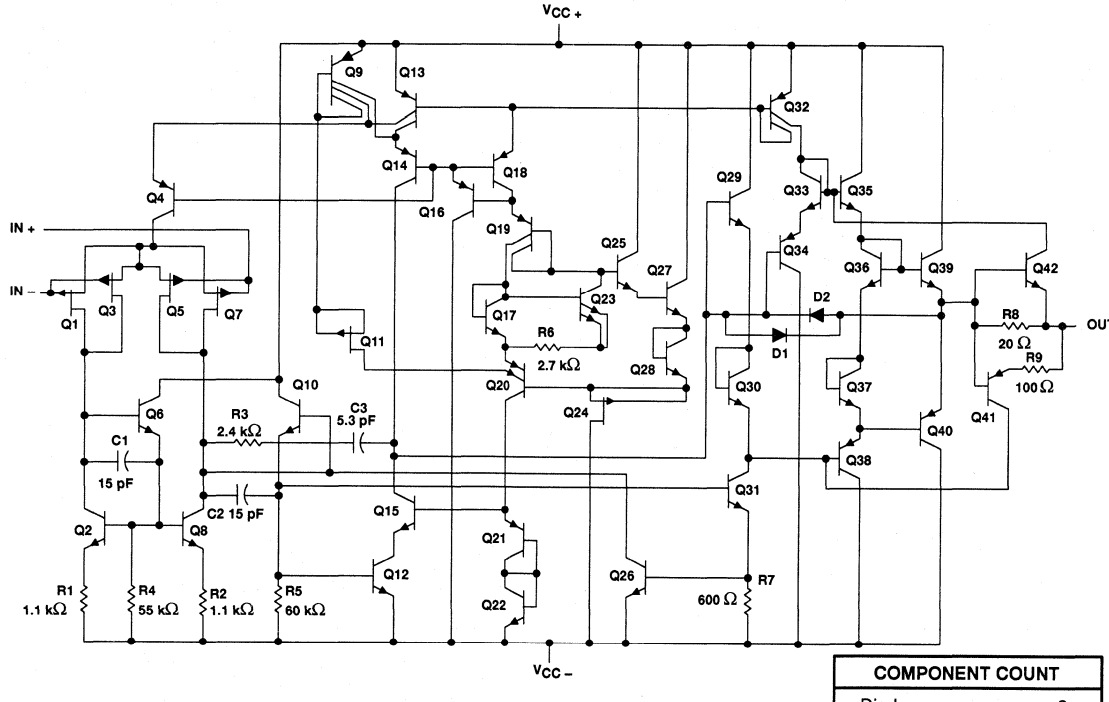


FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic



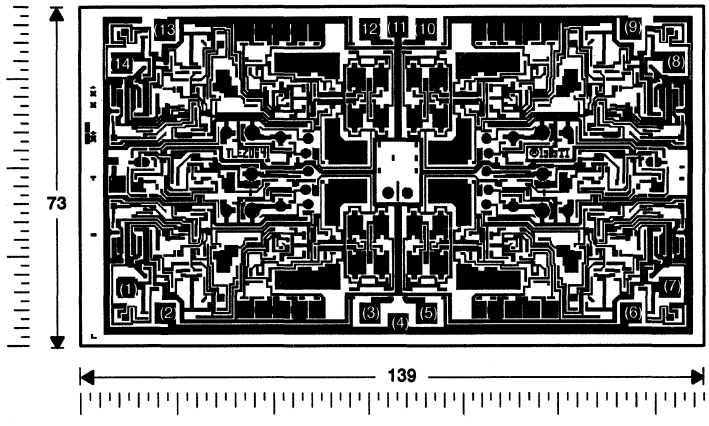
COMPONENT COUNT	
Diodes	2
Capacitors	3
Resistors	9
Transistors	42

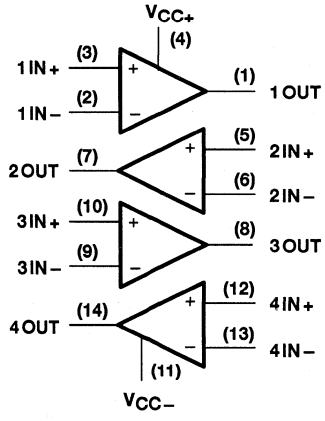
All component values are nominal.

TLE2064Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2064. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} ..... −19 V
Differential input voltage, V_{ID} (see Note 2) ..... ±38 V
Input voltage, V_I (any input) ..... $V_{CC\pm}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	905 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	±3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−1.6	4	−1.6	4	−1.6	4	V
	$V_{CC\pm} = \pm15$ V	−11	13	−11	13	−11	13	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064C	V_{IC} = 0, R_S = 50 Ω	25°C		1.2	7	mV
				Full range			7.9	
		TLE2064AC		25°C		1.2	6	
				Full range			6.9	
		TLE2064BC		25°C		0.8	3.5	
				Full range			4.4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.3			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		52		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064C, TLE2064AC, TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064C	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	6	mV
				Full range			6.9	
		TLE2064AC		25°C		0.9	4	
				Full range			4.9	
		TLE2064BC		25°C		0.7	2	
				Full range			4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		72		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064I	V_{IC} = 0, R_S = 50 Ω	25°C		1.2	7	mV
				Full range			8.3	
		TLE2064AI		25°C		1.2	6	
				Full range			7.3	
		TLE2064BI		25°C		0.8	3.5	
				Full range			4.8	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.1			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.1			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		108		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is –40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064I	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	6	mV
				Full range			7.3	
		TLE2064AI		25°C		0.9	4	
				Full range			5.3	
		TLE2064BI		25°C		0.7	2	
				Full range			3.3	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		148		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is – 40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064M, TLE2064AM, TLE2064BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064M	V_{IC} = 0, R_S = 50 Ω	25°C		1.2	7	mV
				Full range			9	
		TLE2064AM		25°C		1.2	6	
				Full range			8	
		TLE2064BM		25°C		0.8	3.5	
				Full range			5.5	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
		FK and J packages	R_L = 600 Ω	25°C	2.5	3.6		
				Full range	2			
		D and N packages	R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.5	−3.9		V
				Full range	−3			
		FK and J packages	R_L = 600 Ω	25°C	−2.5	−3.5		
				Full range	−2			
		D and N packages	R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and J packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to −2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) continued)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	D and N packages	V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		V/mV
				Full range	0.25			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.4	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current (four amplifiers)		V_O = 0, No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		144		μA
V_{O1}/V_{O2}	Crosstalk attenuation		A_{VD} = 1000, f = 1 kHz	25°C		120		dB

† Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2064M TLE2064AM TLE2064BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		59		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		1.8		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.3		
t_s	Settling time	ε = 0.1%			5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		58°		
		R_L = 600 Ω,	C_L = 100 pF		75°		

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064M, TLE2064AM, TLE2064BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064M	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	6	mV
				Full range			8	
		TLE2064AM		25°C		0.9	4	
				Full range			6	
		TLE2064BM		25°C		0.7	2	
				Full range			4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13	13.7		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13	−13.7		V
				Full range	−12.5			
			R_L = 600 Ω	25°C	−13	−13		
				Full range	−12.5			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	7			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		194		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is – 55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is – 55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

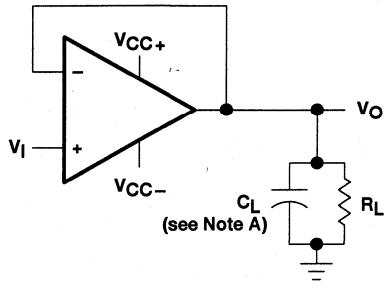
PARAMETER		TEST CONDITIONS		TLE2064Y MIN	TLE2064Y TYP	TLE2064Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.9	6	mV
α_{VIO}	Input offset voltage long-term drift (see Note 4)				0.04		μV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		−13.2	−13.7		V
		R_L = 600 Ω		12.5	13		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V,	R_L = 600 Ω	25	100		
		V_O = 0 to −8 V,	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			560		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, V_{IC} = V_{ICR}min,		72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		1.25	1.4	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz		120		dB

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2064Y MIN	TLE2064Y TYP	TLE2064Y MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		2		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.5		
t_s	Settling time	ε = 0.1%			5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		60°		
		R_L = 600 Ω,	C_L = 100 pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

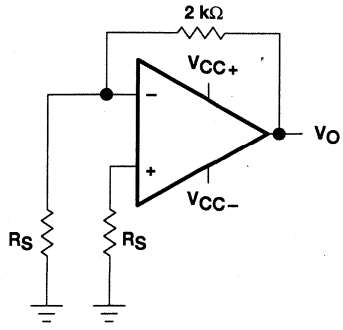
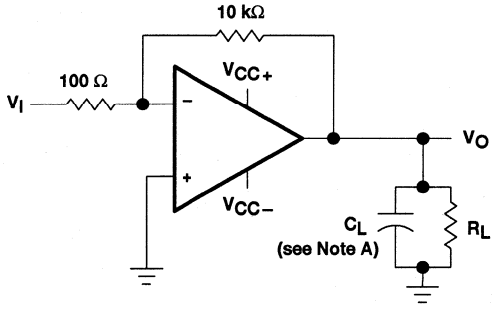


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TLE2064, TLE2064A, and TLE2064B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5 6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{ICR}	Common-mode input voltage	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage	vs Output current vs Supply voltage	8, 9 10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	15 16
I_{OS}	Short-circuit output current	vs Time vs Free-air temperature	17 18
z_o	Output impedance	vs Frequency	19
CMRR	Common-mode rejection ratio	vs Frequency	20
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	21 22
	Pulse response	Small signal Large signal	23, 24 25, 26
	Noise voltage (referred to input)	0.1 to 10 Hz	27
V_n	Equivalent input noise voltage	vs Frequency	28
THD	Total harmonic distortion	vs Frequency	29, 30
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	31 32
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	33 34 35
	Phase shift	vs Frequency	15

TYPICAL CHARACTERISTICS†

**TLE2064
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

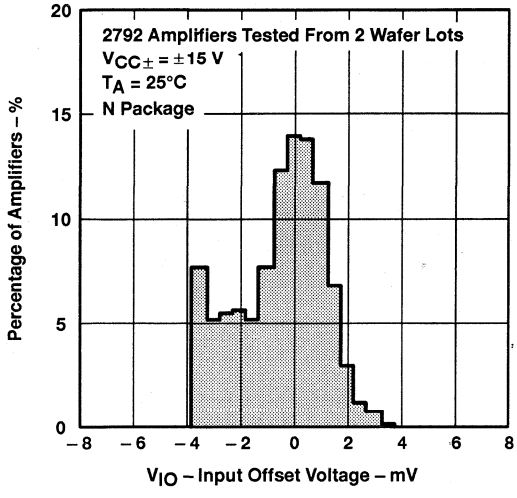


Figure 4

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

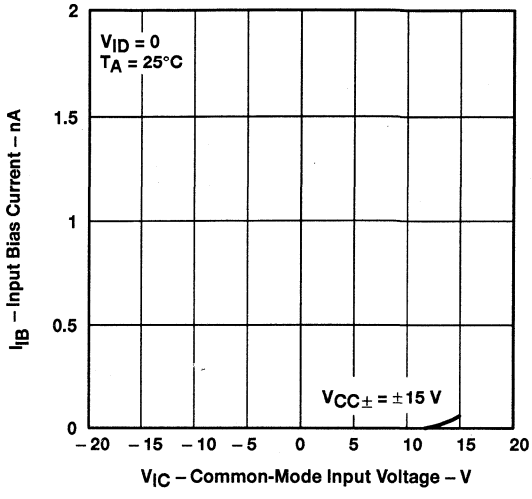


Figure 5

**INPUT BIAS CURRENT
AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

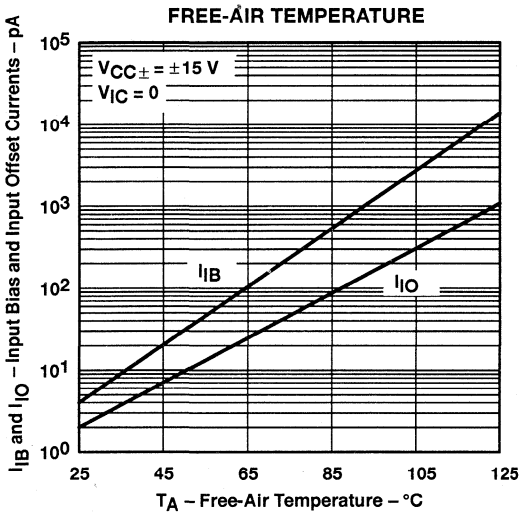


Figure 6

**COMMON-MODE INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

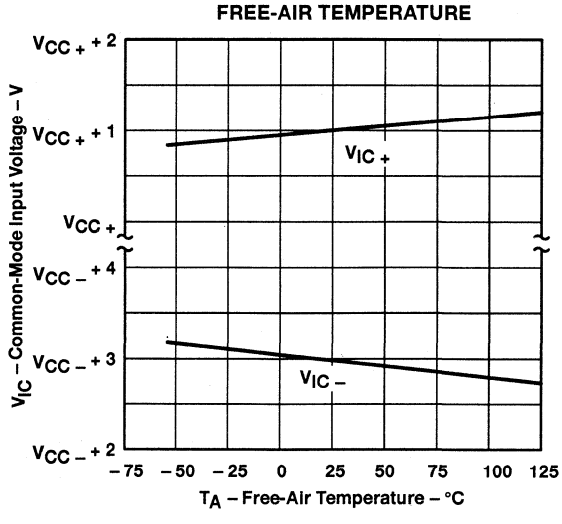


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

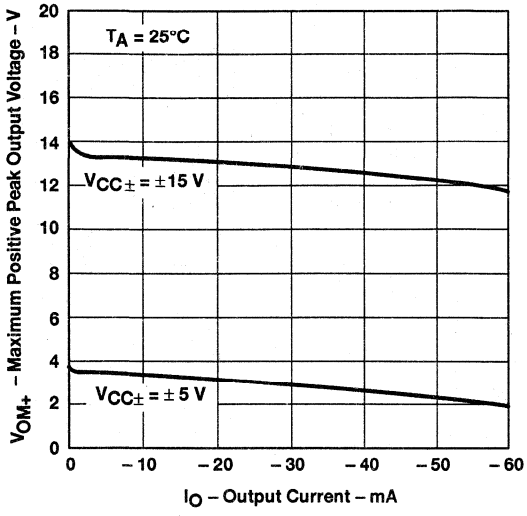


Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

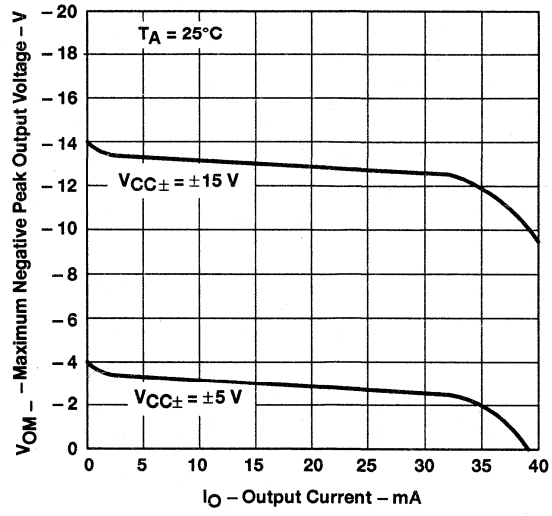


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

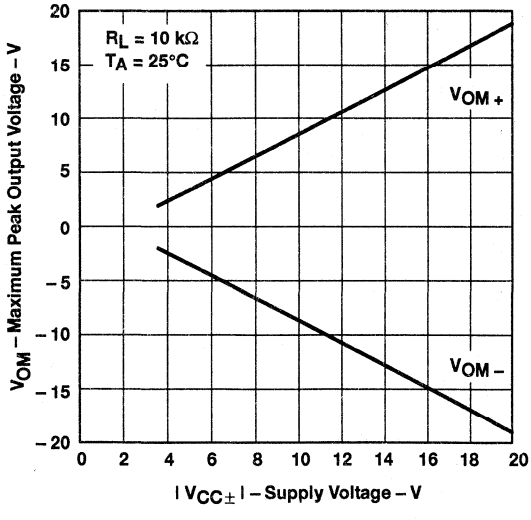


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

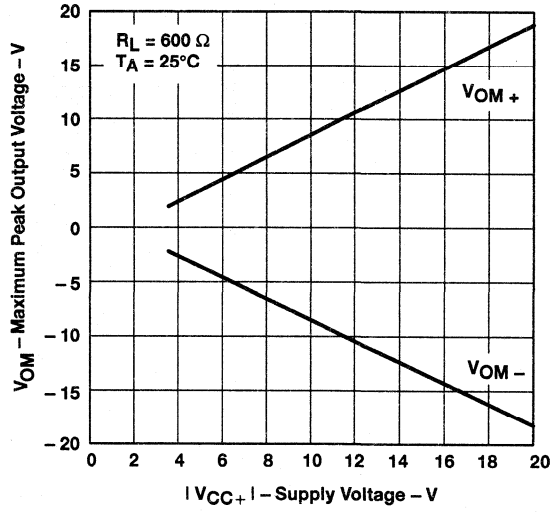


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

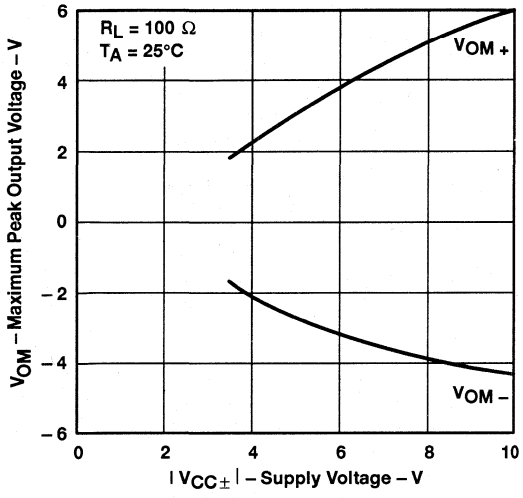


Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

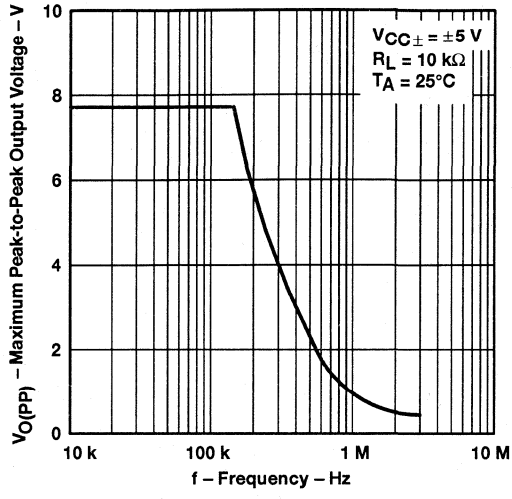


Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

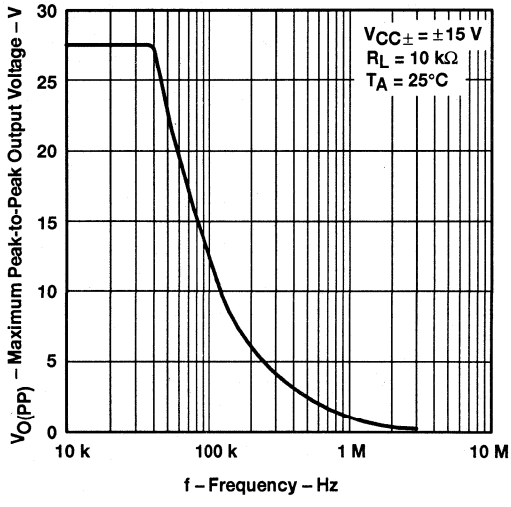


Figure 14

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

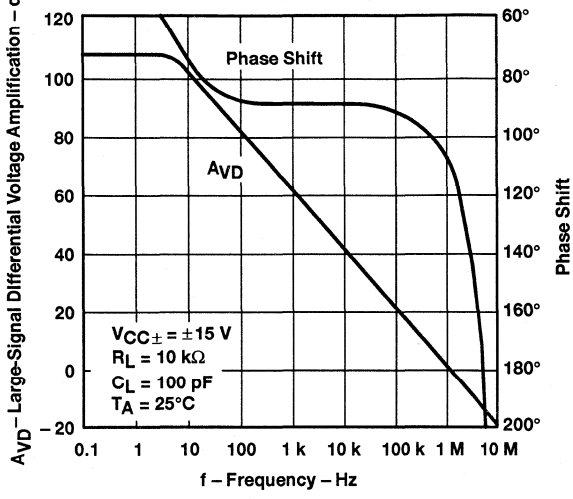


Figure 15

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

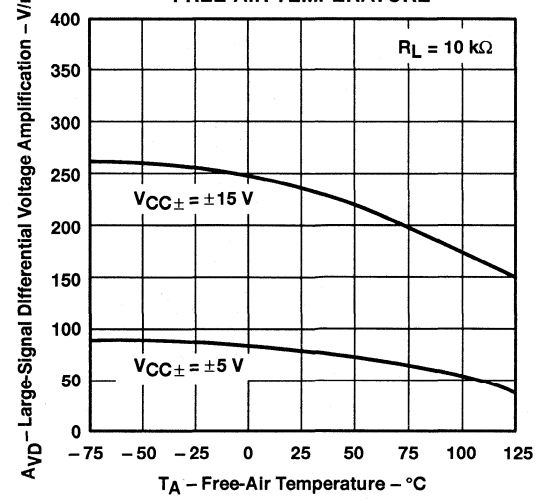


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

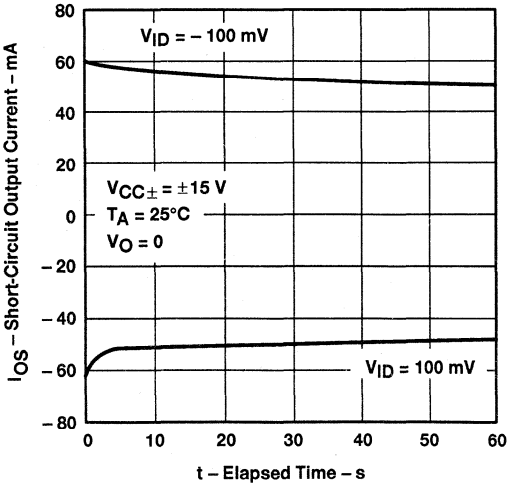


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

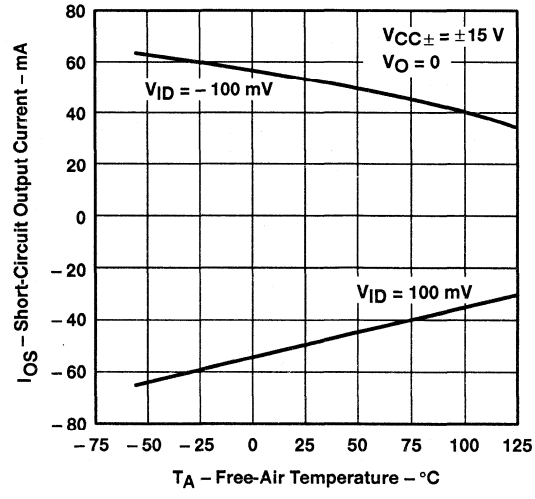


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE vs FREQUENCY

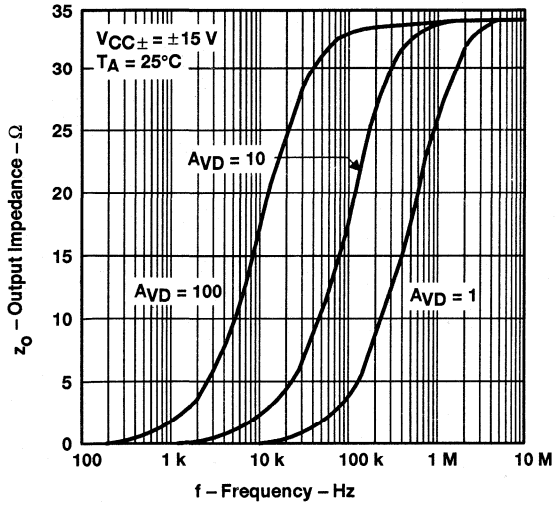


Figure 19

COMMON-MODE REJECTION RATIO vs FREQUENCY

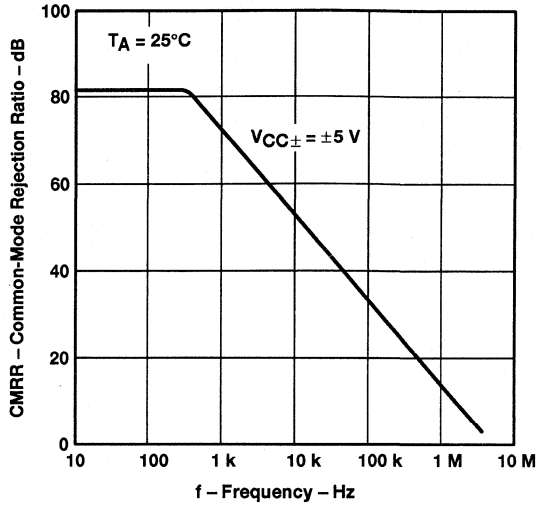


Figure 20

SUPPLY CURRENT vs SUPPLY VOLTAGE

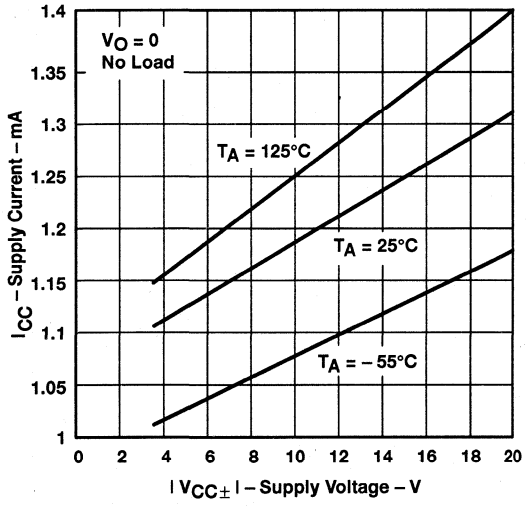


Figure 21

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

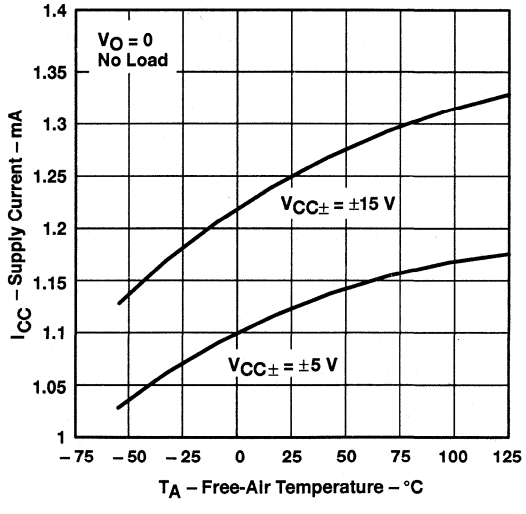


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

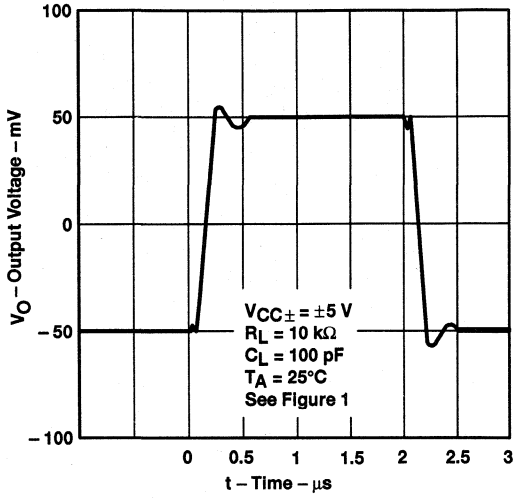


Figure 23

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

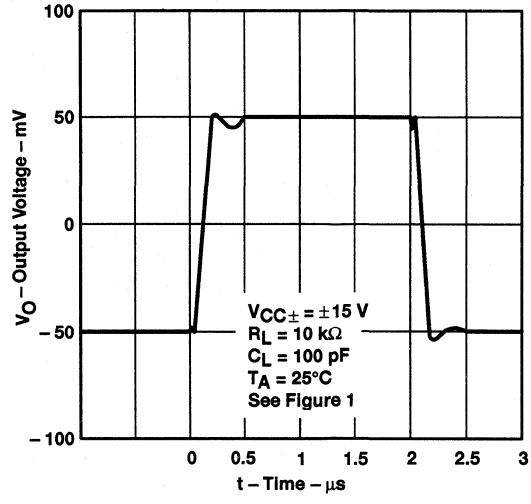


Figure 24

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

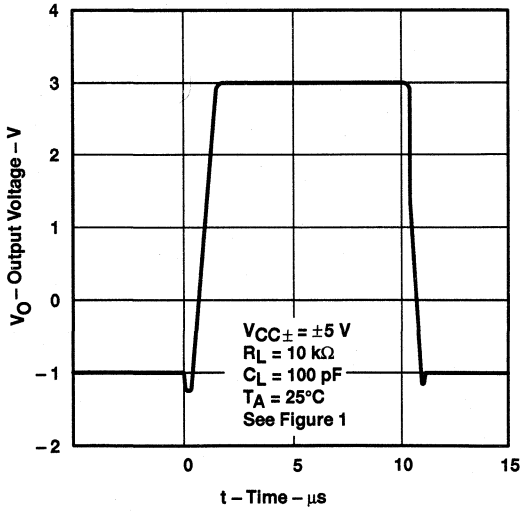


Figure 25

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

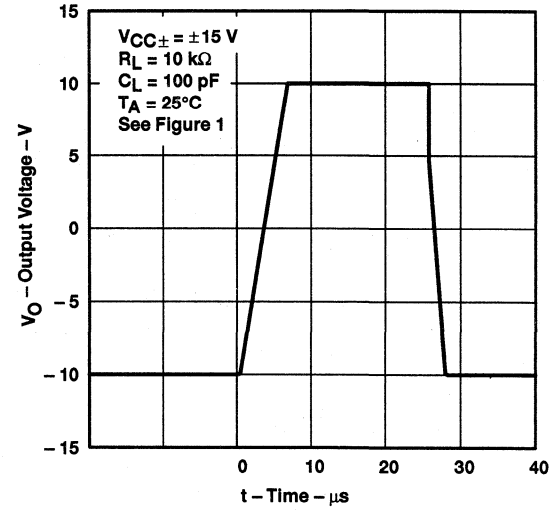


Figure 26

TYPICAL CHARACTERISTICS

NOISE VOLTAGE
(REFERRED TO INPUT)
0.1 TO 10 Hz

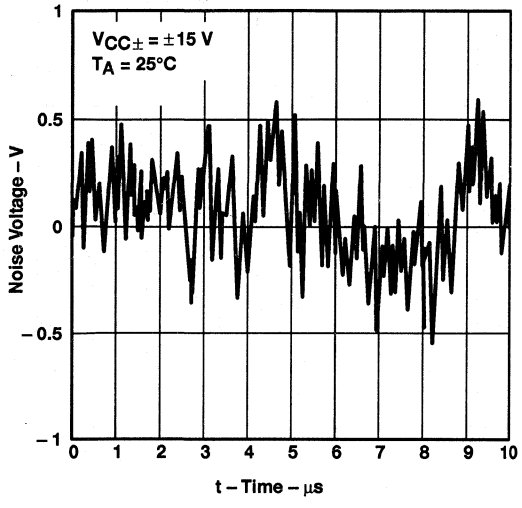


Figure 27

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

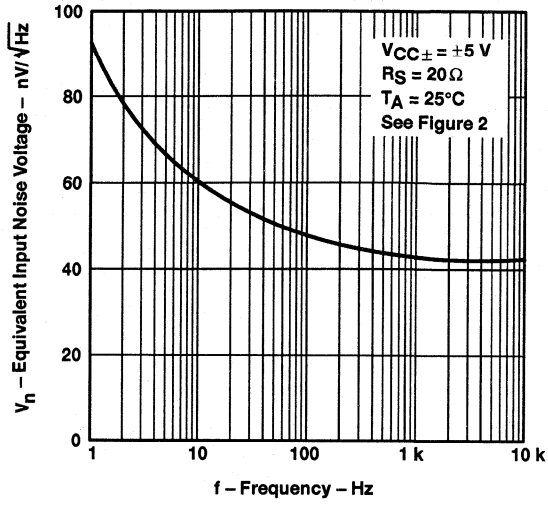


Figure 28

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

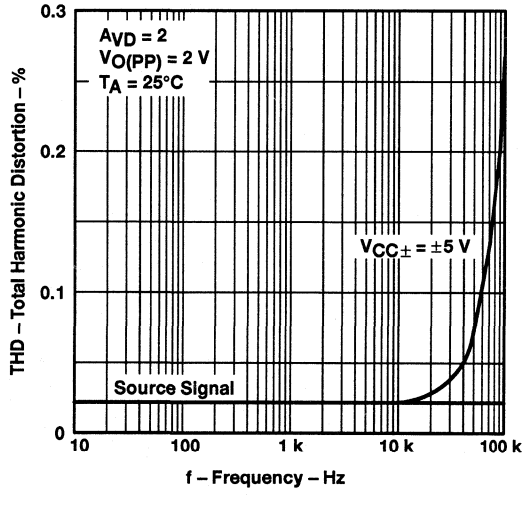


Figure 29

TOTAL HARMONIC DISTORATION
vs
FREQUENCY

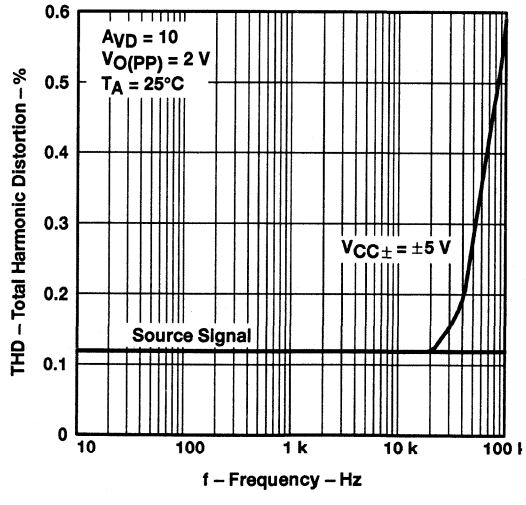


Figure 30

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

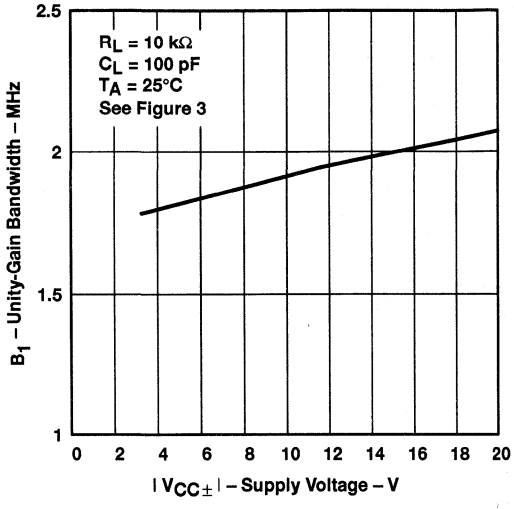


Figure 31

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

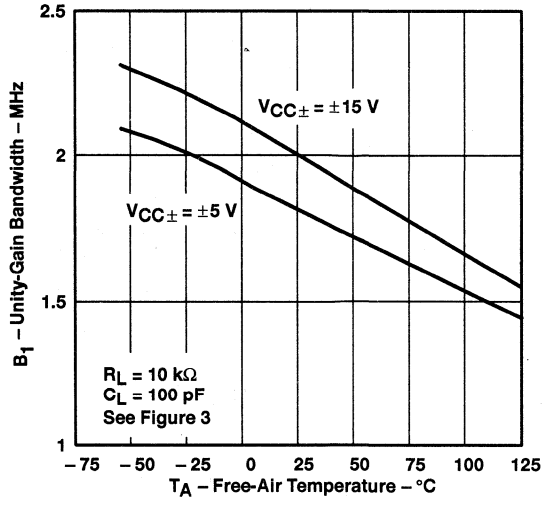


Figure 32

PHASE MARGIN vs SUPPLY VOLTAGE

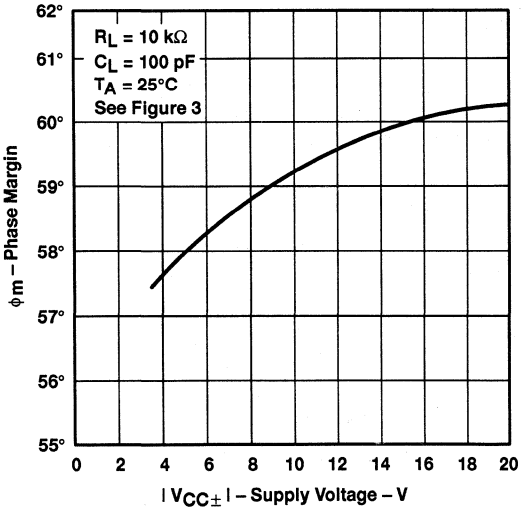


Figure 33

PHASE MARGIN vs LOAD CAPACITANCE

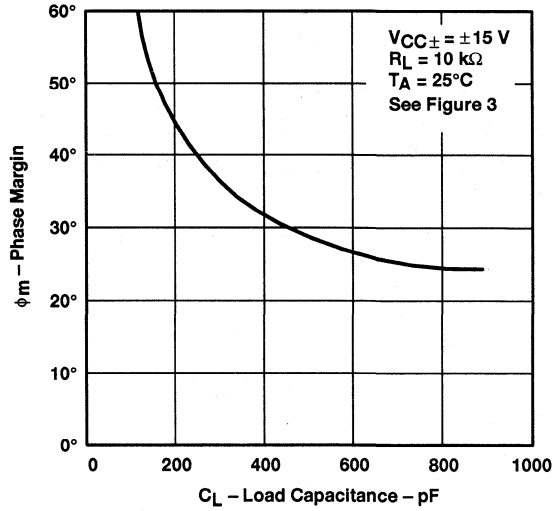


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

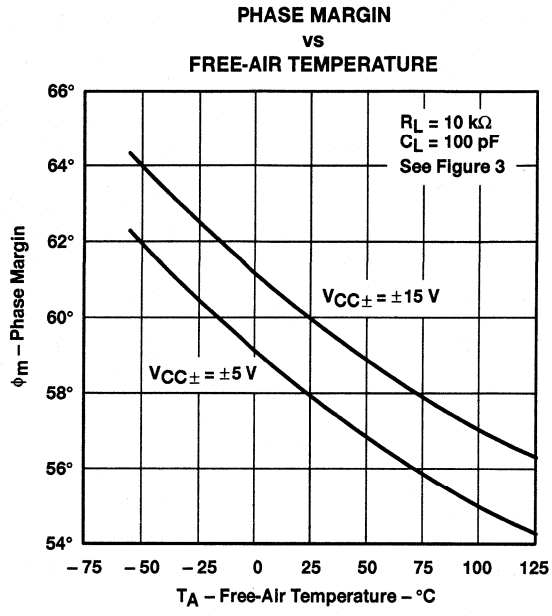


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 36 were generated using the TLE2064 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

To model the TLE2064, TLE2064A, or TLE2064B, use four macromodels in the simulation.

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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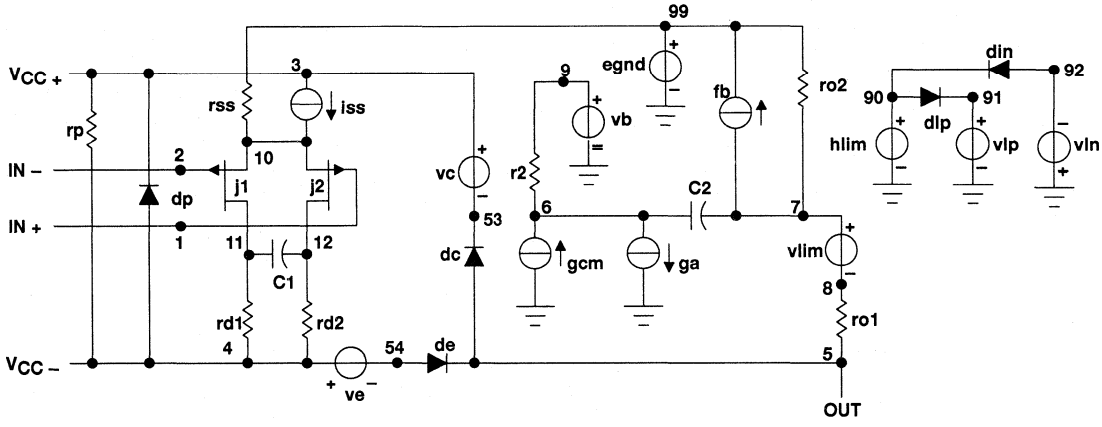
APPLICATION INFORMATION

macromodel information (continued)




```
.subckt TLE2064 1 2 3 4 5
  c1   11   12  1.457E-12
  c2    6    7  15.00E-12
  dc    5   53  dx
  de   54    5  dx
  dlp  90   91  dx
  dln  92   90  dx
  dp    4    3  dx
  egnd 99    0  poly(2) (3,0) (4,0) 0 .5 .5
  fb    7   99  poly(5) vb vc ve vlp vln 0 4.357E6  -4E6 4E6 4E6 -4E6
  ga    6    0  11 12 188.5E-6
  gcm   0    6  10 99 3.352E-9
  iss   3   10  dc 51.00E-6
  hlim 90    0  vlim 1K
  j1   11    2  10 jx
  j2   12    1  10 jx
  r2    6    9  100.0E3
  rd1   4   11  5.305E3
  rd2   4   12  5.305E3
  ro1   8    5  280
  ro2   7   99  280
  rp    3    4  113.2E3
  rss  10   99  3.922E6
  vb    9    0  dc 0
  vc    3   53  dc 2
  ve   54    4  dc 2
  vlim  7    8  dc 0
  vlp  91    0  dc 50
  vln   0   92  dc 50
.model dx D(Is=800.0E-18)
.model jx PJF(Is=2.000E-12 Beta=423E-6 Vto=-1)
.ends
```

Figure 36. Boyle Macromodel and Subcircuit

APPLICATION INFORMATION

Input characteristics

The TLE2064, TLE2064A, and TLE2064B are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TLE2064, TLE2064A, and TLE2064B are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 37). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

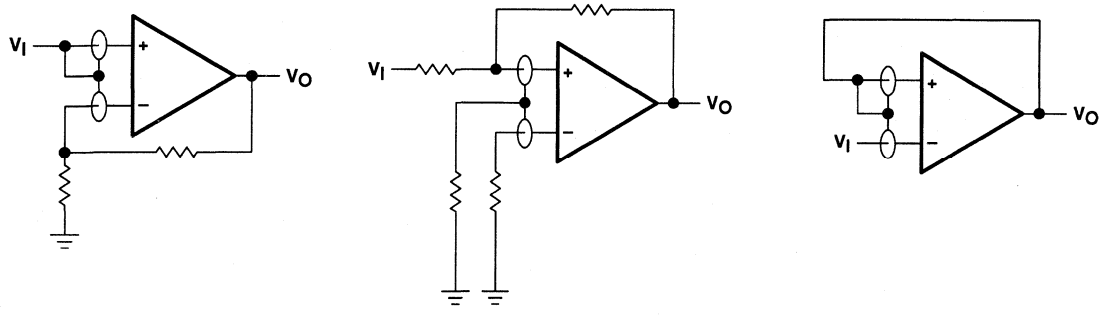
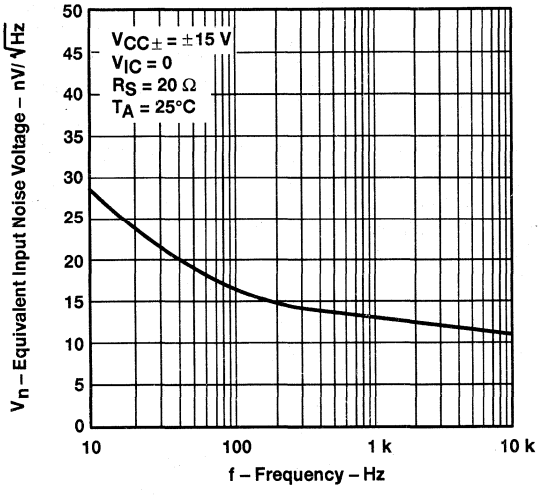


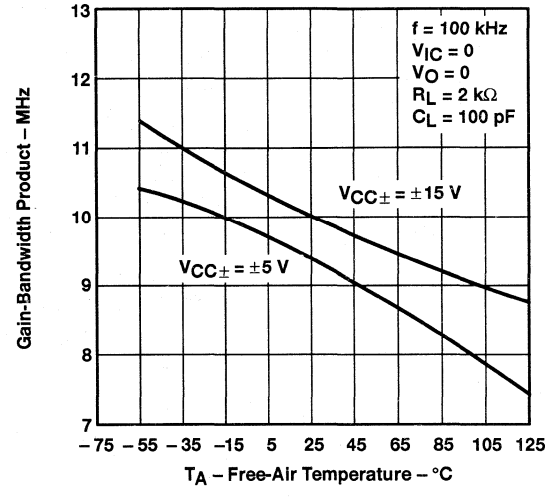
Figure 37. Use of Guard Rings

- 40-V/μs Slew Rate Typ
- Low Noise
  17 nV/√Hz Max at f = 10 kHz
  11.6 nV/√Hz Typ at f = 10 kHz
- High Gain-Bandwidth Product . . . 10 MHz
- ±30-mA Minimum Short-Circuit Output Current
- Wide Supply Range . . . ±2.25 V to ±19 V
- Input Range Includes the Positive Supply
- Macromodel Included
- Fast Settling Time Using 10-V Step
  400 ns to 10 mV Typ
  1.5 μs to 1 mV Typ

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE



description

The TLE2071 and TLE2071A are low-noise, high-performance, high-speed, internally compensated JFET-input operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2071 and TLE2071A have maximum noise specifications for designs requiring certain noise limitations. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	2 mV	TLE2071ACD	—	—	TLE2071ACP	—
	4 mV	TLE2071CD	—	—	TLE2071CP	TLE2071Y
–40°C to 85°C	2 mV	TLE2071AID	—	—	TLE2071AIP	—
	4 mV	TLE2071ID	—	—	TLE2071IP	—
–55°C to 125°C	2 mV	—	TLE2071AMFK	TLE2071AMJG	—	—
	4 mV	—	TLE2071MFK	TLE2071MJG	—	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2071ACDR). Chip-form versions are tested at T_A = 25°C. For chip-form orders, contact your local TI sales office.

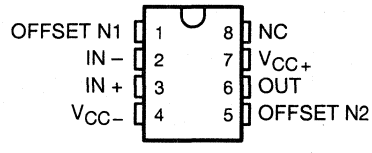
description (continued)

The design features a 30-V/μs minimum slew rate, which results in a high-power bandwidth. A low audio-band noise of 28 nV/√Hz is typical with a 55 nV/√Hz maximum at 10 Hz. Settling time to 0.1% of a 10-V step (1-kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8 MHz minimum. As such, the TLE2071 and TLE2071A offer significant speed and noise advantages at a low 1.7-mA typical supply current.

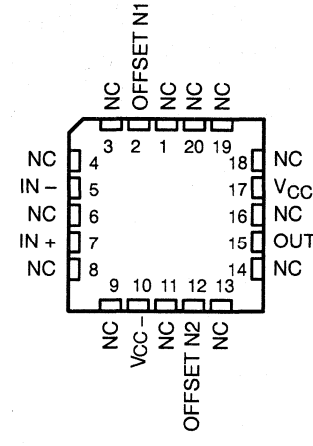
The input current characteristics traditionally associated with JFET-input amplifiers have been maintained. Input offset voltage is graded to a 4 mV and 2 mV maximum for the TLE2071 and TLE2071A, respectively. Typically, temperature coefficient of input offset voltage is 3.2 μV/°C and typical CMRR and k_{SVR} are 98 dB and 99 dB, respectively. Device performance is relatively independent of supply voltage over the wide ±2.25-V to ±19-V range. The input common-mode voltage range extends from the positive supply down to V_{CC-} + 4 V without significant degradation to dynamic performance. Maximum peak output voltage swing is from V_{CC+} – 1 V to V_{CC-} + 1 V under light loading conditions. The output is capable of sourcing and sinking currents to at least 30 mA and can sustain shorts to either supply. Care must be taken to ensure that maximum power dissipation is not exceeded.

Both the TLE2071 and TLE2071A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix devices over the –40°C to 85°C range, and the M-suffix devices over the full military temperature range of –55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

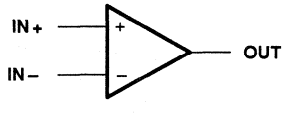


FK PACKAGE
(TOP VIEW)



NC – No internal connection

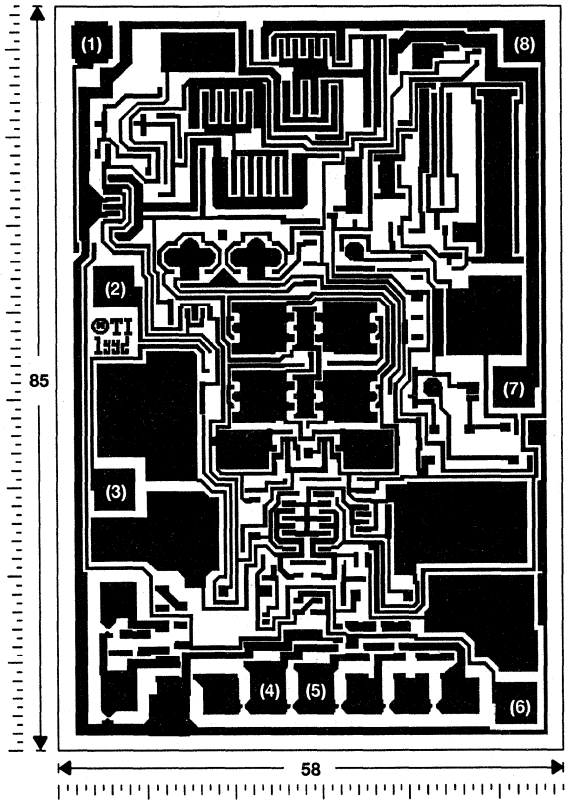
symbol

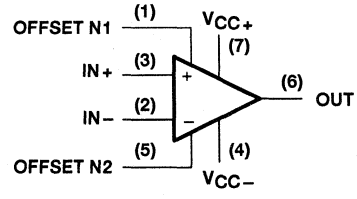


TLE2071Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2071. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

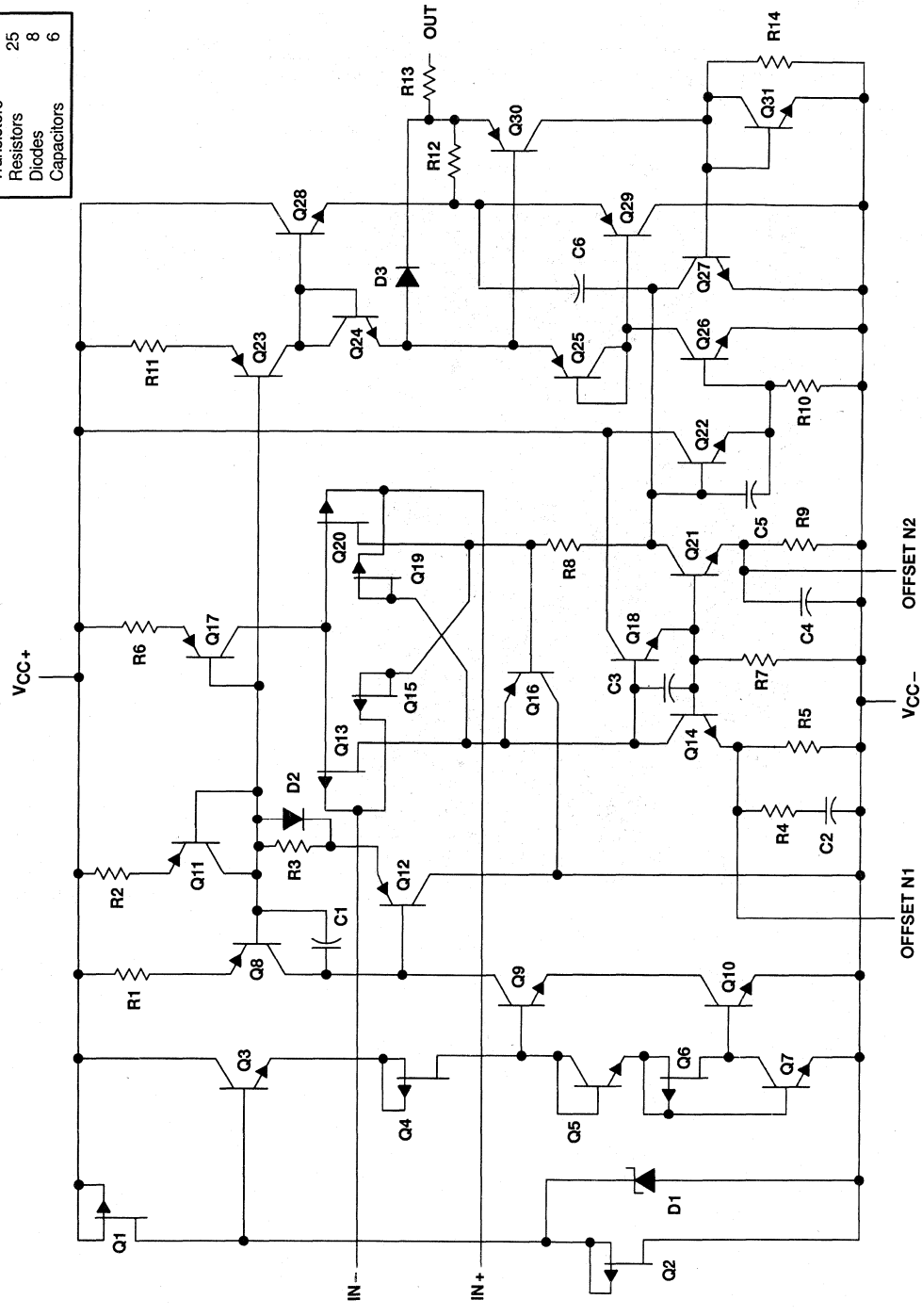
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic

ACTUAL DEVICE COMPONENT COUNT	
Transistors	33
Resistors	25
Diodes	8
Capacitors	6



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} (see Note 1) ..... −19 V
Differential input voltage range, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-}
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output can be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	344 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2.25	±19	±2.25	±19	±2.25	±19	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−0.9	5	−0.8	5	−0.8	5	V
	$V_{CC\pm} = \pm15$ V	−10.9	15	−10.8	15	−10.8	15	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071C			TLE2071AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.34	4		0.3	2	mV
				Full range			6			4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29		3.2	29	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.9			5 to −0.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−3.5	−4.2		−3.5	−4.2		V
				Full range	−3.4			−3.4			
		I_O = 2 mA		25°C	−3.7	−4.1		−3.7	−4.1		
				Full range	−3.6			−3.6			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071C			TLE2071AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0,	No load	25°C	1.35	1.6	2.2	1.35	1.6	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071C			TLE2071AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	23			23			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	23			23			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071C			TLE2071AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.49	4		0.47	2	mV
				Full range			6			4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29		3.2	29	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.9			15 to −10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.4			−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			81			

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071C			TLE2071AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0,	No load	25°C	1.35	1.7	2.2	1.35	1.7	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071C			TLE2071AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	30	40		30	40		V/μs
				Full range	27			27			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	27			27			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071I			TLE2071AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.34	4		0.3	2	mV
				Full range			7.6			5.6	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29		3.2	29	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			5			5	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			10			10	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.7			−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.4			−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071I			TLE2071AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.6	2.2	1.35	1.6	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071I			TLE2071AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		25°C		35			35		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF, R_L = 2 kΩ, See Figure 2		25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ, A_{VD} = −1, C_L = 25 pF		25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF, R_L = 2 kΩ, See Figure 2		25°C		56°			56°		

† Full range is 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071I			TLE2071AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.49	4		0.47	2	mV
				Full range			7.6			5.6	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29		3.2	29	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			5			5	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			10			10	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.4			−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071I			TLE2071AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.7	2.2	1.35	1.7	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071I			TLE2071AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±10 V, A_{VD} = −1, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		25°C	30	40		30	40		V/μs
				Full range	24			24			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	24			24			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF, R_L = 2 kΩ, See Figure 2		25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF, R_L = 2 kΩ, See Figure 2		25°C		57°			57°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071M			TLE2071AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.34	4		0.3	2	mV
				Full range			9.2			7.2	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29*		3.2	29*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.6			3.6			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.3			3.3			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.6			−3.6			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.3			−3.3			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071M			TLE2071AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.6	2.2	1.35	1.6	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071M			TLE2071AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		25°C		35			35		V/μs
				Full range	20*			20*			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	20*			20*			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55*		28	55*	nV/√Hz
			f = 10 kHz			11.6	17*		11.6	17*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071M			TLE2071AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.49	4		0.47	2	mV
				Full range			9.2			7.2	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29*		3.2	29*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.9			15 to −10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.3			13.3			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.6			−13.6			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.3			−13.3			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2071M			TLE2071AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.7	2.2	1.35	1.7	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2071M			TLE2071AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C	30	40		30	40		V/μs
				Full range	22			22		*	
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55*		28	55*	nV/√Hz
			f = 10 kHz			11.6	17*		11.6	17*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C	8*	10		8*	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C	478*	637		478*	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		57°			57°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLE2071Y MIN	TLE2071Y TYP	TLE2071Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0,	V_O = 0,	R_S = 50 Ω		0.49	4	mV
I_{IO}	Input offset current	V_{IC} = 0,	V_O = 0,	See Figure 4		6	100	pA
I_{IB}	Input bias current					20	175	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω			15 to −11	15 to 11.9		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA			13.8	14.1		V
		I_O = −2 mA			13.5	13.9		
		I_O = −20 mA			11.5	12.3		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA			−13.8	−14.2		V
		I_O = 2 mA			−13.5	−14		
		I_O = 20 mA			−11.5	−12.4		
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω		80	96		dB
			R_L = 2 kΩ		90	109		
			R_L = 10 kΩ		95	118		
r_i	Input resistance	V_{IC} = 0				10^{12}		Ω
c_i	Input capacitance	V_O = 0, See Figure 5	Common mode			7.5		pF
			Differential			2.5		
z_o	Open-loop output impedance	f = 1 MHz				80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		V_O = 0,	80	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		V_O = 0,	82	99		dB
I_{CC}	Supply current	V_O = 0,	No load		1.35	1.7	2.2	mA
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V		−30	−45		mA
			V_{ID} = −1 V		30	48		

PARAMETER MEASUREMENT INFORMATION

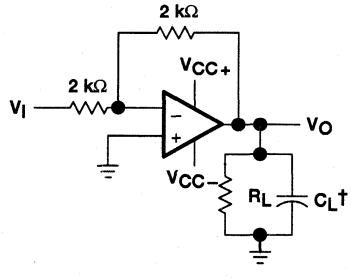


Figure 1. Slew-Rate Test Circuit

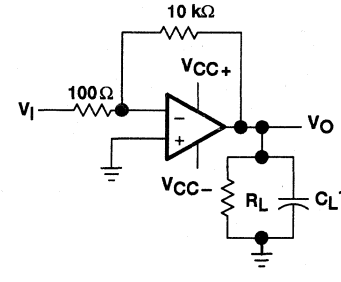


Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

† Includes fixture capacitance

PARAMETER MEASUREMENT INFORMATION

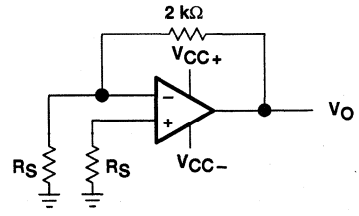


Figure 3. Noise-Voltage Test Circuit

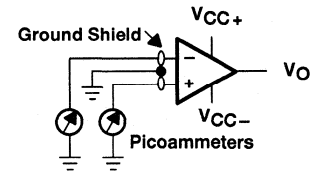


Figure 4. Input-Bias and Offset-Current Test Circuit

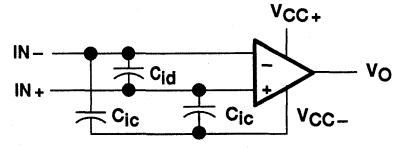


Figure 5. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2071 and TLE2071A, accurate measurement of the bias becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient	Distribution	7
I_{IO}	Input offset current	vs Free-air temperature	8, 9
I_{IB}	Input bias current	vs Free-air temperature vs Supply voltage	8, 9 10
V_{ICR}	Common-mode input voltage range	vs Free-air temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM+}	Maximum positive peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	14 16, 17 18

TYPICAL CHARACTERISTICS

Table of Graphs (Continued)

			FIGURE
V_{OM-}	Maximum negative peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	15 16, 17 18
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
V_O	Output voltage	vs Settling time	20
A_{VD}	Differential voltage amplification	vs Load resistance vs Free-air temperature vs Frequency	21 22, 23 24, 25
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	26 27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	28 29
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	30 31 32, 33
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	34 35 36
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THD + N	Total harmonic distortion plus noise	vs Frequency	45, 46
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	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	48 49
	Gain margin	vs Load capacitance	50
ϕ_m	Phase margin	vs Free-air temperature vs Supply voltage vs Load capacitance	51 52 53
	Phase shift	vs Frequency	24, 25
	Large-signal pulse response, noninverting	vs Time	54
	Small-signal pulse response	vs Time	55
z_o	Closed-loop output impedance	vs Frequency	56

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLE2071
INPUT OFFSET VOLTAGE

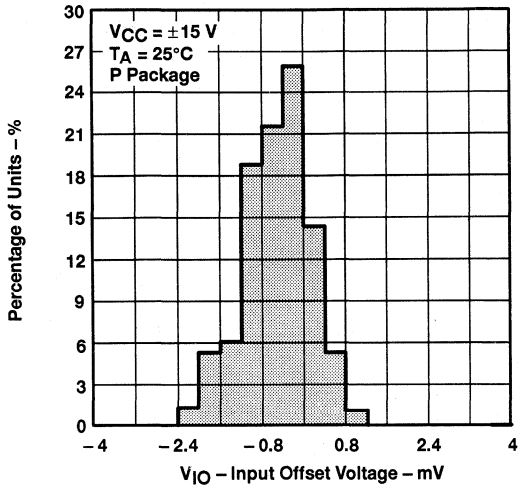


Figure 6

DISTRIBUTION OF TLE2071 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

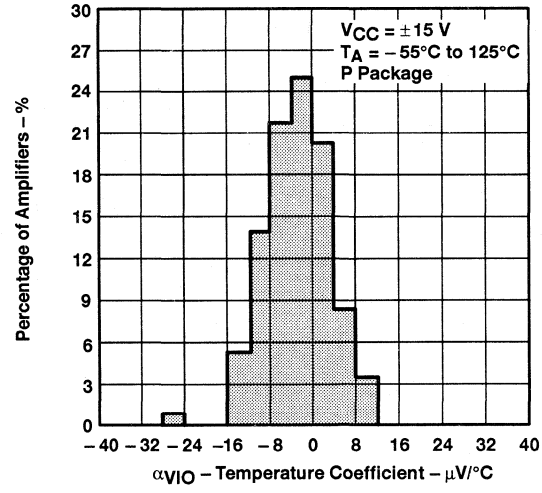


Figure 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

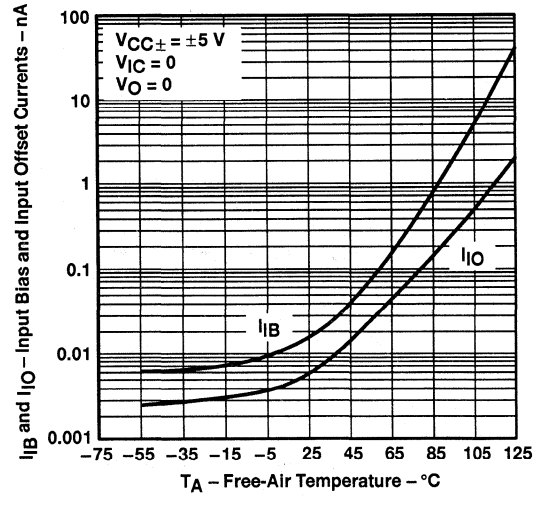


Figure 8

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

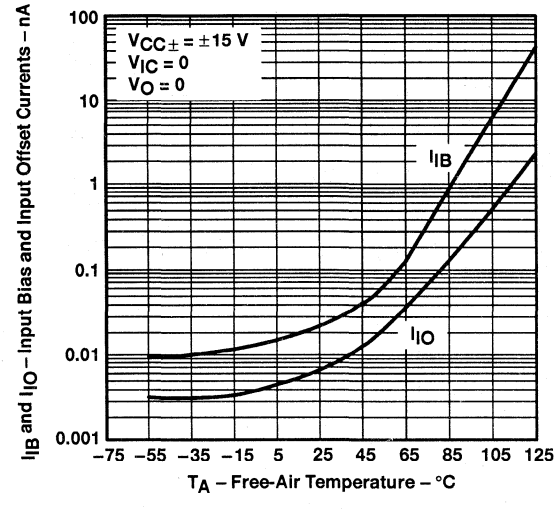


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

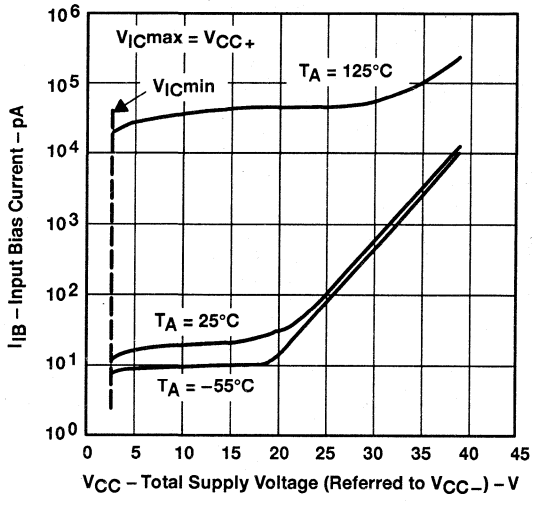


Figure 10

COMMON-MODE INPUT VOLTAGE RANGE
vs
FRRE-AIR TEMPERATURE

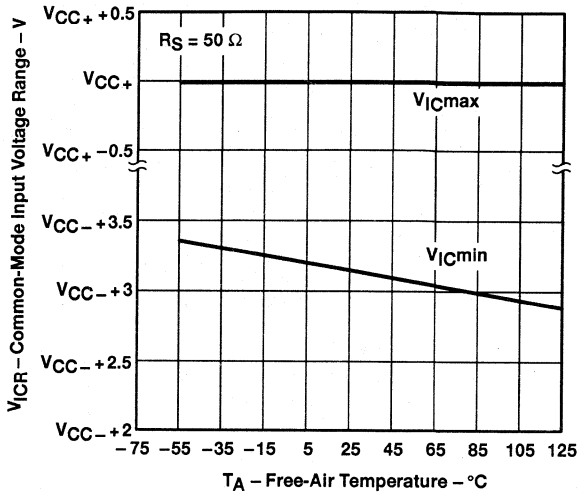


Figure 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

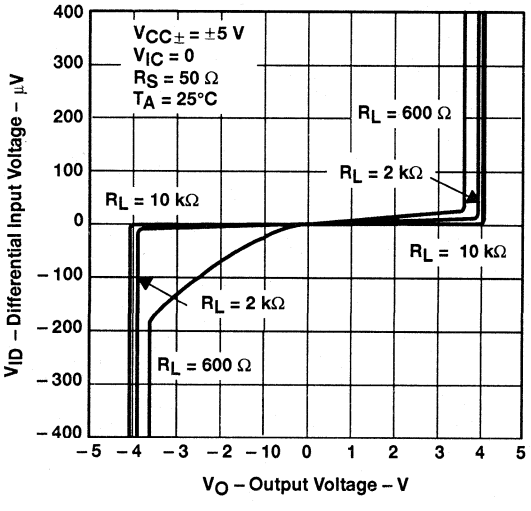


Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

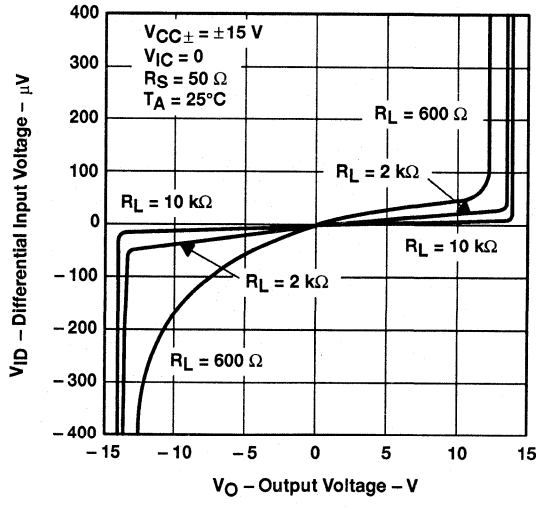


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

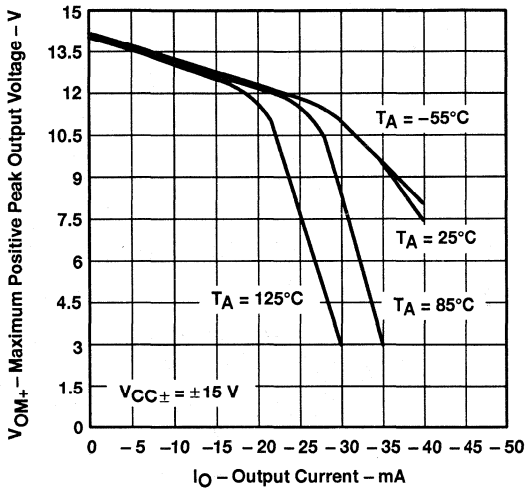


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

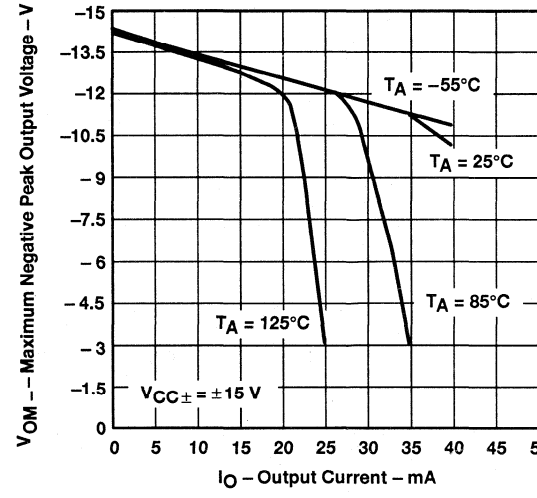


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

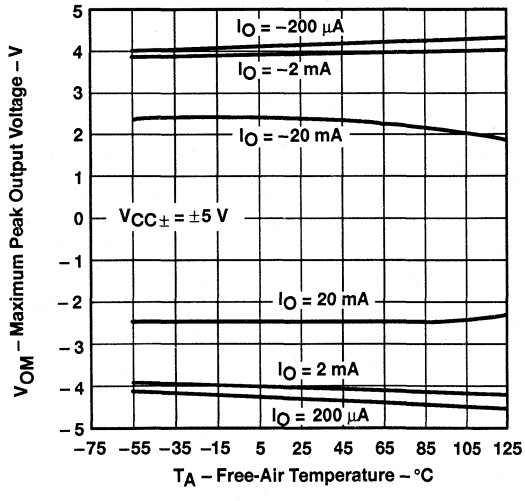


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

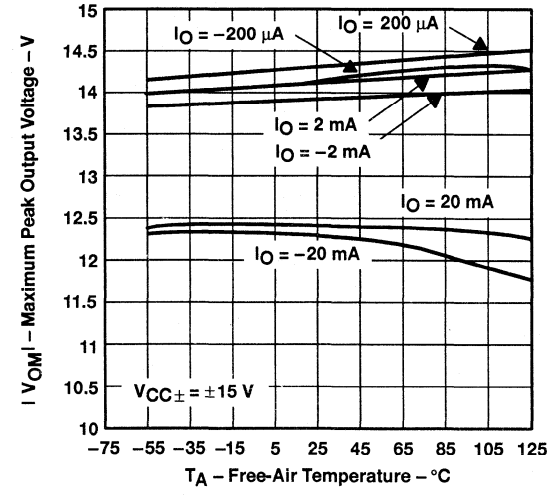


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

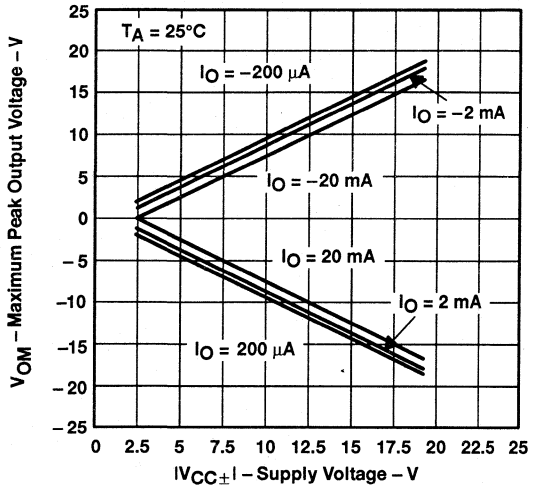


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

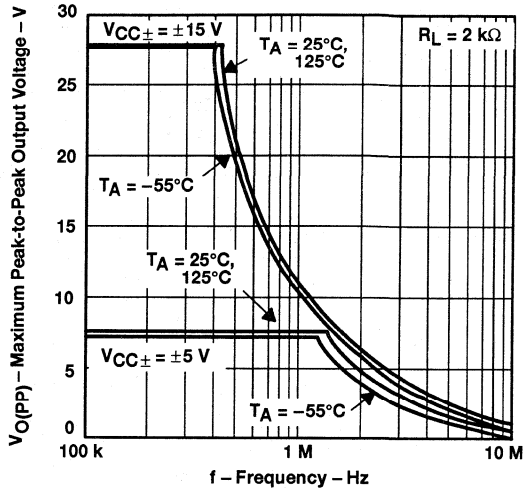


Figure 19

OUTPUT VOLTAGE
vs
SETTLING TIME

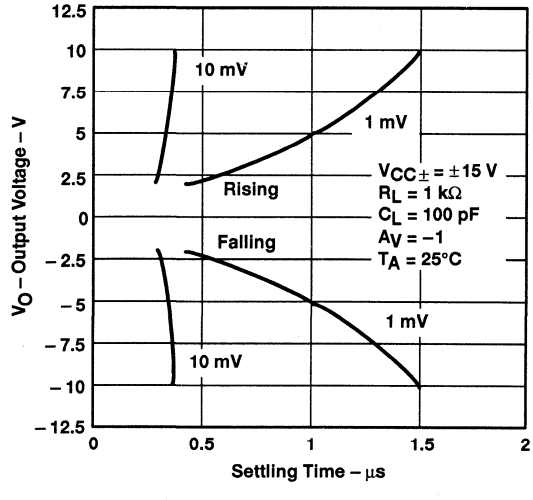


Figure 20

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

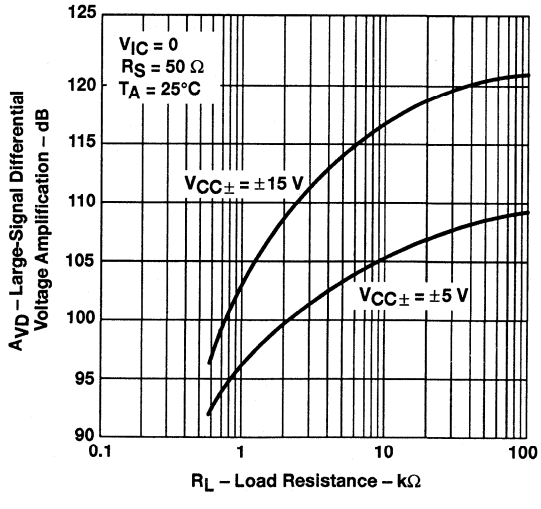


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

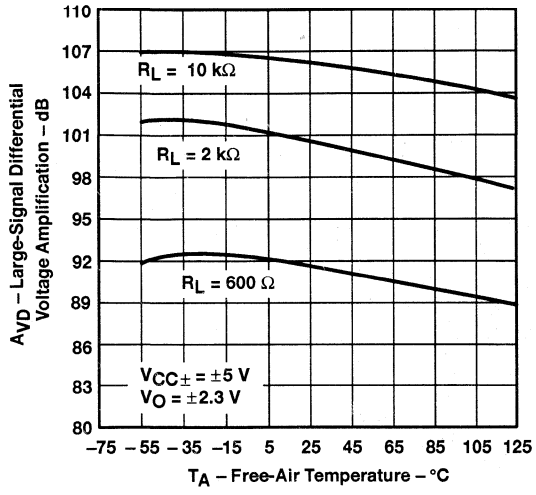


Figure 22

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

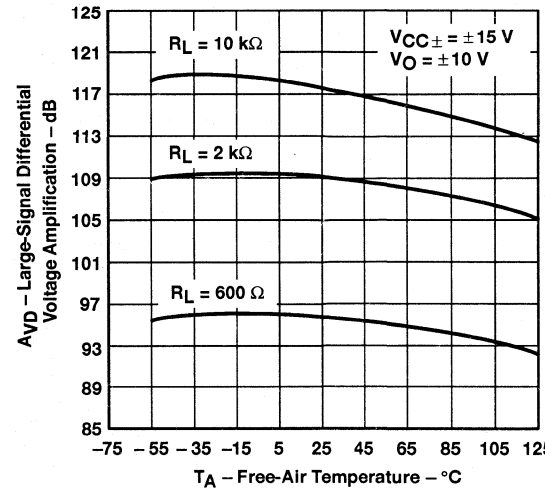


Figure 23

SMALL-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

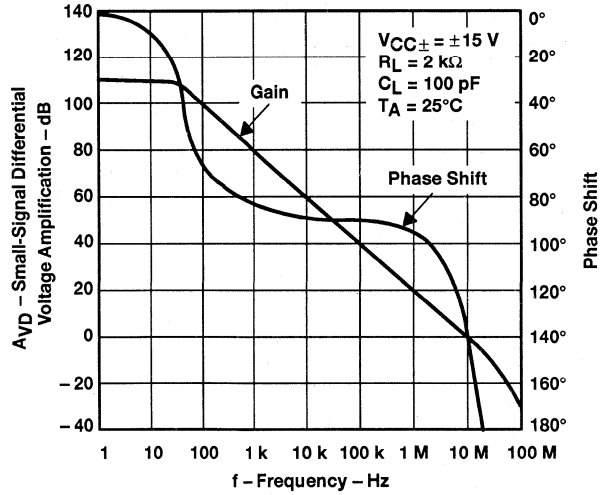


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

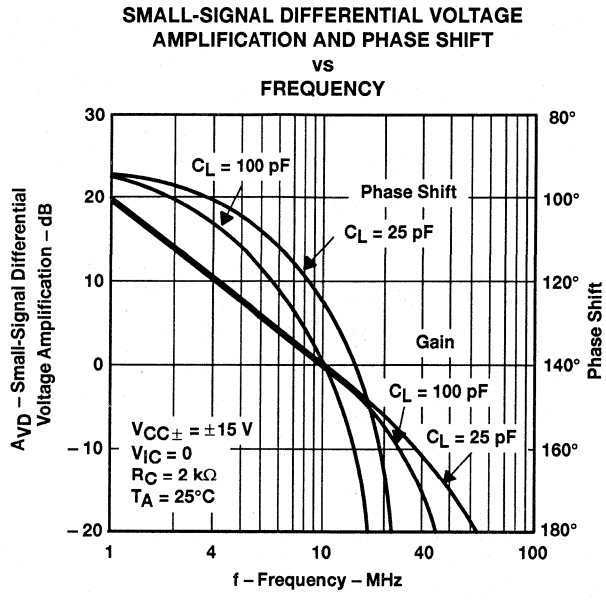


Figure 25

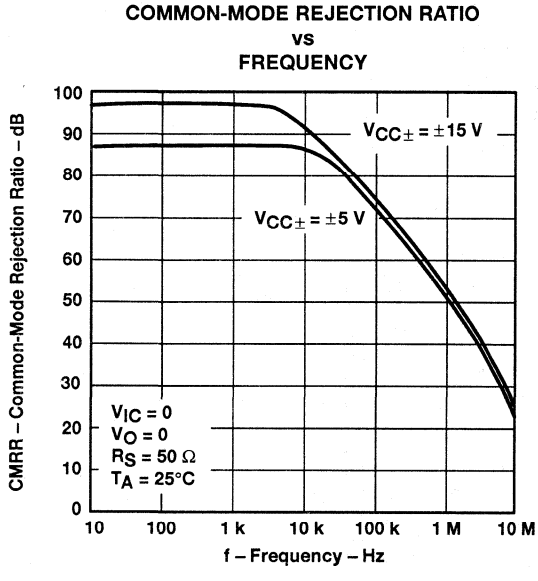


Figure 26

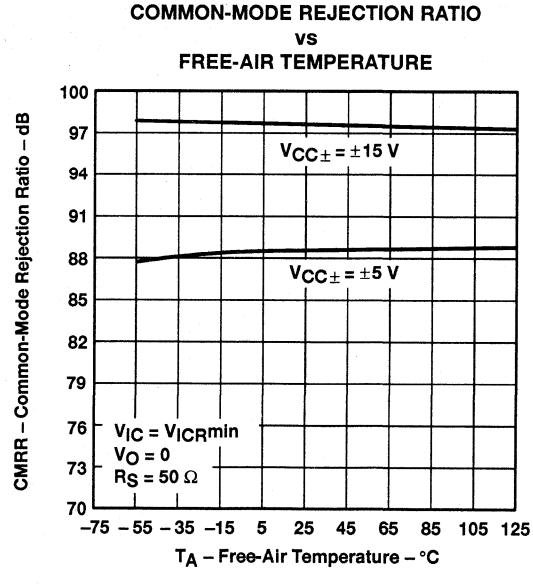


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

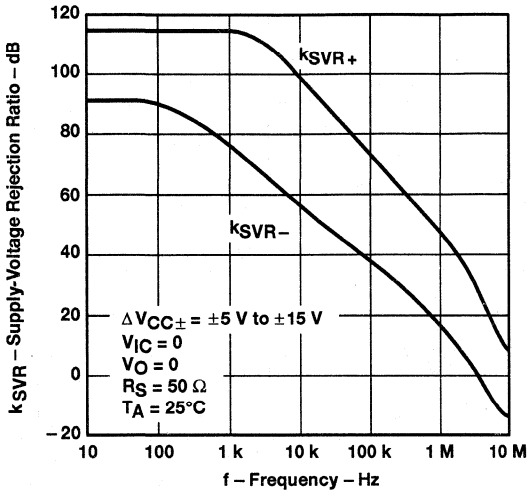


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

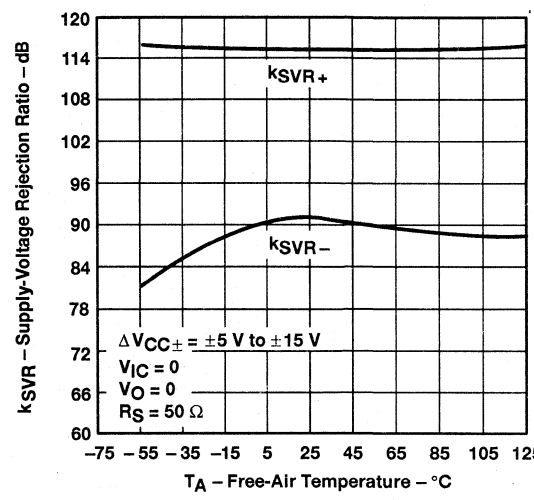


Figure 29

SUPPLY CURRENT vs SUPPLY VOLTAGE

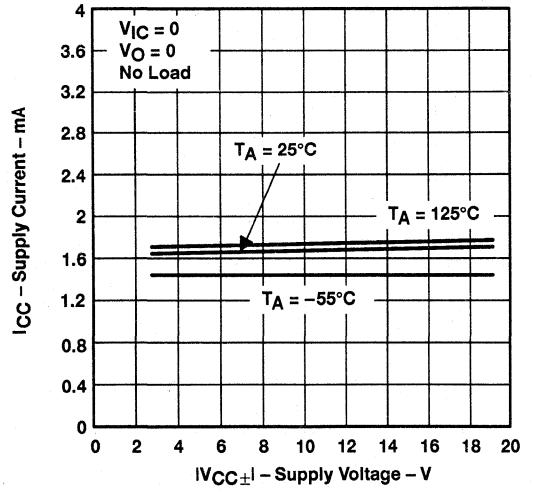


Figure 30

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

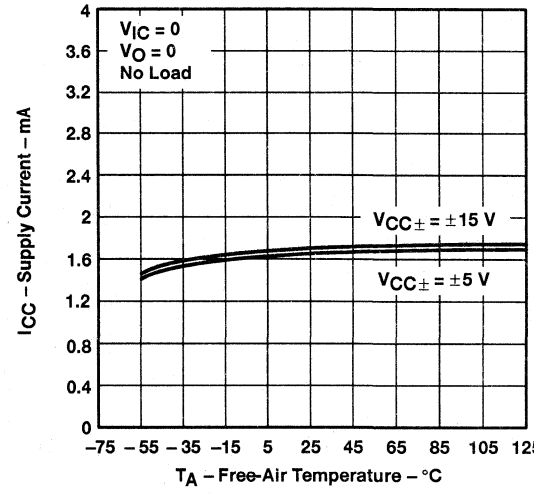


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

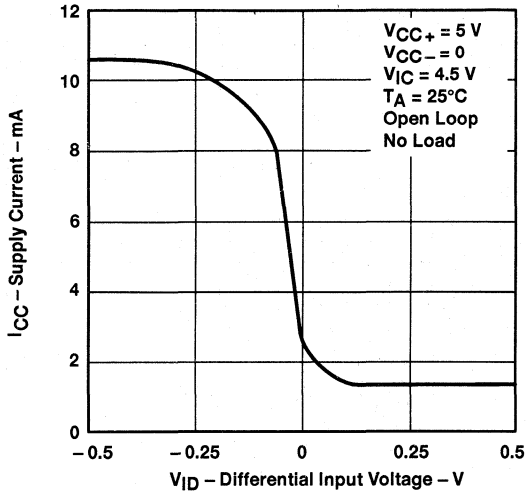


Figure 32

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

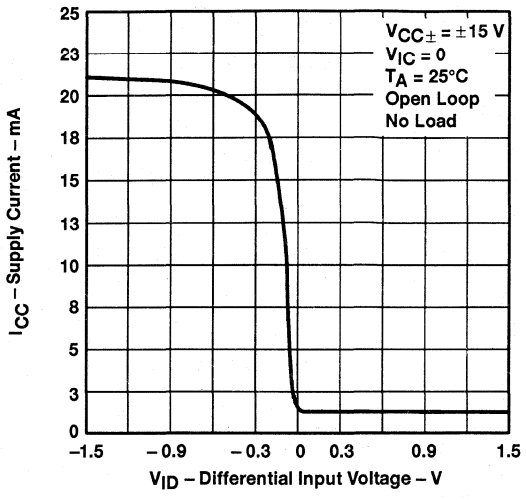


Figure 33

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

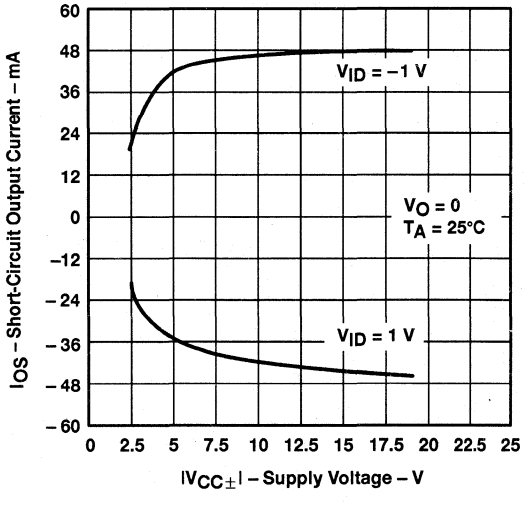


Figure 34

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

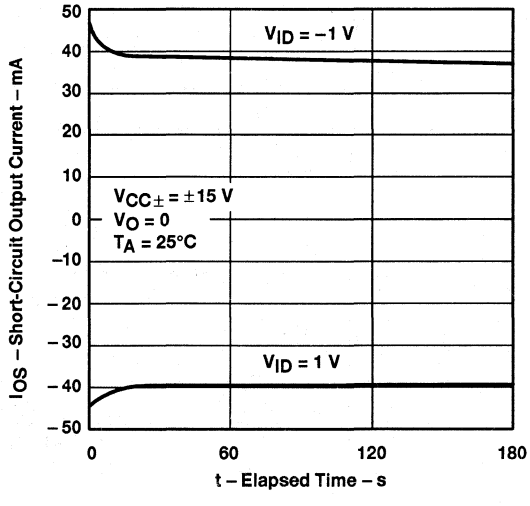


Figure 35

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

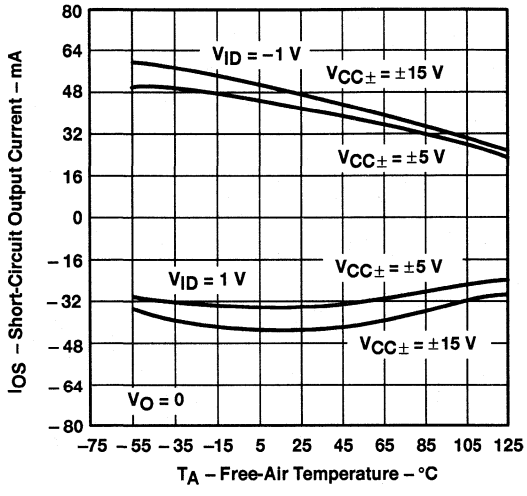


Figure 36

SLEW RATE vs FREE-AIR TEMPERATURE

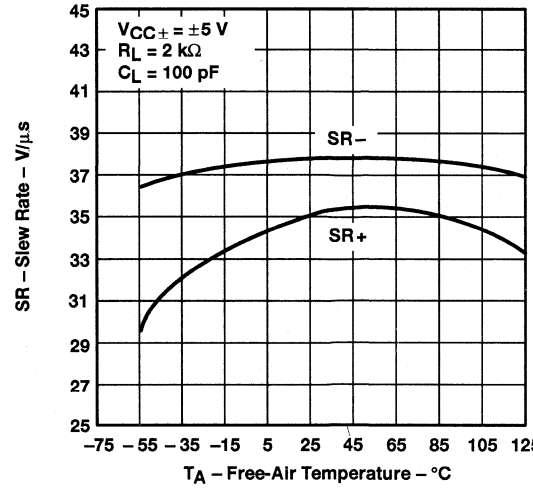


Figure 37

SLEW RATE vs FREE-AIR TEMPERATURE

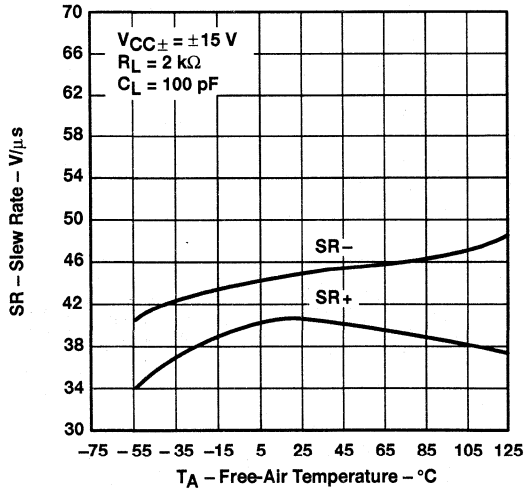


Figure 38

SLEW RATE vs LOAD RESISTANCE

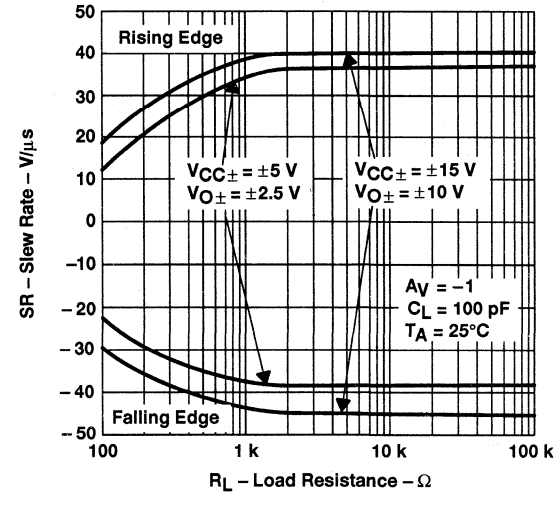


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SLEW RATE
vs
DIFFERENTIAL INPUT VOLTAGE

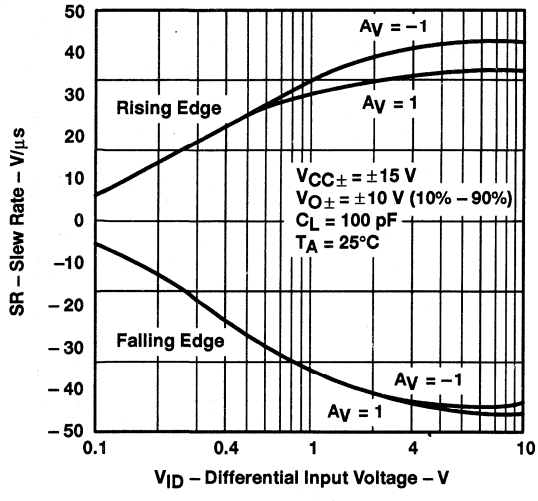


Figure 40

INPUT-REFERRED NOISE VOLTAGE
SPECTRAL DENSITY
vs
FREQUENCY

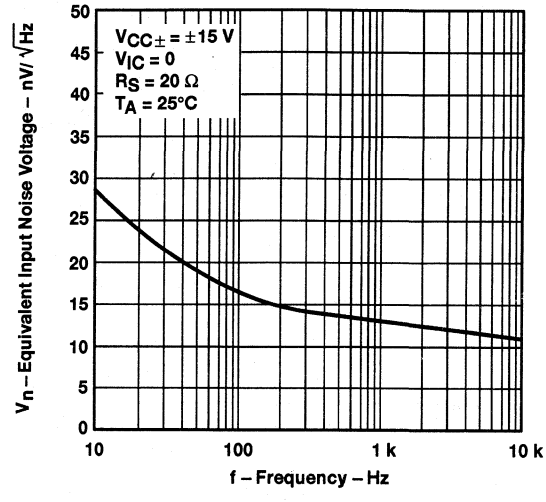


Figure 41

INPUT-REFERRED NOISE VOLTAGE
vs
NOISE BANDWIDTH

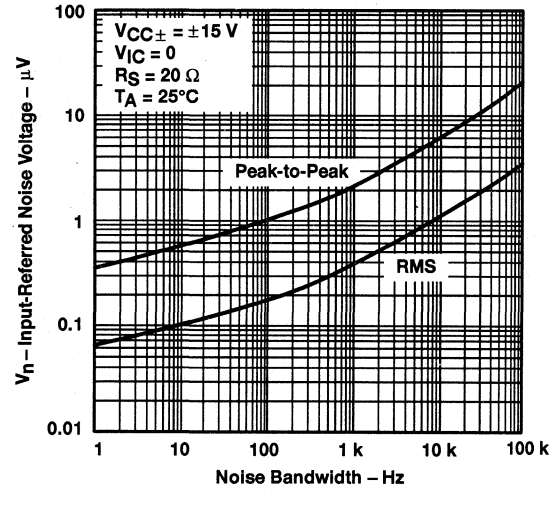


Figure 42

INPUT-REFERRED NOISE VOLTAGE
OVER A 10-SECOND TIME INTERVAL

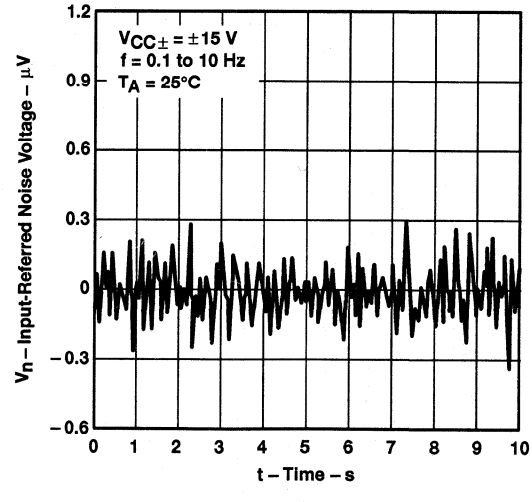


Figure 43

TYPICAL CHARACTERISTICS

THIRD-OCTAVE SPECTRAL NOISE DENSITY
vs
FREQUENCY BANDS

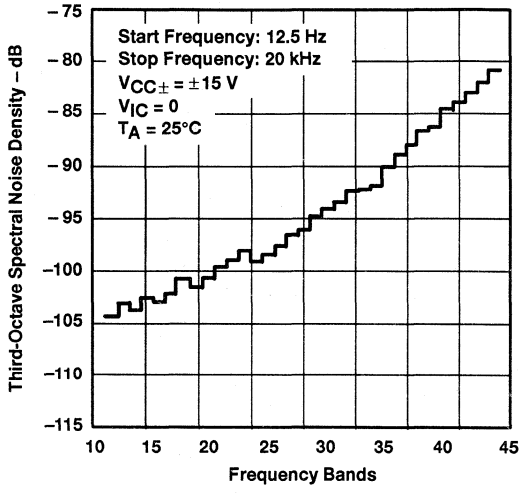


Figure 44

TOTAL HARMONIC DISTORTION PLUS
NOISE
vs
FREQUENCY

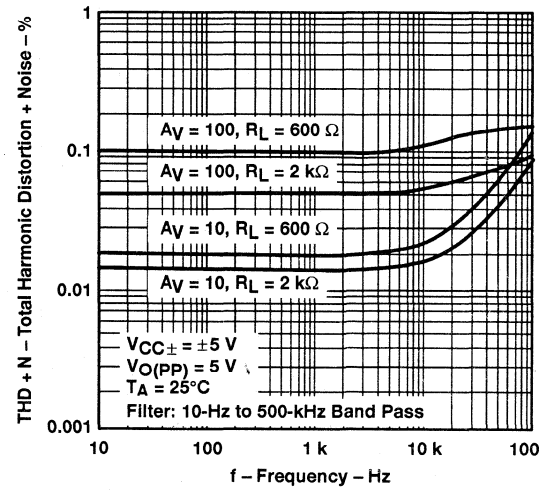


Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

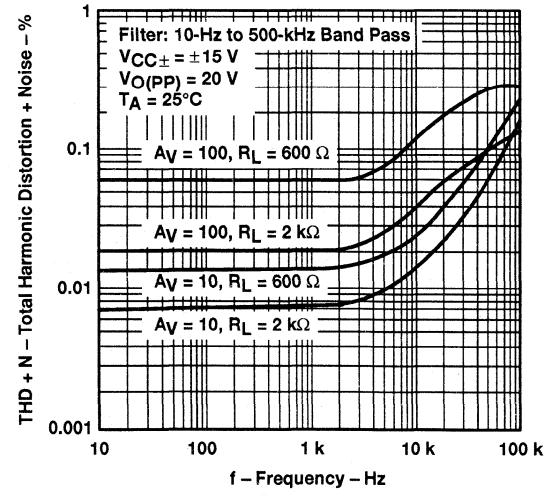


Figure 46

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

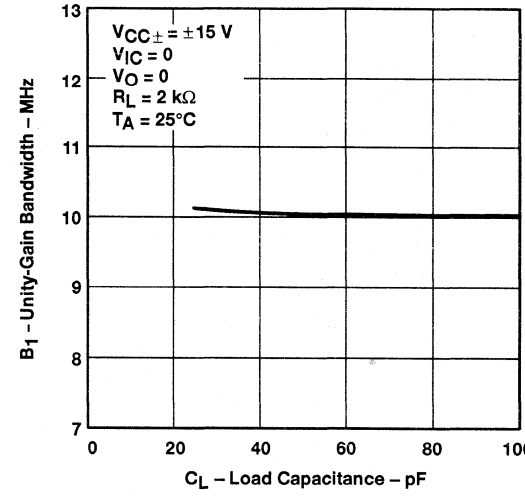


Figure 47

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

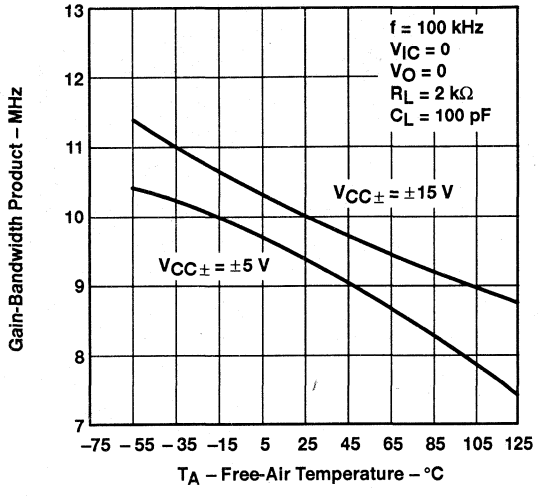


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

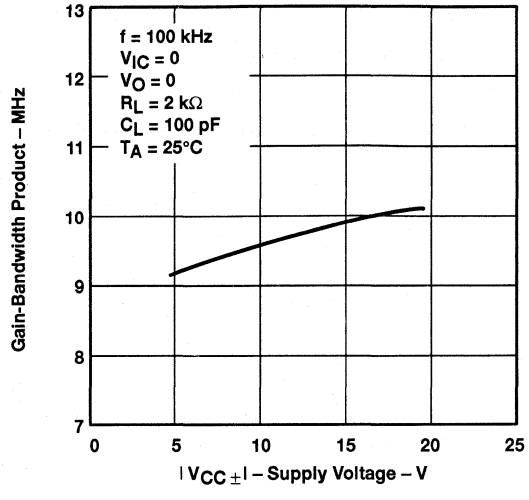


Figure 49

GAIN MARGIN
vs
LOAD CAPACITANCE

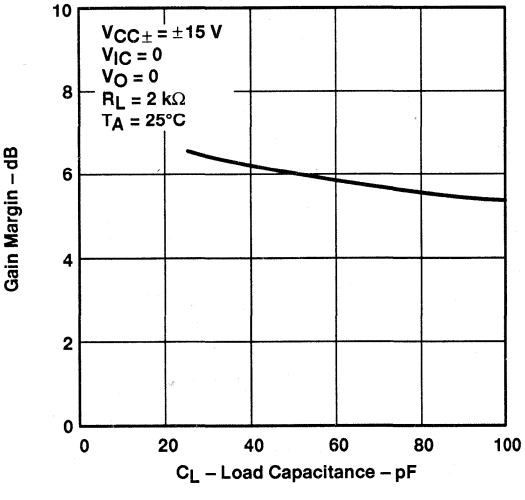


Figure 50

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

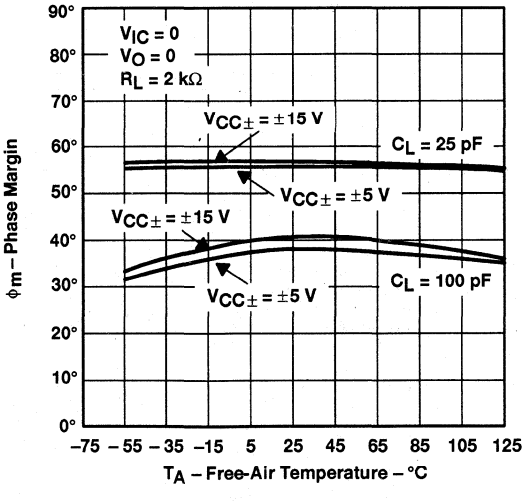


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

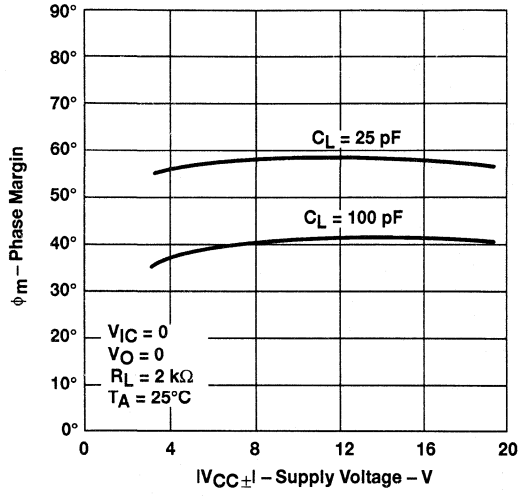


Figure 52

PHASE MARGIN
vs
LOAD CAPACITANCE

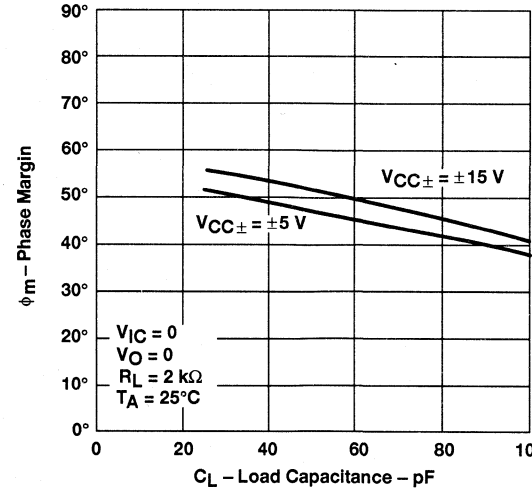


Figure 53

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

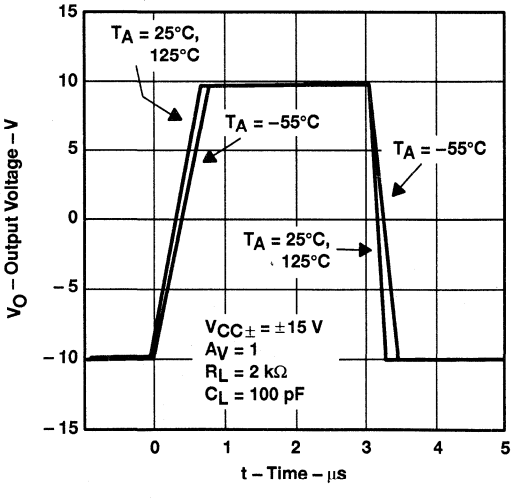


Figure 54

SMALL-SIGNAL PULSE RESPONSE

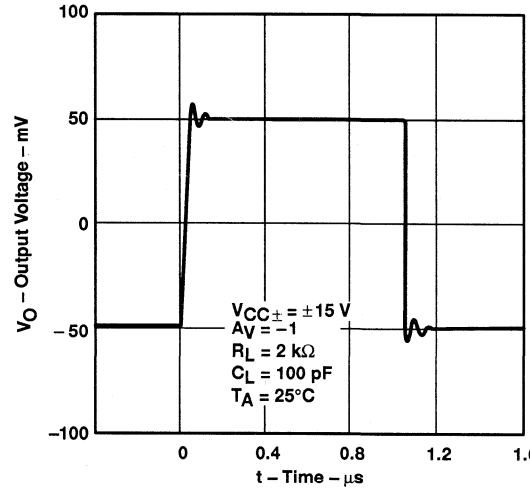


Figure 55

TYPICAL CHARACTERISTICS

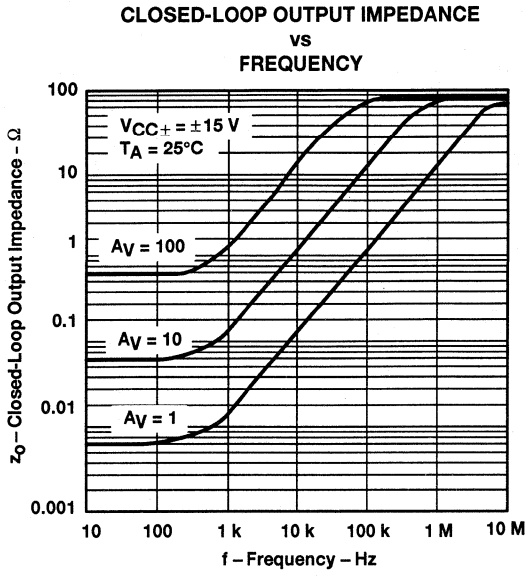


Figure 56

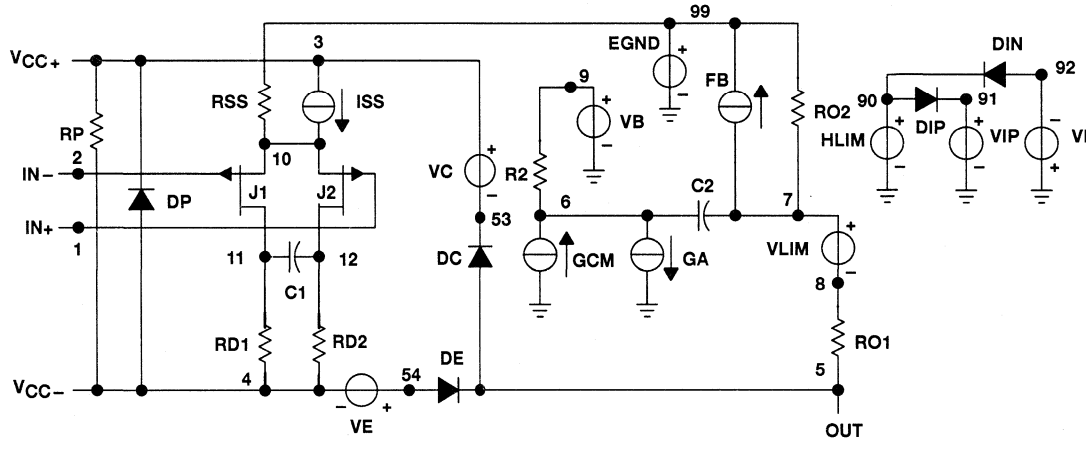
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 4) and subcircuit in Figure 57 were generated using the TLE2071 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G.R. Boyle, B.M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



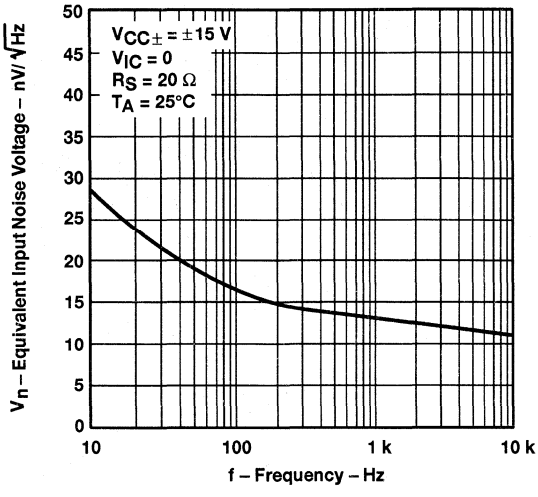

```
.SUBCKT TLE2071 1 2 3 4 5
  C1   11   12     2.2E-12
  C2    6    7     10.00E-12
  DC    5   53     DX
  DE   54    5     DX
  DLP  90   91     DX
  DLN  92   90     DX
  DP    4    3     DX
  EGND 99    0     POLY (2) (3,0) (4,0) 0 .5 .5
  FB    7   99     POLY (5) VB VC VE VLP VLN 0
+ 5.607E6 -6E6 6E6 6E6 -6E6
  GA    6    0     11 12 333.0E-6
  GCM   0    6     10 99 7.43E-9
  ISS   3   10     DC 400.0E-6
  HLIM 90    0     VLIM 1K
  J1   11    2     10 JX
  J2   12    1     10 JX
  R2    6    9     100.0E3
  RD1   4   11     3.003E3
  RD2   4   12     3.003E3
  RO1   8    5     80
  RO2   7   99     80
  RP    3    4     27.30E3
  RSS  10   99     500.0E3
  VB    9    0     DC 0
  VC    3   53     DC 2.20
  VE   54    4     DC 2.20
  VLIM  7    8     DC 0
  VLP  91    0     DC 45
  VLN   0   92     DC 45
.MODEL DX D (IS=800.0E-18)
.MODEL JX PJF (IS=15.00E-12 BETA=554.5E-6
+ VTO=-.6)
.ENDS
```

Figure 57. Boyle Macromodel and Subcircuit

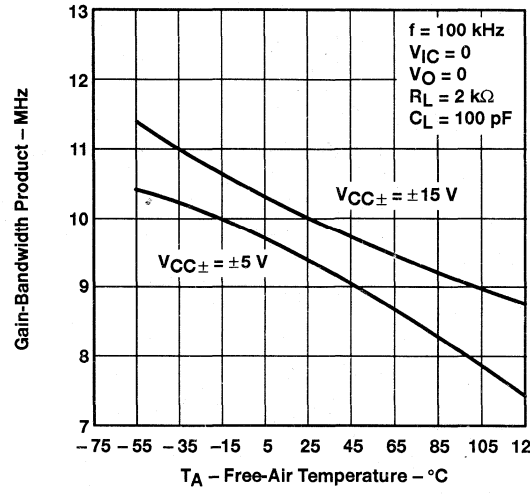
PSpice and *Parts* are registered trademarks of MicroSim Corporation.

- 40-V/μs Slew Rate Typ
- Low Noise
  17 nV/√Hz Max at f = 10 kHz
  11.6 nV/√Hz Typ at f = 10 kHz
- High Gain-Bandwidth Product . . . 10 MHz
- ±30-mA Minimum Short-Circuit Output Current
- Wide Supply Range . . . ±2.25 V to ±19 V
- Input Range Includes the Positive Supply
- Macromodel Included
- Fast Settling Time Using 10-V Step
  400 ns to 10 mV Typ
  1.5 μs to 1 mV Typ

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE



description

The TLE2072 and TLE2072A are low-noise, high-performance, internally compensated JFET-input dual operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. These devices combine low noise with outstanding output drive capability, high slew rate, and wide bandwidth.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	3.5 mV 6 mV	TLE2072ACD TLE2072CD	—	—	TLE2072ACP TLE2072CP	— TLE2072Y
–40°C to 85°C	3.5 mV 6 mV	TLE2072AID TLE2072ID	—	—	TLE2072AIP TLE2072IP	—
–55°C to 125°C	3.5 mV 6 mV	—	TLE2072AMFK TLE2072MFK	TLE2072AMJG TLE2072MJG	—	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2072ACDR). Chip-form versions are tested at T_A = 25°C. For chip-form orders, contact your local TI sales office.

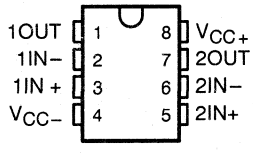
description (continued)

The design features a 28-V/μs minimum slew rate, which results in a high-power bandwidth. A low audio-band noise of 28 nV/√Hz is typical with a 55 nV/√Hz maximum at 10 Hz. Settling time to 0.1% of a 10-V step (1-kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8 MHz minimum. As such, the TLE2072 and TLE2072A offer significant speed and noise advantages at a low 1.5-mA typical supply current per channel.

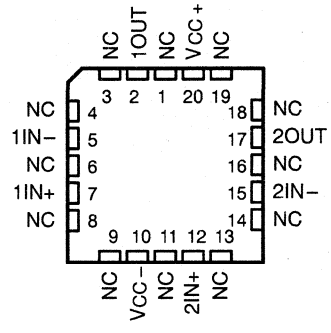
The input current characteristics traditionally associated with JFET-input amplifiers have been maintained. Input offset voltage is graded to a 6 mV and 3.5 mV maximum for the TLE2072 and TLE2072A, respectively. Typically, temperature coefficient of input offset voltage is 2.4 μV/°C and typical CMRR and k_{SVR} are 98 dB and 99 dB, respectively. Device performance is relatively independent of supply voltage over the wide ±2.25-V to ±19-V range. The input common-mode voltage range extends from the positive supply down to V_{CC-} + 4 V without significant degradation to dynamic performance. Maximum peak output voltage swing is from V_{CC+} – 1 V to V_{CC-} + 1 V under light current loading conditions. The output is capable of sourcing and sinking currents to at least 30 mA and can sustain shorts to either supply. Care must be taken to ensure that maximum power dissipation is not exceeded.

Both the TLE2072 and TLE2072A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix devices over the –40°C to 85°C range, and the M-suffix devices over the full military temperature range of –55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

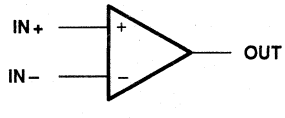


FK PACKAGE
(TOP VIEW)



NC – No internal connection

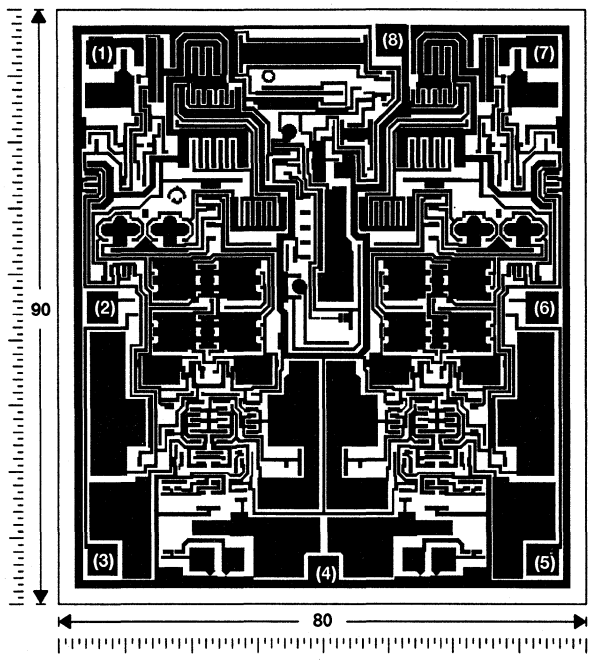
symbol

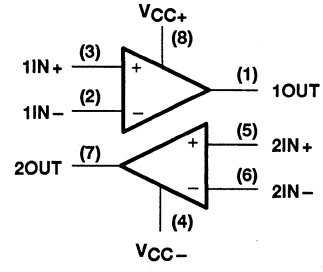


TLE2072Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2072. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

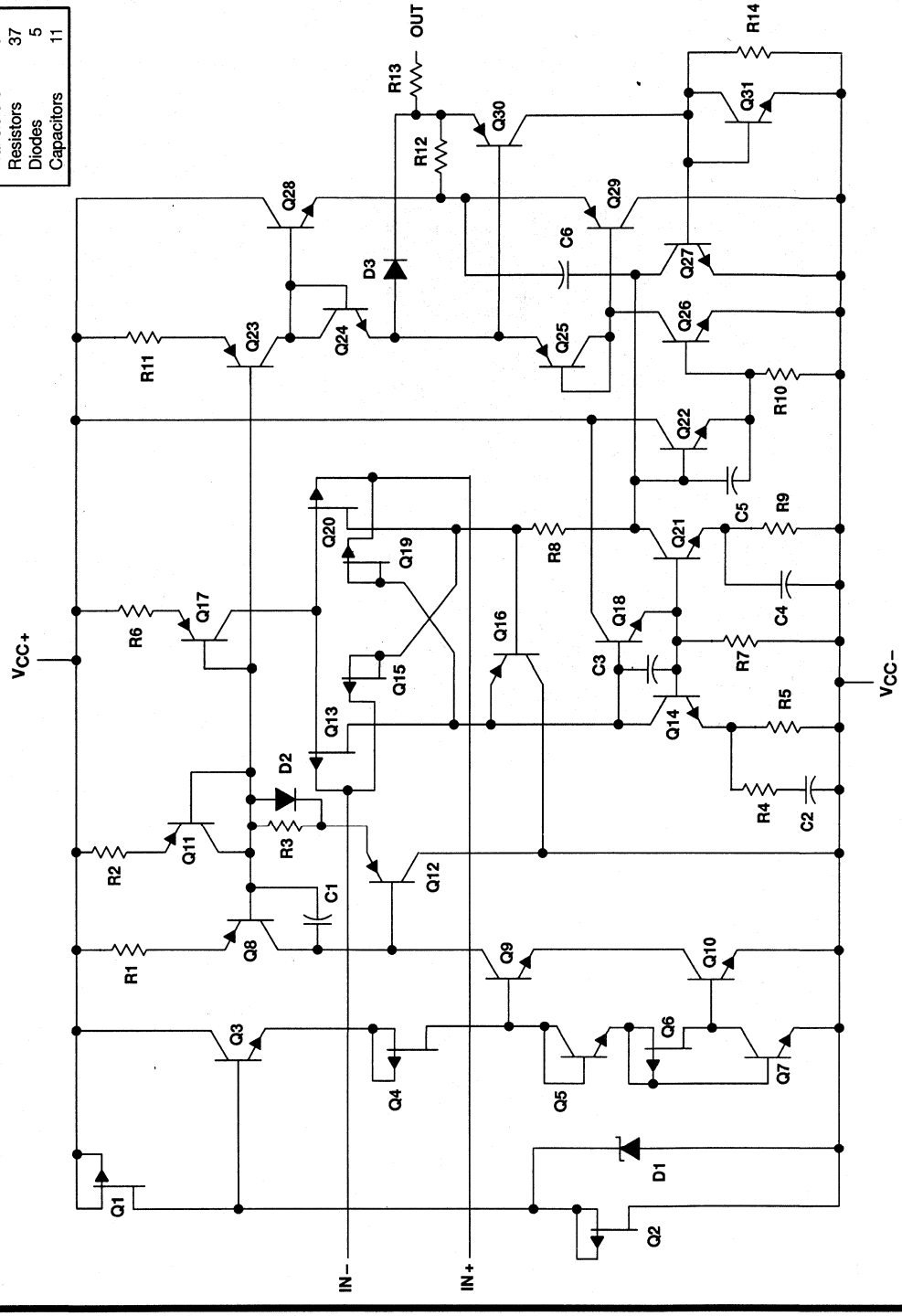
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

ACTUAL DEVICE COMPONENT COUNT	
Transistors	57
Resistors	37
Diodes	5
Capacitors	11

equivalent schematic (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} (see Note 1) ..... −19 V
Differential input voltage range, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-}
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output can be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	344 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2.25	±19	±2.25	±19	±2.25	±19	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−0.9	5	−0.8	5	−0.8	5	V
	$V_{CC\pm} = \pm15$ V	−10.9	15	−10.8	15	−10.8	15	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072C			TLE2072AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.9	6		0.65	3.5	mV
				Full range			7.8			5.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.3	25		2.3	25	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.9			5 to −0.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.7			−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.4			−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	2.9	3.6	2.7	2.9	3.6	mA
				Full range			3.6			3.6	

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072C			TLE2072AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
a_X	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072C			TLE2072AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072C			TLE2072AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	6		0.7	3.5	mV
				Full range			7.8			5.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25		2.4	25	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.9			15 to −10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.4			−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	81			81			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	3.1	3.6	2.7	3.1	3.6	mA
				Full range			3.6			3.6	

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072C			TLE2072AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
a_x	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072C			TLE2072AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C	28	40		28	40		V/μs
				Full range	25			25			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	25			25			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072I			TLE2072AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.9	6		0.65	3.5	mV
				Full range			9.1			6.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25		2.4	25	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			5			5	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			10			10	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.7			−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.4			−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	2.9	3.6	2.7	2.9	3.6	mA
				Full range			3.6			3.6	

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072I			TLE2072AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
a_X	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072I			TLE2072AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	20			20			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072I			TLE2072AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		1.1	6		0.7	3.5	mV
				Full range			9.1			6.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25		2.4	25	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			5			5	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			10			10	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.4			−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	3.1	3.6	2.7	3.1	3.6	mA
				Full range			3.6			3.6	

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072I			TLE2072AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
a_x	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072I			TLE2072AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±10 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C	28	40		28	40		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 0 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072M			TLE2072AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,		25°C		0.9	6		0.65	3.5	mV
				Full range			10.5			8	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.3	25*		2.3	25*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.6			3.6			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.3			3.3			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.6			−3.6			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.3			−3.3			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072M			TLE2072AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0,	R_S = 50 Ω	Full range	80			80			dB
I_{CC}	Supply current (both channels)	V_O = 0,	No load	25°C	2.7	2.9	3.6	2.7	2.9	3.6	mA
				Full range			3.6			3.6	
a_x	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072M			TLE2072AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	18*			18*			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	18*			18*			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55*		28	55*	nV/√Hz
			f = 10 kHz			11.6	17*		11.6	17*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072M			TLE2072AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	6		0.7	3.5	mV
				Full range			10.5			8	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25*		2.4	25*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.3			13.3			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.6			−13.6			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.3			−13.3			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2072M			TLE2072AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (both channels)	V_O = 0,	No load	25°C	2.7	3.1	3.6	2.7	3.1	3.6	mA
				Full range			3.6			3.6	
a_x	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2072M			TLE2072AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	28	40		28	40		V/μs
				Full range	20			20			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55*		28	55*	nV/√Hz
			f = 10 kHz			11.6	17*		11.6	17*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8*	10		8*	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478*	637		478*	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2072Y MIN	TLE2072Y TYP	TLE2072Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω			1.1	6	mV
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4			6	100	pA
I_{IB}	Input bias current				20	175	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		15 to −11	15 to 11.9		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		13.8	14.1		V
		I_O = −2 mA		13.5	13.9		
		I_O = −20 mA		11.5	12.3		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		−13.8	−14.2		V
		I_O = 2 mA		−13.5	−14		
		I_O = 20 mA		−11.5	−12.4		
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	80	96		dB
			R_L = 2 kΩ	90	109		
			R_L = 10 kΩ	95	118		
r_i	Input resistance	V_{IC} = 0			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode		7.5		pF
			Differential		2.5		
z_o	Open-loop output impedance	f = 1 MHz			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		80	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	V_O = 0,	82	99		dB
I_{CC}	Supply current (both channels)	V_O = 0,	No load		2.7	3.1	3.6 mA
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−30	−45		mA
			V_{ID} = −1 V	30	48		

PARAMETER MEASUREMENT INFORMATION

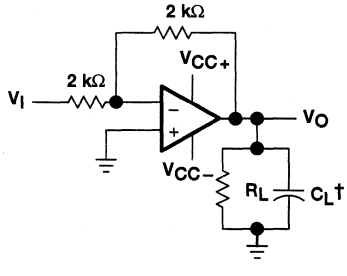


Figure 1. Slew-Rate Test Circuit

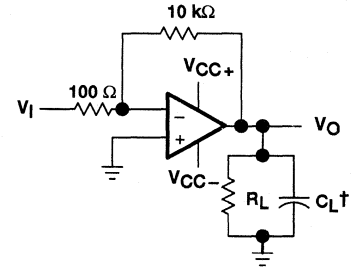


Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

† Includes fixture capacitance

PARAMETER MEASUREMENT INFORMATION

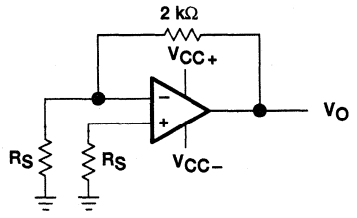


Figure 3. Noise-Voltage Test Circuit

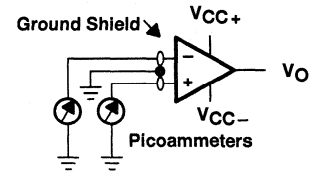


Figure 4. Input-Bias and Offset-Current Test Circuit

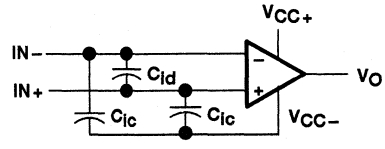


Figure 5. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2072 and TLE2072A, accurate measurement of the bias becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient	Distribution	7
I_{IO}	Input offset current	vs Free-air temperature	8, 9
I_{IB}	Input bias current	vs Free-air temperature vs Supply voltage	8, 9 10
V_{ICR}	Common-mode input voltage range	vs Free-air temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13

TYPICAL CHARACTERISTICS

Table of Graphs (Continued)

			FIGURE
V_{OM+}	Maximum positive peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	14 16, 17 18
V_{OM-}	Maximum negative peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	15 16, 17 18
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
V_O	Output voltage	vs Settling time	20
A_{VD}	Differential voltage amplification	vs Load resistance vs Free-air temperature vs Frequency	21 22, 23 24, 25
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	26 27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	28 29
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	30 31 32, 33
I_{OS}	Short-circuit output current	vs Supply voltage vs Elapsed time vs Free-air temperature	34 35 36
SR	Slew rate	vs Free-air temperature vs Load resistance vs Differential input voltage	37, 38 39 40
V_n	Equivalent input noise voltage	vs Frequency	41
V_n	Input-referred noise voltage	vs Noise bandwidth Over a 10-second time interval	42 43
	Third-octave spectral noise density	vs Frequency bands	44
THD + N	Total harmonic distortion plus noise	vs Frequency	45, 46
B_1	Unity-gain bandwidth	vs Load capacitance	47
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	48 49
	Gain margin	vs Load capacitance	50
ϕ_m	Phase margin	vs Free-air temperature vs Supply voltage vs Load capacitance	51 52 53
	Phase shift	vs Frequency	24, 25
	Large-signal pulse response, noninverting	vs Time	54
	Small-signal pulse response	vs Time	55
z_o	Closed-loop output impedance	vs Frequency	56
a_x	Crosstalk attenuation	vs Frequency	57

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLE2072
INPUT OFFSET VOLTAGE

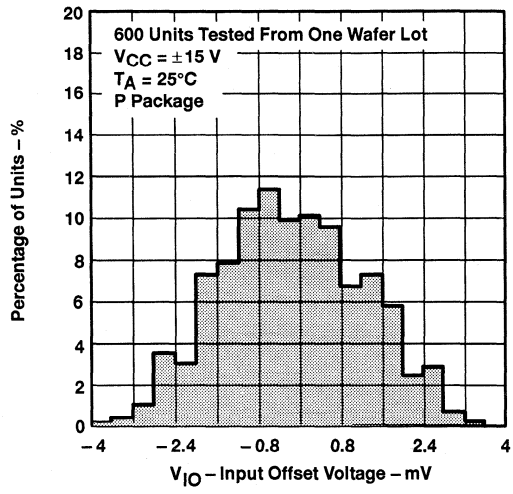


Figure 6

DISTRIBUTION OF TLE2072 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

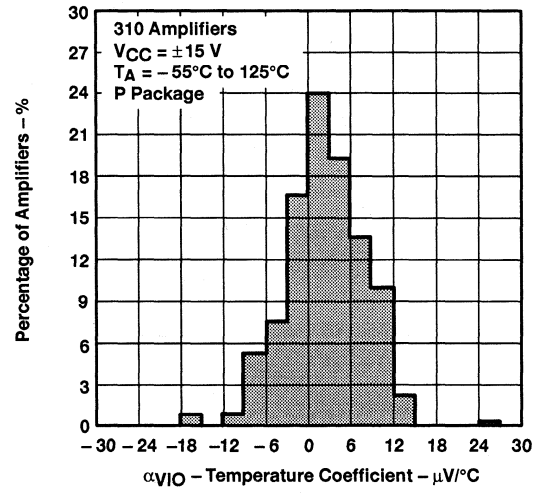


Figure 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

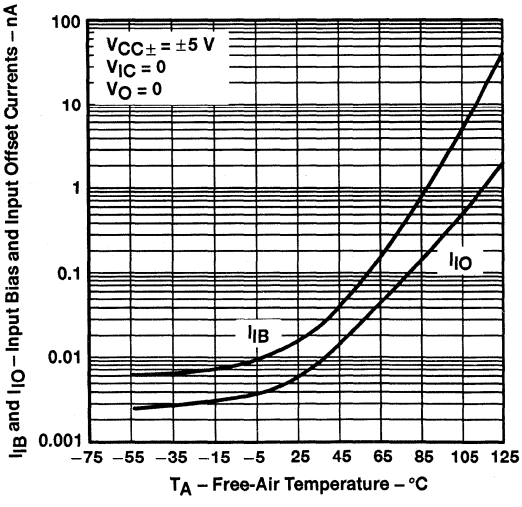


Figure 8

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

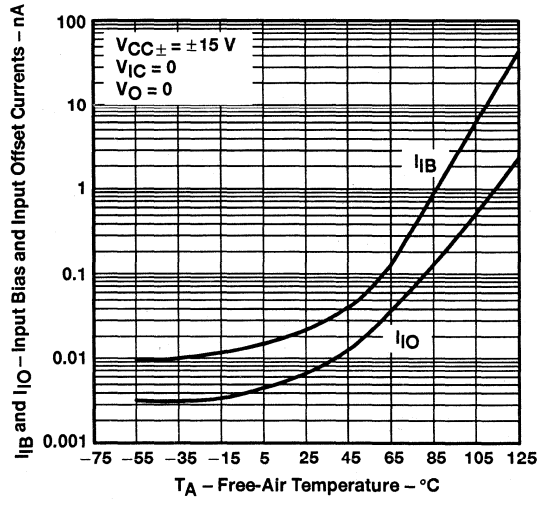


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

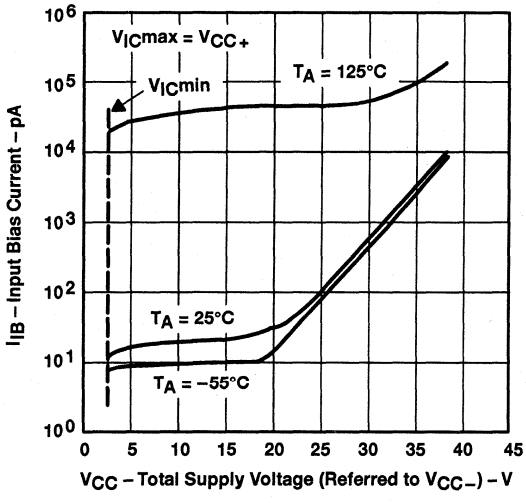


Figure 10

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

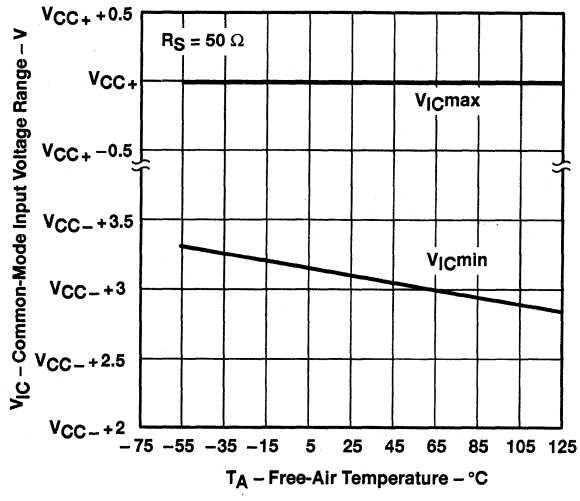


Figure 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

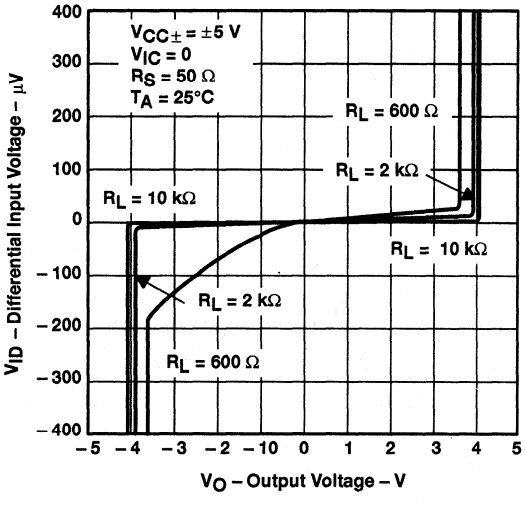


Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

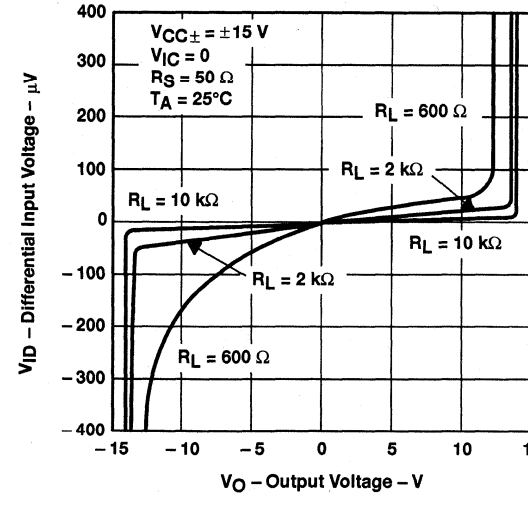


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

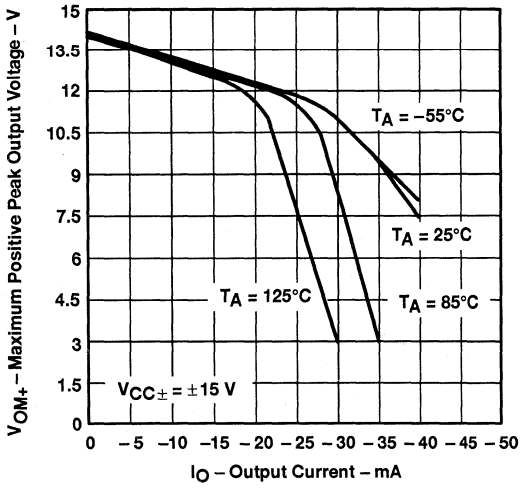


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

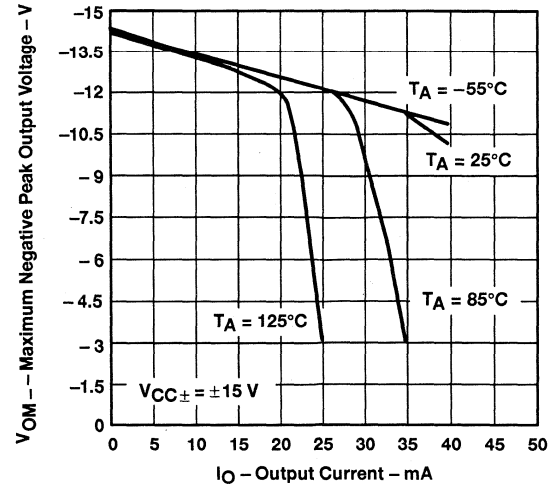


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

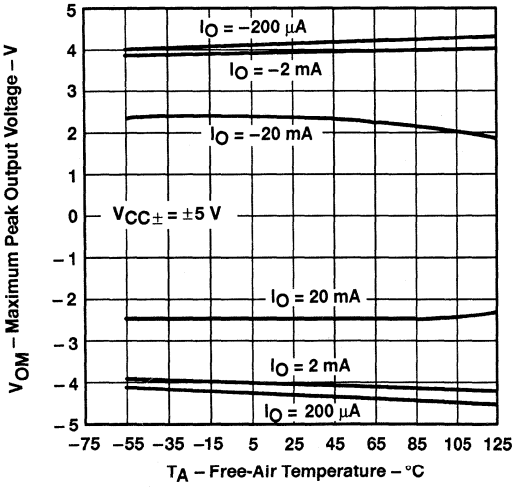


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

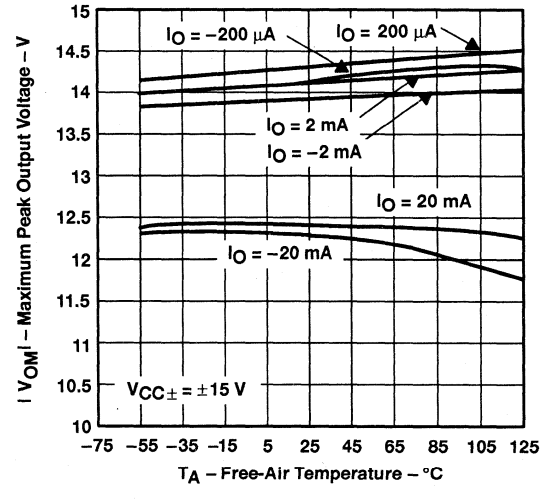


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

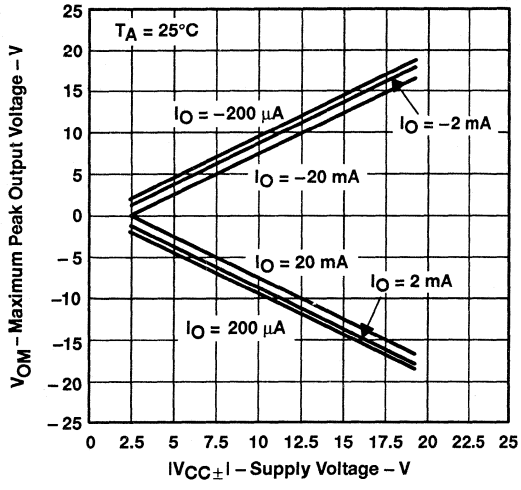


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

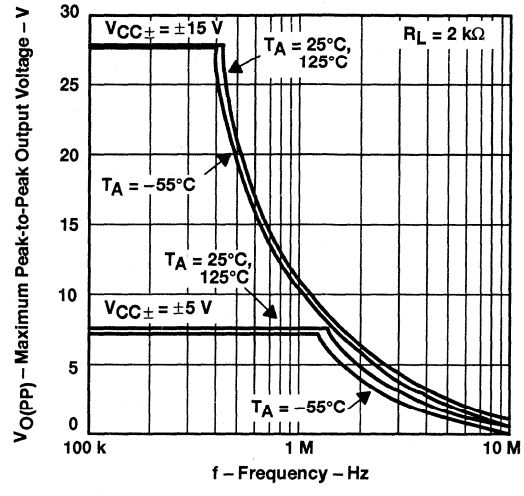


Figure 19

OUTPUT VOLTAGE
vs
SETTLING TIME

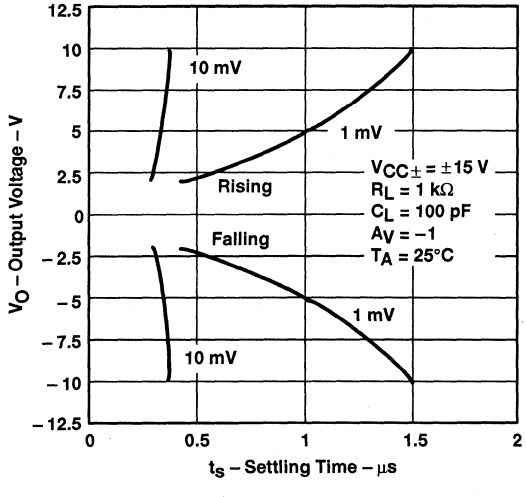


Figure 20

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

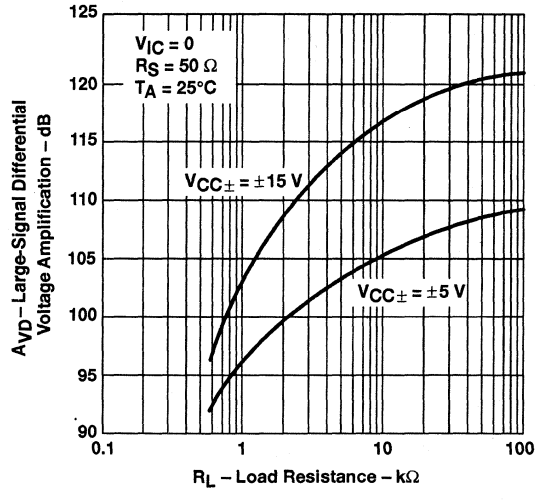


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

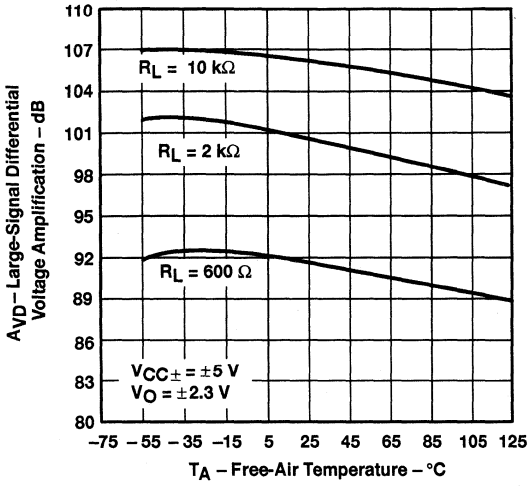


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

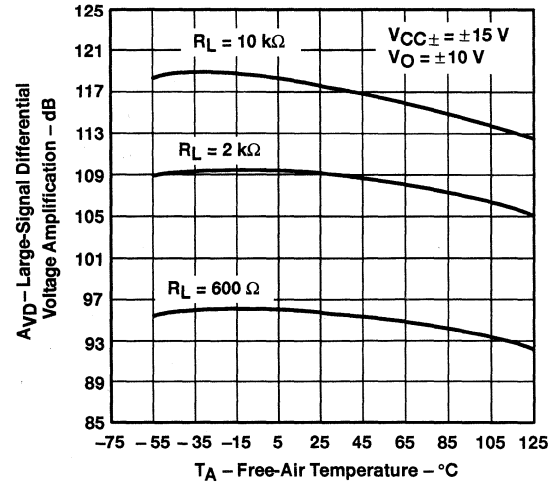


Figure 23

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

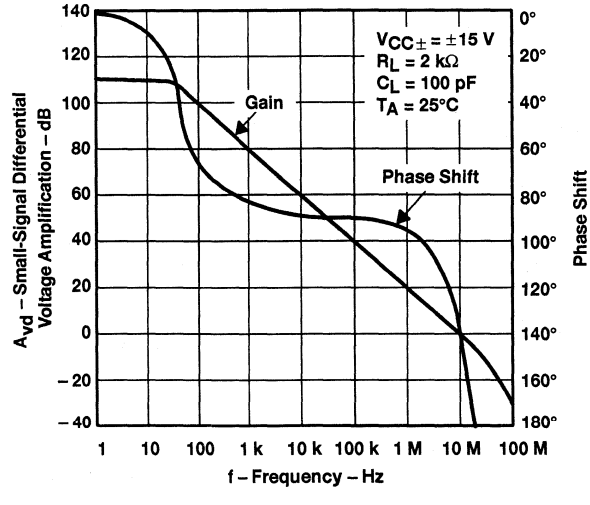


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

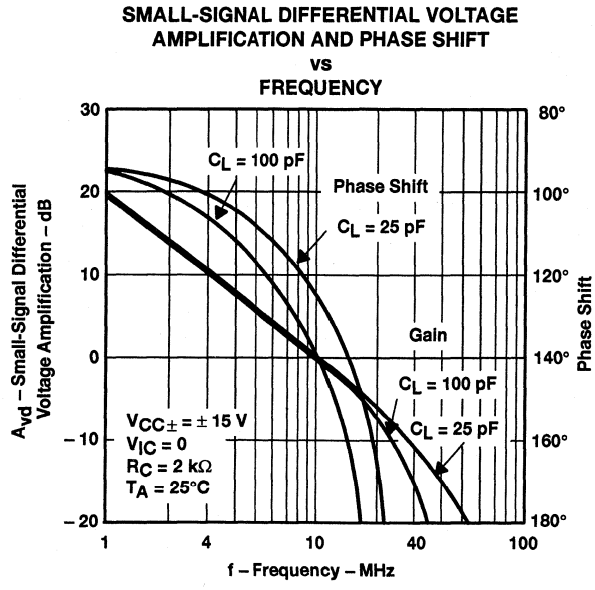


Figure 25

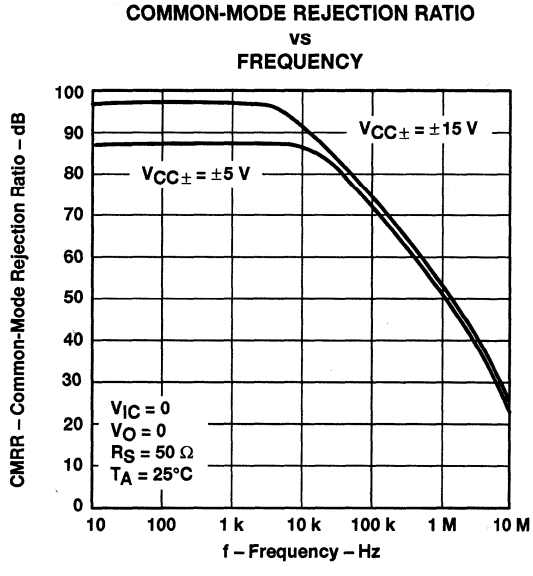


Figure 26

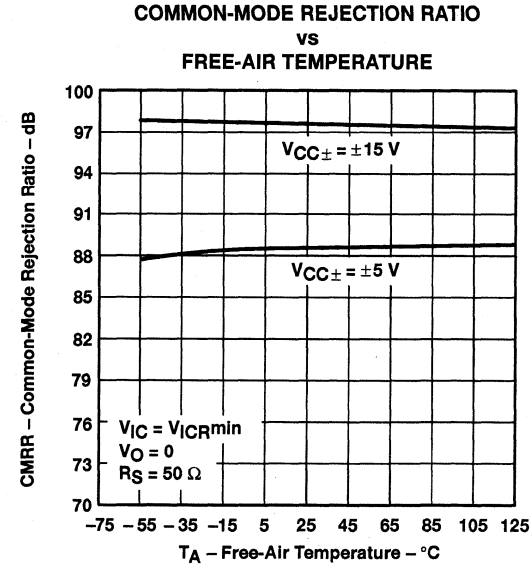


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

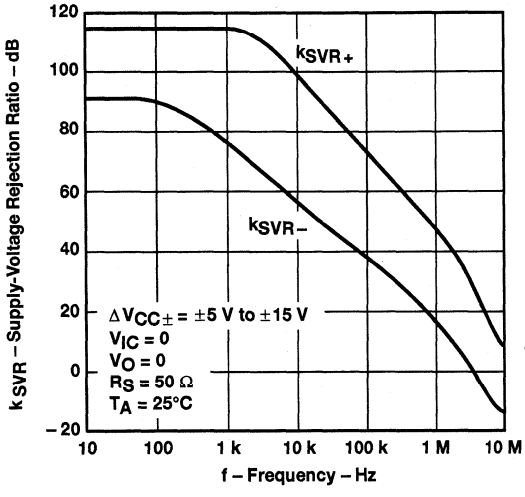


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

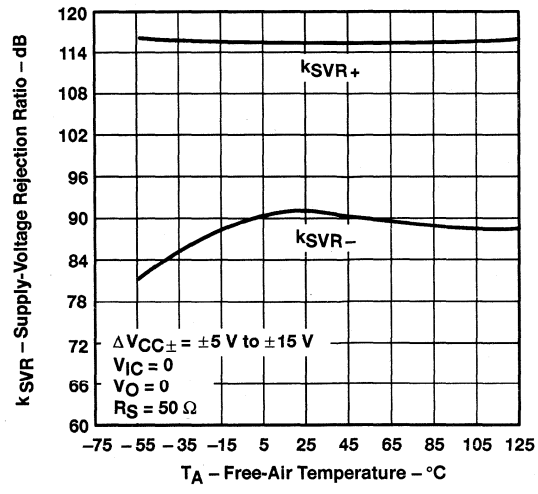


Figure 29

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

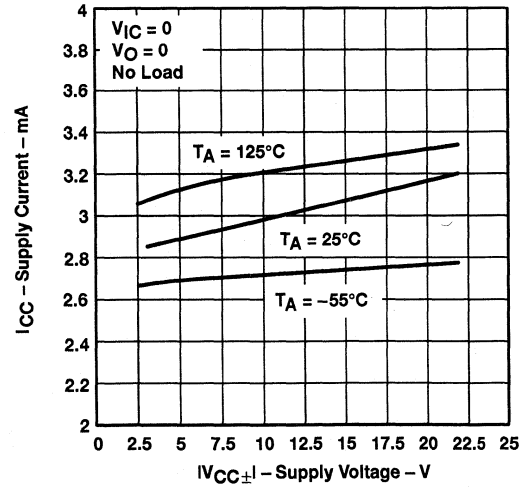


Figure 30

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

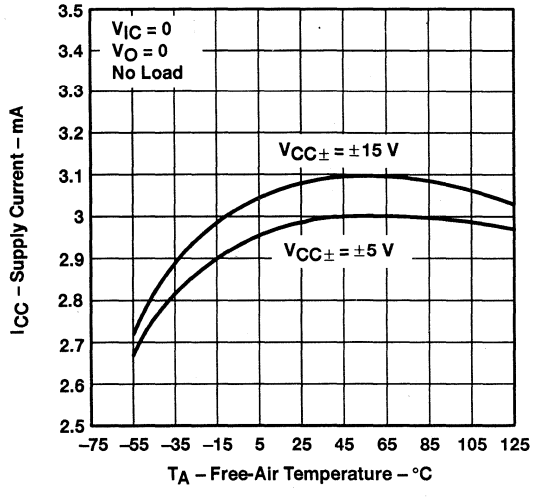


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

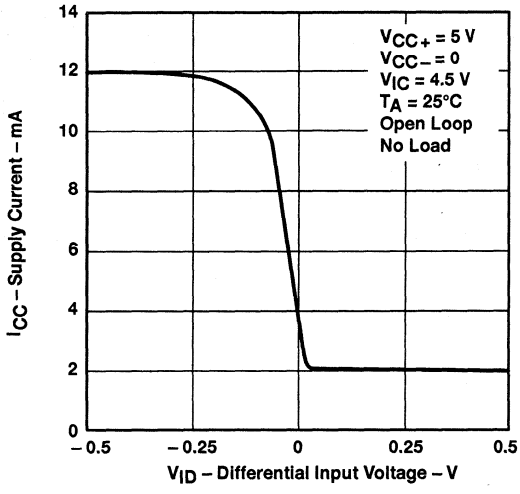


Figure 32

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

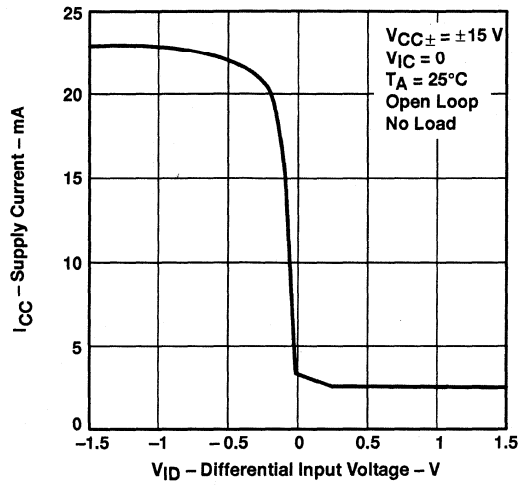


Figure 33

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

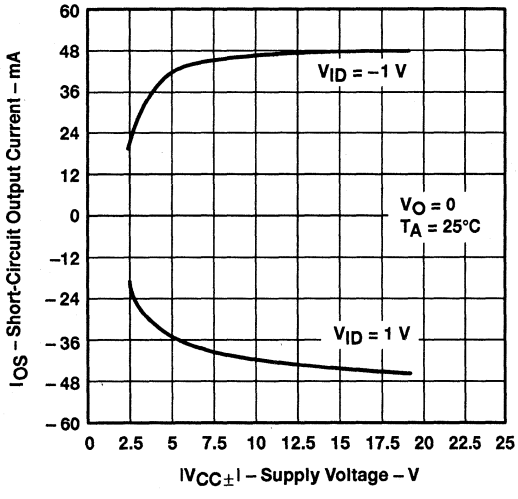


Figure 34

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

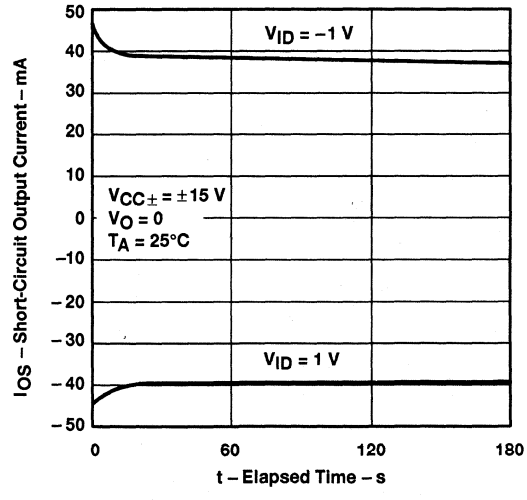


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

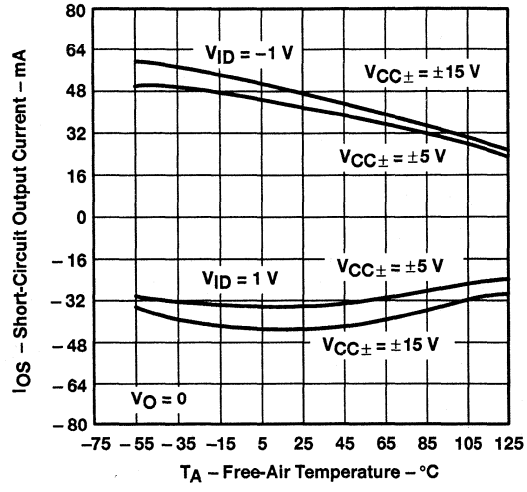


Figure 36

SLEW RATE vs FREE-AIR TEMPERATURE

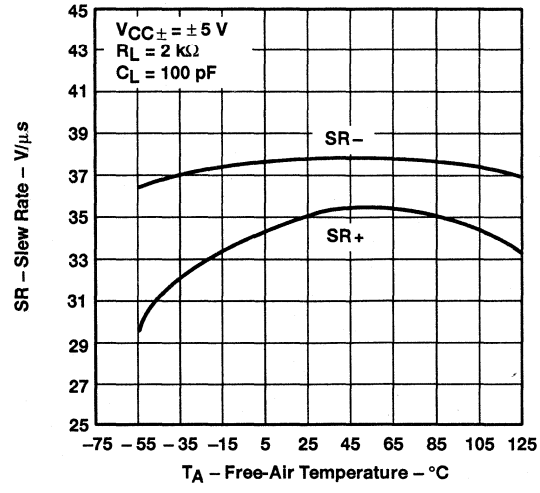


Figure 37

SLEW RATE vs FREE-AIR TEMPERATURE

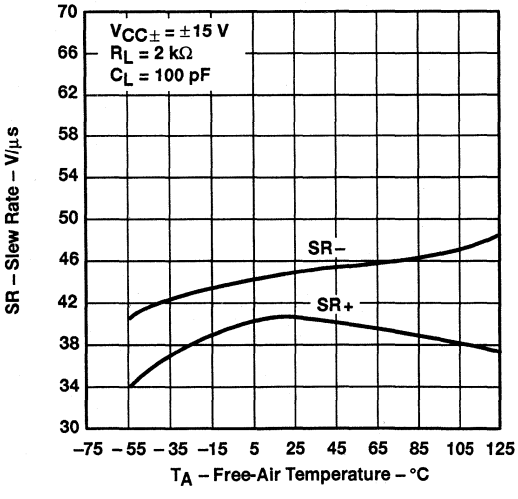


Figure 38

SLEW RATE vs LOAD RESISTANCE

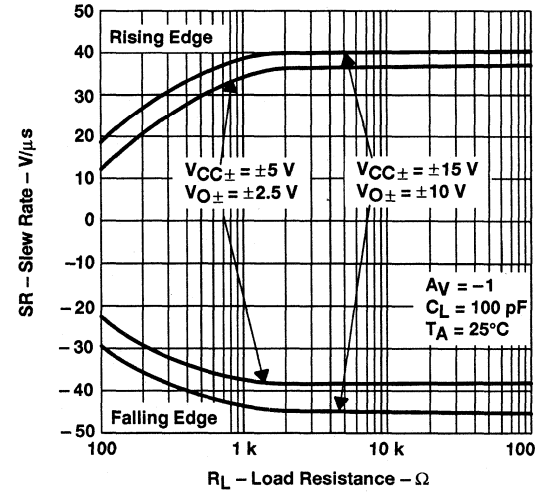


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

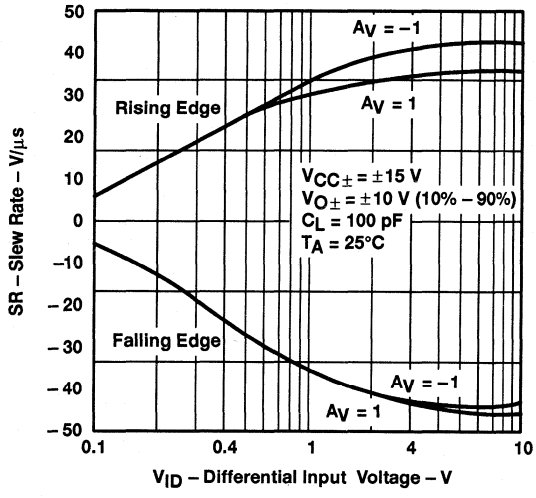


Figure 40

INPUT-REFERRED NOISE VOLTAGE SPECTRAL DENSITY vs FREQUENCY

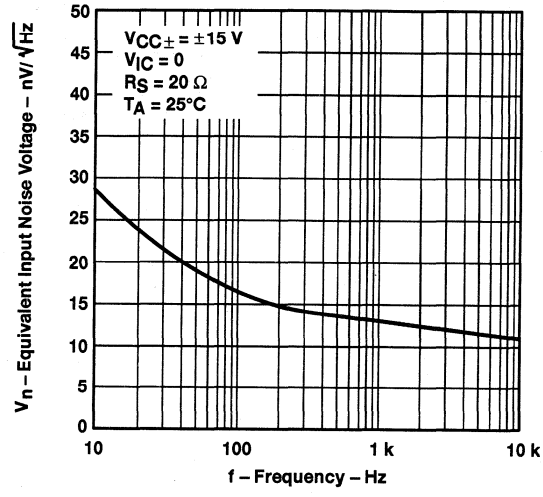


Figure 41

INPUT-REFERRED NOISE VOLTAGE vs NOISE BANDWIDTH

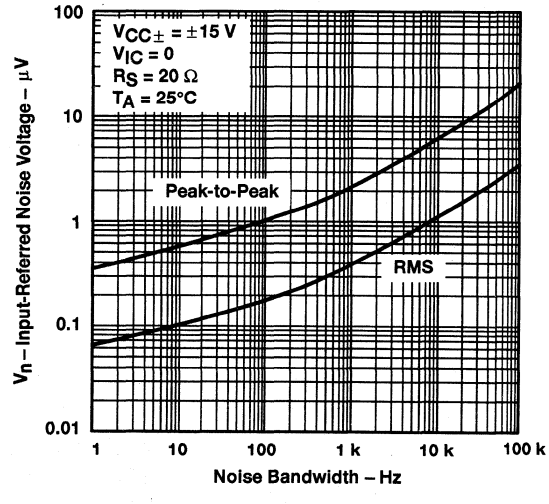


Figure 42

INPUT-REFERRED NOISE VOLTAGE OVER A 10-SECOND TIME INTERVAL

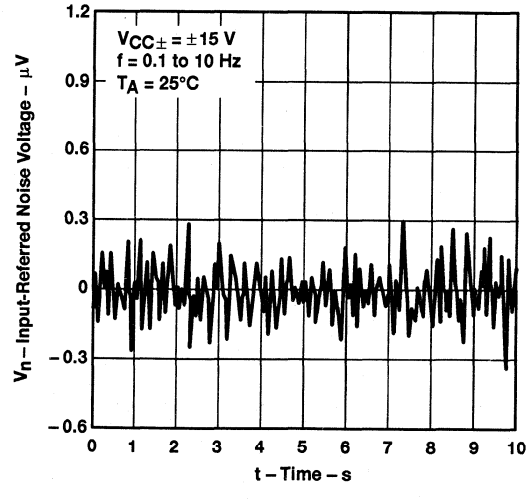


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

THIRD-OCTAVE SPECTRAL NOISE DENSITY
vs
FREQUENCY BANDS

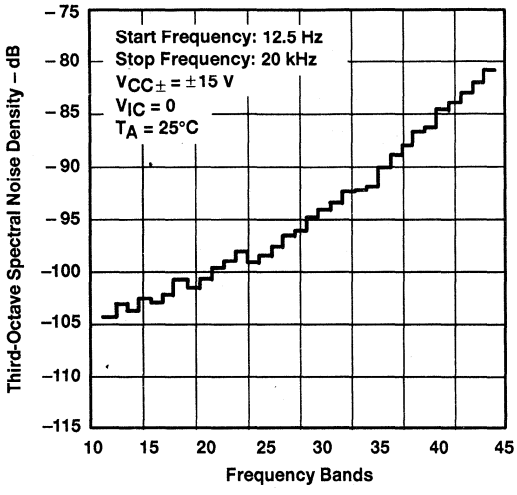


Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

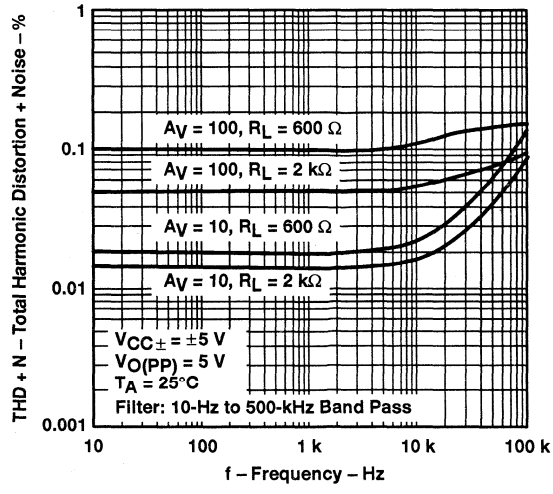


Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

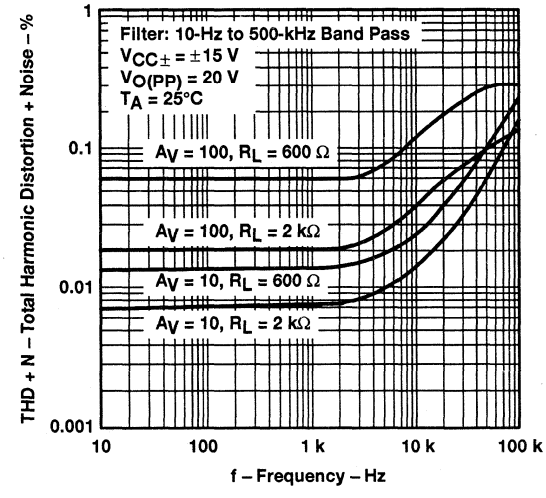


Figure 46

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

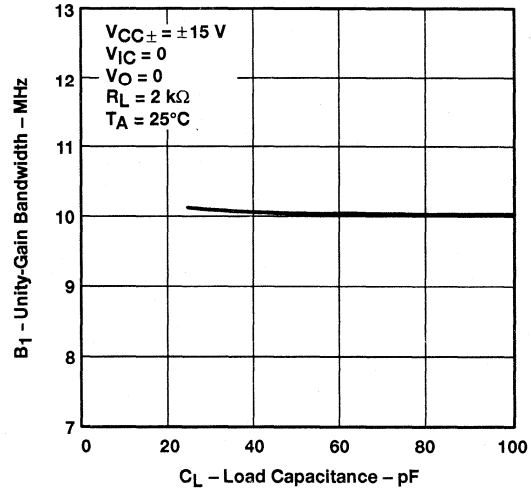


Figure 47

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

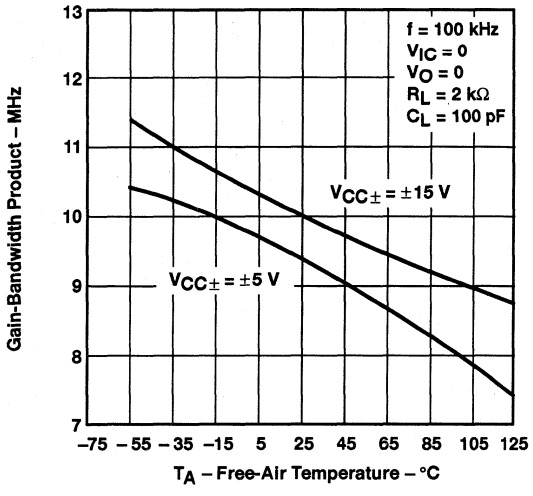


Figure 48

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

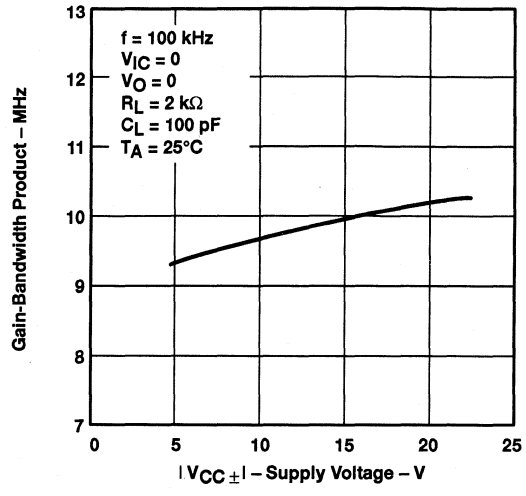


Figure 49

GAIN MARGIN vs LOAD CAPACITANCE

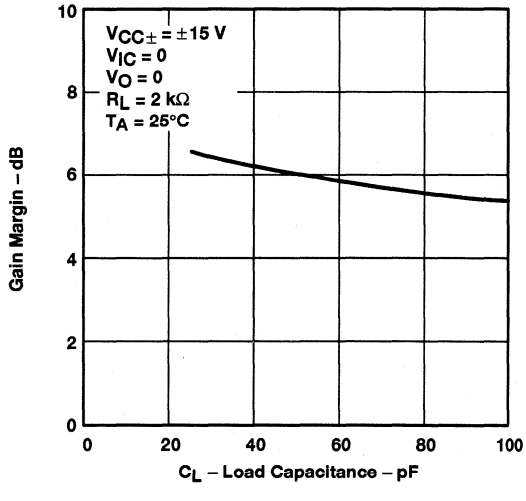


Figure 50

PHASE MARGIN vs FREE-AIR TEMPERATURE

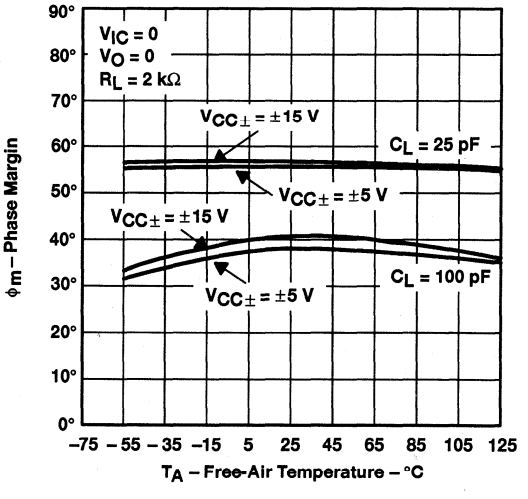


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

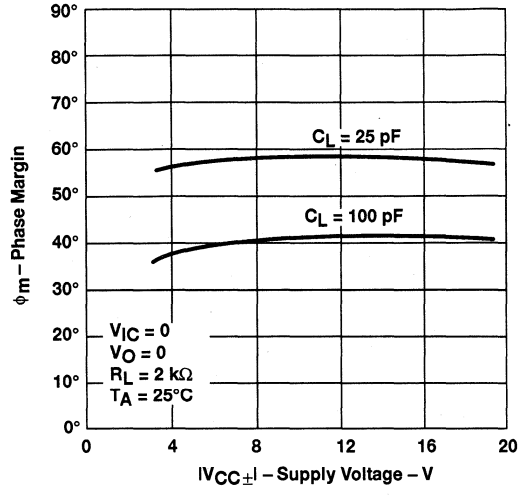


Figure 52

PHASE MARGIN
vs
LOAD CAPACITANCE

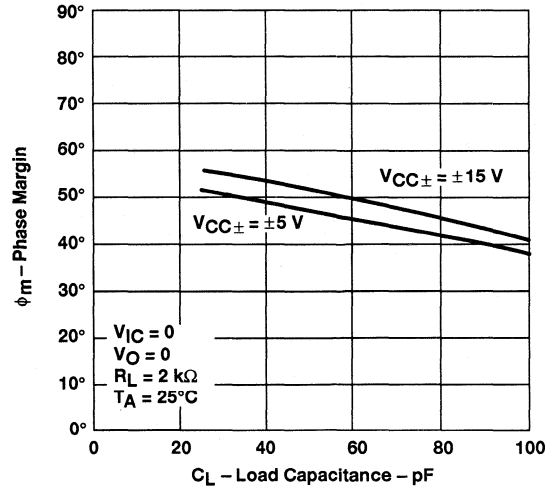


Figure 53

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

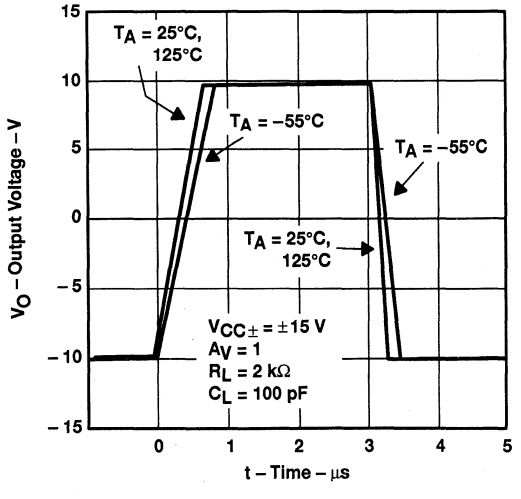


Figure 54

SMALL-SIGNAL PULSE RESPONSE

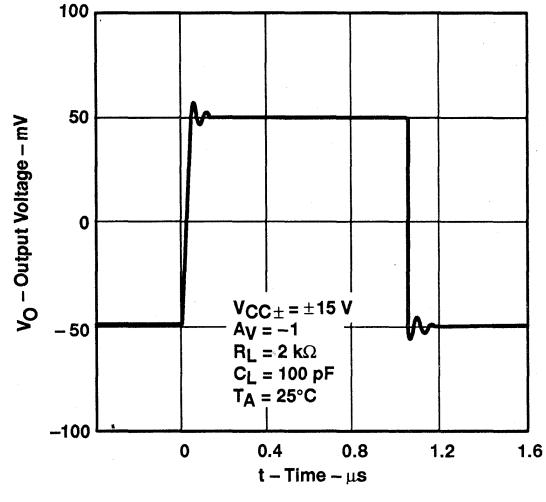


Figure 55

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

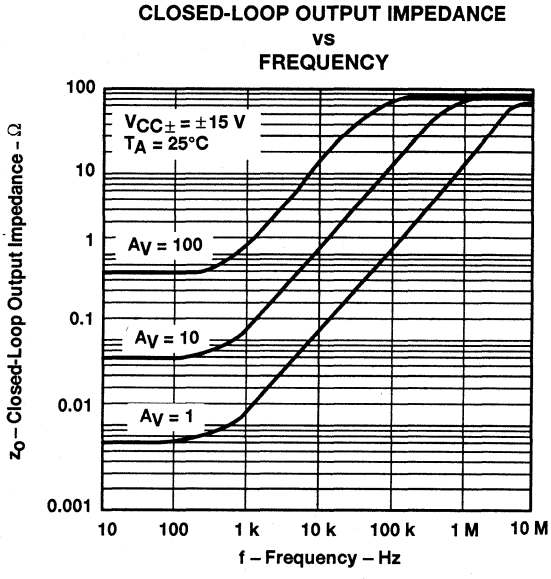


Figure 56

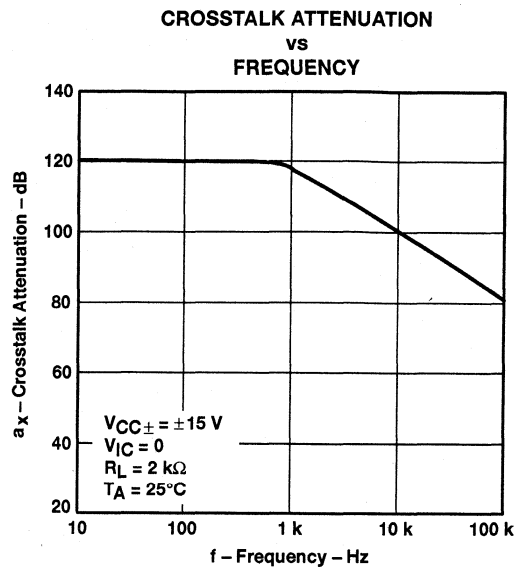


Figure 57

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

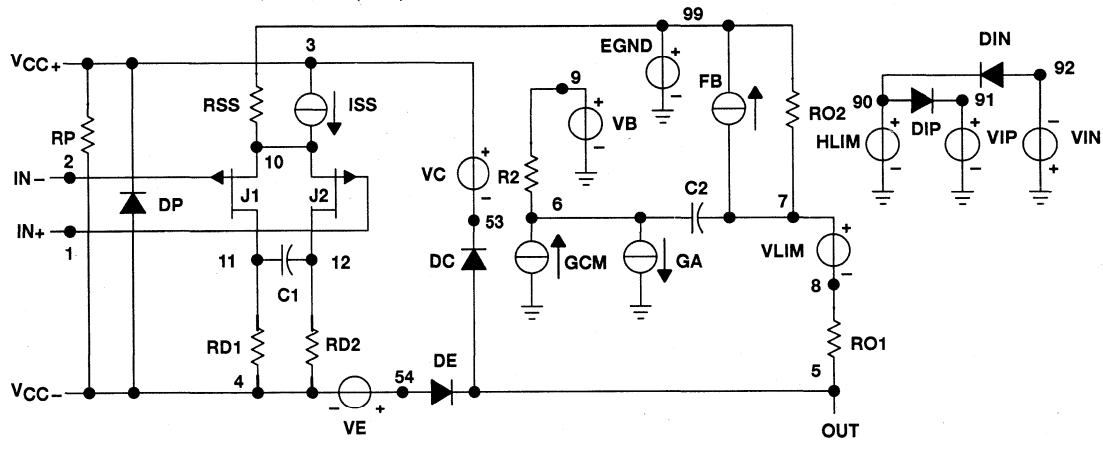
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 4) and subcircuit in Figure 58 were generated using the TLE2072 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G.R. Boyle, B.M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLE2072 1 2 3 4 5
C1      11      12      2.2E-12
C2      6       7       10.00E-12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
FB      7       99      POLY (5) VB VC VE VLP
+ VLN 0 5.607E6 –6E6 6E6 6E6 –6E6
GA      6       0       11 12 333.0E–6
GCM     0       6       10 99 7.43E–9
ISS     3       10      DC 400.0E–6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.0E3
RD1     4       11      3.003E3
RD2     4       12      3.003E3
R01     8       5       80
R02     7       99      80
RP      3       4       27.30E3
RSS     10      99      500.0E3
VB      9       0       DC 0
VC      3       53      DC 2.20
VE      54      4       DC 2.20
VLIM    7       8       DC 0
VLP     91      0       DC 45
VLN     0       92      DC 45
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=15.00E–12 BETA=554.5E–6
+ VTO=–.6)
.ENDS
```

Figure 58. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

- 25-V/μs Slew Rate Min
- Low Noise
  17 nV/√Hz Max at f = 10 kHz
  11.6 nV/√Hz Typ at f = 10 kHz
- High Gain-Bandwidth Product . . . 10 MHz
- ±30-mA Minimum Short-Circuit Output Current
- Wide Supply-Voltage Range
  ±2.25 V to ±19 V
- Input Range Includes the Positive Supply
- Macromodel Included
- Fast Settling Time Using 10-V Step
  400 ns to 10 mV Typ
  1.5 μs to 1 mV Typ

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

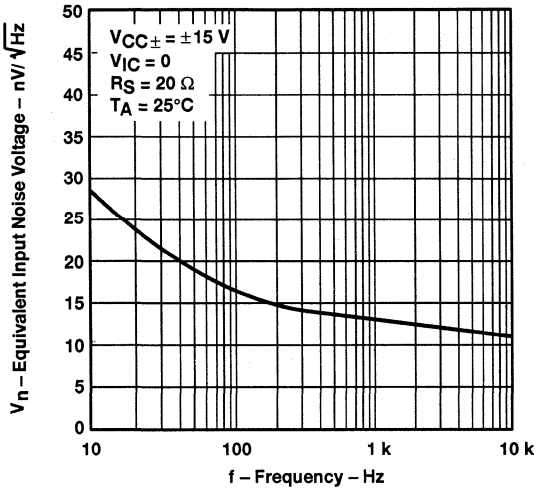


Figure 1

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

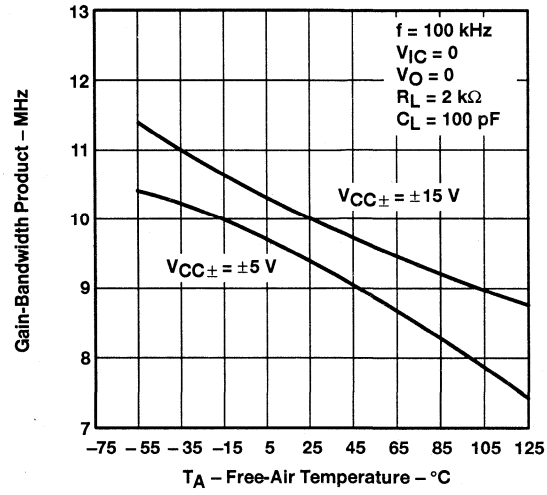


Figure 2

description

The TLE2074 and TLE2074A are low-noise, high-performance, high-speed, internally compensated JFET-input quadruple operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. These devices combine low noise (see Figure 1) with outstanding output drive capability, high slew rate, and wide bandwidth (see Figure 2).

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)‡
		SMALL OUTLINE (DW)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	3 mV 5 mV	TLE2074ACDW TLE2074CDW	—	—	TLE2074ACN TLE2074CN	— TLE2074Y
–40°C to 85°C	3 mV 5 mV	TLE2074AIDW TLE2074IDW	—	—	TLE2074AIN TLE2074IN	—
–55°C to 125°C	3 mV 5 mV	—	TLE2074AMFK TLE2074MFK	TLE2074AMJ TLE2074MJ	—	—

† The DW packages are available taped and reeled. Add R suffix to device type (e.g., TLE2074ACDWR).
‡ Chip-form versions are tested at T_A = 25°C. For chip-form orders, contact your local TI sales office.

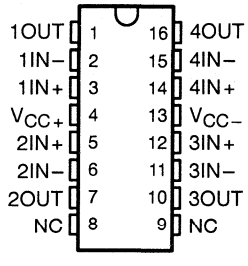
description (continued)

The design features a low audio-band noise of 11.6 nV/$\sqrt{\text{Hz}}$ typical at 10 kHz. This, coupled with a 25-V/μs minimum slew rate, results in the low distortion and high-power bandwidth necessary for high-fidelity audio applications. Settling time to 0.1% of a 10-V step (1-kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8 MHz minimum. As such, the TLE2074 and TLE2074A offer significant speed and noise advantages at a low 1.6-mA typical supply current per channel.

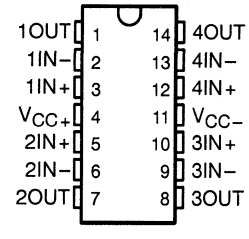
The input current characteristics traditionally associated with JFET-input amplifiers have been maintained. Input offset voltage is graded to a 7 mV and 4 mV maximum for the TLE2074 and TLE2074A, respectively. Typically, temperature coefficient of input offset voltage is 10.1 μV/°C and typical CMRR and k_{SVR} are 98 dB and 99 dB, respectively. Device performance is relatively independent of supply voltage over the wide ±2.25-V to ±19-V range. The input common-mode voltage range extends from the positive supply down to V_{CC-} + 4 V without significant degradation to dynamic performance. Maximum peak output voltage swing is from V_{CC+} – 1 V to V_{CC-} + 1 V under light loading conditions. The output is capable of sourcing and sinking a minimum of 30 mA and can sustain shorts to either supply. Care must be taken to ensure that maximum power dissipation is not exceeded.

Both the TLE2074 and TLE2074A are available in a wide variety of packages, including both the industry-standard 16-pin wide-body SOIC and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix devices over the –40°C to 85°C range, and the M-suffix devices over the full military temperature range of –55°C to 125°C.

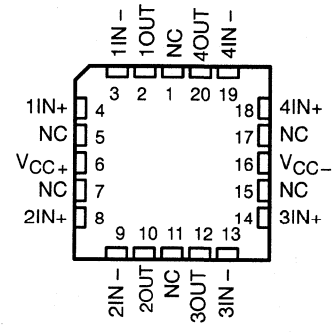
DW PACKAGE
(TOP VIEW)



J OR N PACKAGE
(TOP VIEW)

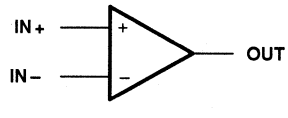


FK PACKAGE
(TOP VIEW)



NC – No internal connection

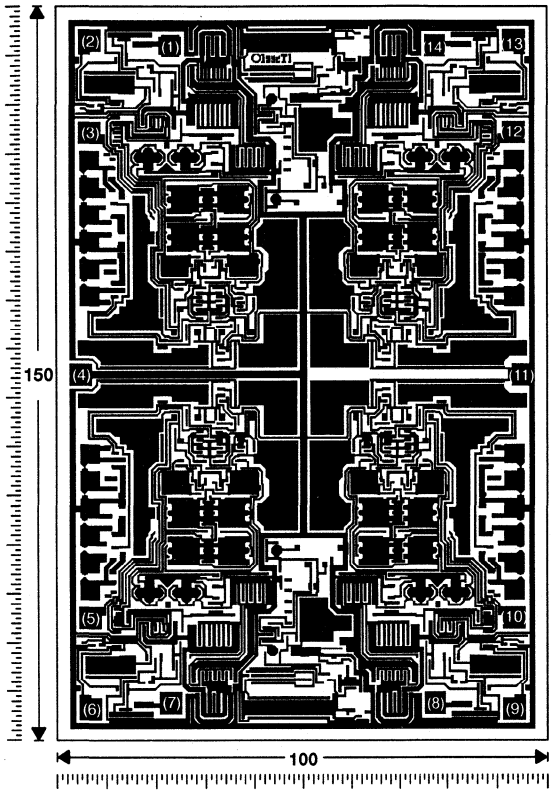
symbol

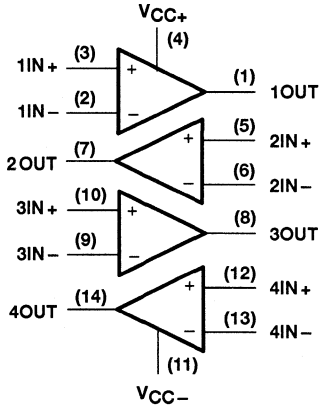


TLE2074Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2074. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

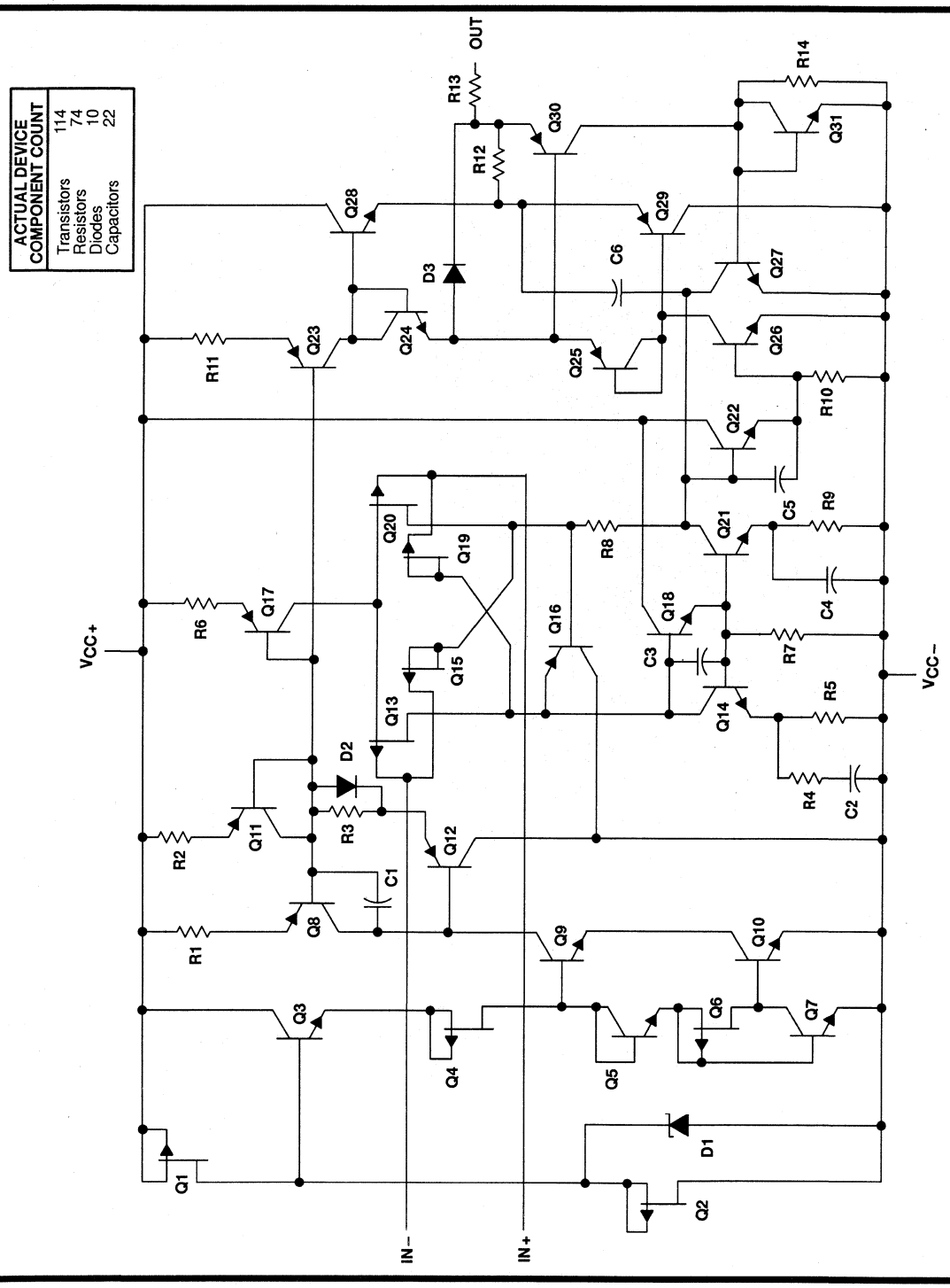
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} (see Note 1) ..... −19 V
Differential input voltage range, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-}
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2.25	±19	±2.25	±19	±2.25	±19	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−0.9	5	−0.8	5	−0.8	5	V
	$V_{CC\pm} = \pm15$ V	−10.9	15	−10.8	15	−10.8	15	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074C			TLE2074AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		−1.6	5		−0.5	3	mV
				Full range			7.1			5.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		10.1	30		10.1	30	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
				Full range			1400			1400	
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			5000			5000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.9			5 to −0.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.7			−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.4			−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance		V_{IC} = 0	25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5	25°C		11			11		pF
		Differential		25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz	25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074C			TLE2074AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.3	7.5	5.2	6.3	7.5	mA
				Full range			7.5			7.5	
a_X	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2074C			TLE2074AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074C			TLE2074AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		–1.6	5		–0.5	3	mV
				Full range			7.1			5.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		10.1	30		10.1	30	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
				Full range			1400			1400	
I_{IB}	Input bias current			25°C		25	175		25	175	pA
				Full range			5000			5000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to –11	15 to –11.9		15 to –11	15 to –11.9		V
				Full range	15 to –10.9			15 to –10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = –200 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = –2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = –20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	–13.8	–14.2		–13.8	–14.2		V
				Full range	–13.7			–13.7			
		I_O = 2 mA		25°C	–13.7	–14		–13.7	–14		
				Full range	–13.6			–13.6			
		I_O = 20 mA		25°C	–11.5	–12.4		–11.5	–12.4		
				Full range	–11.5			–11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance		V_{IC} = 0	25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5	25°C		7.5			7.5		pF
		Differential		25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz	25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	81			81			

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074C			TLE2074AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.5	7.5	5.2	6.5	7.5	mA
				Full range			7.5			7.5	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2074C			TLE2074AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	25	40		25	40		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	25			25			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074I			TLE2074AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		–1.6	5		–0.5	3	mV
				Full range			9			7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		10.1	30		10.1	30	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
				Full range			5			5	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			10			10	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to –1	5 to –1.9		5 to –1	5 to –1.9		V
				Full range	5 to –0.8			5 to –0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = –200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = –2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = –20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	–3.8	–4.2		–3.8	–4.2		V
				Full range	–3.7			–3.7			
		I_O = 2 mA		25°C	–3.5	–4.1		–3.5	–4.1		
				Full range	–3.4			–3.4			
		I_O = 20 mA		25°C	–1.5	–2.4		–1.5	–2.4		
				Full range	–1.5			–1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance, Common mode	V_{IC} = 0, See Figure 5		25°C		11			11		pF
	Input capacitance, Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is –40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074I			TLE2074AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.3	7.5	5.2	6.3	7.5	mA
				Full range			7.5			7.5	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2074I			TLE2074AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	20			20			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074I			TLE2074AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,	25°C		–1.6	5		–0.5	3	mV
				Full range			9			7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		10.1	30		10.1	30	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, See Figure 4	V_O = 0,	25°C		15	100		15	100	pA
				Full range			5			5	nA
I_{IB}	Input bias current			25°C		25	175		25	175	pA
				Full range			10			10	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to –11	15 to –11.9		15 to –11	15 to –11.9		V
				Full range	15 to –10.8			15 to –10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = –200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = –2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = –20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	–13.8	–14.2		–13.8	–14.2		V
				Full range	–13.7			–13.7			
		I_O = 2 mA		25°C	–13.5	–14		–13.5	–14		
				Full range	–13.4			–13.4			
		I_O = 20 mA		25°C	–11.5	–12.4		–11.5	–12.4		
				Full range	–11.5			–11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5	25°C		7.5			7.5		pF
		Differential		25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is –40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074I			TLE2074AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.5	7.5	5.2	6.5	7.5	mA
				Full range			7.5			7.5	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2074I			TLE2074AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±10 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C	25	40		25	40		V/μs
				Full range	19			19			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55		28	55	nV/√Hz
			f = 10 kHz			11.6	17		11.6	17	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLE2074M			TLE2074AM			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50Ω		25°C		−1.6	5		−0.5	3	mV
					Full range			10.5			8.5	
α_{VIO}	Temperature coefficient of input offset voltage				Full range		10.1	30*		10.1	30*	µV/°C
I_{IO}	Input offset current		V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
					Full range			20			20	nA
I_{IB}	Input bias current				25°C		20	175		20	175	pA
					Full range			65			65	nA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
					Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing		I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
					Full range	3.6			3.6			
			I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
					Full range	3.3			3.3			
			I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
					Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
					Full range	−3.6			−3.6			
			I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
					Full range	−3.3			−3.3			
			I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
					Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
					Full range	78			78			
				R_L = 2 kΩ	25°C	90	100		90	100		
					Full range	88			88			
				R_L = 10 kΩ	25°C	95	106		95	106		
					Full range	93			93			
r_i	Input resistance		V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5		25°C		11			11		pF
		Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
					Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
					Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074M			TLE2074AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.3	7.5	5.2	6.3	7.5	mA
				Full range			7.5			7.5	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2074M			TLE2074AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	18*			18*			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	18*			18*			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55*		28	55*	nV/√Hz
			f = 10 kHz			11.6	17*		11.6	17*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLE2074M			TLE2074AM			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		−1.6	5		−0.5	3	mV
					Full range			10.5			8.5	
α_{VIO}	Temperature coefficient of input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω		Full range		10.1	30*		10.1	30*	µV/°C
I_{IO}	Input offset current		V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
					Full range			20			20	nA
I_{IB}	Input bias current				25°C		25	175		25	175	pA
					Full range			65			65	nA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
					Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing		I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
					Full range	13.6			13.6			
			I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
					Full range	13.3			13.3			
			I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
					Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
					Full range	−13.6			−13.6			
			I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
					Full range	−13.3			−13.3			
			I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
					Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
					Full range	78			78			
				R_L = 2 kΩ	25°C	90	109		90	109		
					Full range	88			88			
				R_L = 10 kΩ	25°C	95	118		95	118		
					Full range	93			93			
r_i	Input resistance		V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5		25°C		7.5			7.5		pF
		Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
					Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
					Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2074M			TLE2074AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C	5.2	6.5	7.5	5.2	6.5	7.5	mA
				Full range			7.5			7.5	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

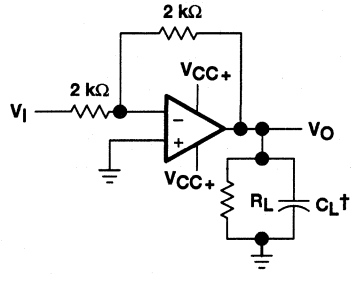
PARAMETER		TEST CONDITIONS		T_A†	TLE2074M			TLE2074AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	25	40		25	40		V/μs
				Full range	17			17			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28	55*		28	55*	nV/√Hz
			f = 10 kHz			11.6	17*		11.6	17*	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8*	10		8*	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478*	637		478*	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

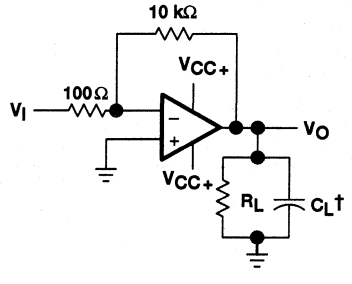
PARAMETER			TEST CONDITIONS		TLE2074Y MIN	TLE2074Y TYP	TLE2074Y MAX	UNIT
V_{IO}	Input offset voltage		V_{IC} = 0, R_S = 50 Ω	V_O = 0,			5	mV
I_{IO}	Input offset current		V_{IC} = 0, See Figure 4	V_O = 0,		15	100	pA
I_{IB}	Input bias current					25	175	pA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω		15 to −11	15 to 11.9		V
V_{OM+}	Maximum positive peak output voltage swing		I_O = −200 µA		13.8	14.1		V
			I_O = −2 mA		13.5	13.9		
			I_O = −20 mA		11.5	12.3		
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA		−13.8	−14.2		V
			I_O = 2 mA		−13.5	−14		
			I_O = 20 mA		−11.5	−12.4		
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V	R_L = 600 Ω	80	96		dB
				R_L = 2 kΩ	90	109		
				R_L = 10 kΩ	95	118		
r_i	Input resistance		V_{IC} = 0			10^{12}		Ω
c_i	Input capacitance	Common mode	V_O = 0, See Figure 5			7.5		pF
		Differential				2.5		
z_o	Open-loop output impedance		f = 1 MHz			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	V_O = 0,	80	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0,	R_S = 50 Ω	82	99		dB
I_{CC}	Supply current (four amplifiers)		V_O = 0,	No load	5.2	6.5	7.5	mA
I_{OS}	Short-circuit output current		V_O = 0	V_{ID} = 1 V	−30	−45		mA
				V_{ID} = −1 V	30	48		

PARAMETER MEASUREMENT INFORMATION



† Includes fixture capacitance

Figure 3. Slew-Rate Test Circuit



† Includes fixture capacitance

Figure 4. Unity-Gain Bandwidth and Phase-Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION

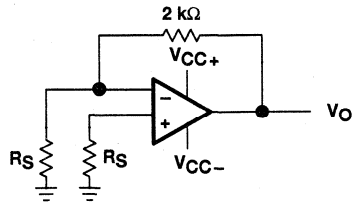


Figure 5. Noise-Voltage Test Circuit

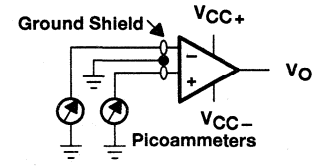


Figure 6. Input-Bias and Offset-Current Test Circuit

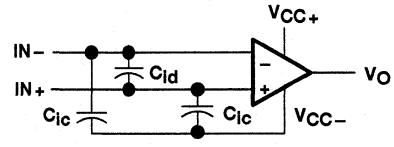


Figure 7. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TLE2074 and TLE2074A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
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	Crosstalk attenuation	vs Frequency	59

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLE2074
INPUT OFFSET VOLTAGE

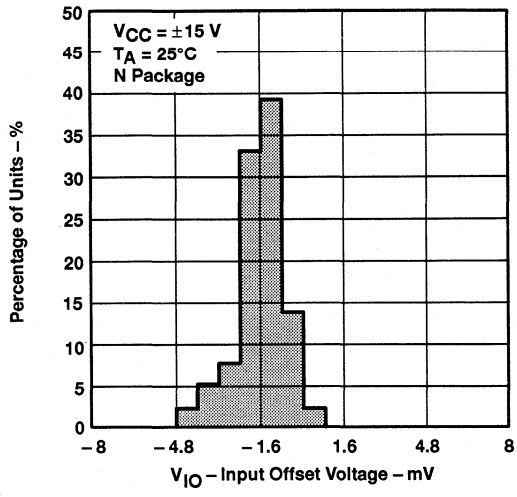


Figure 8

DISTRIBUTION OF TLE2074 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

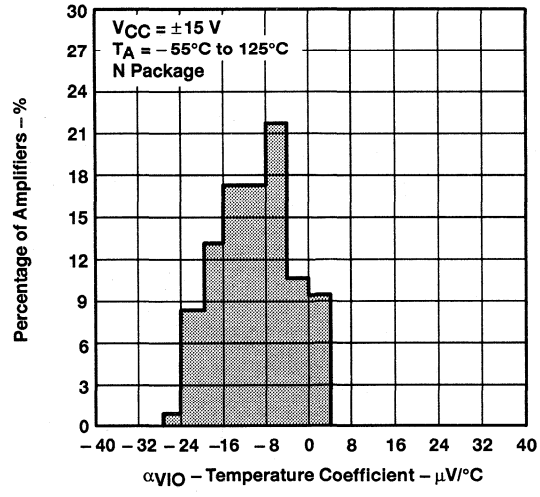


Figure 9

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

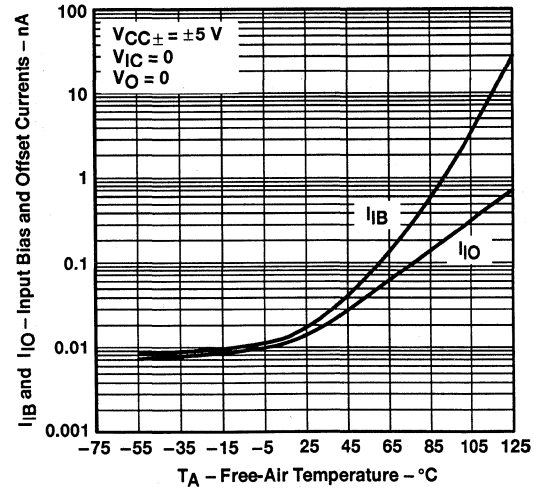


Figure 10

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

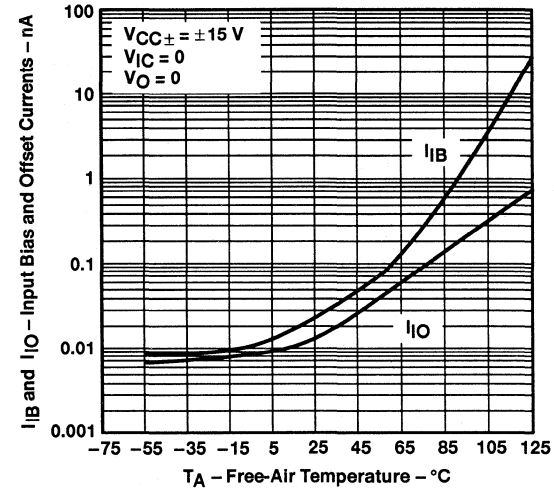


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs TOTAL SUPPLY VOLTAGE

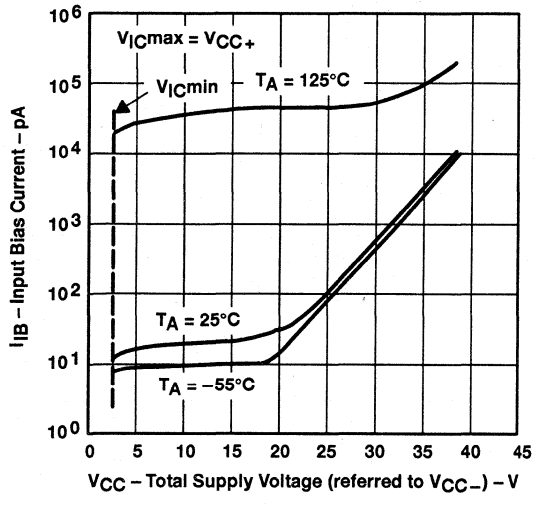


Figure 12

COMMON-MODE INPUT VOLTAGE RANGE vs FREE-AIR TEMPERATURE

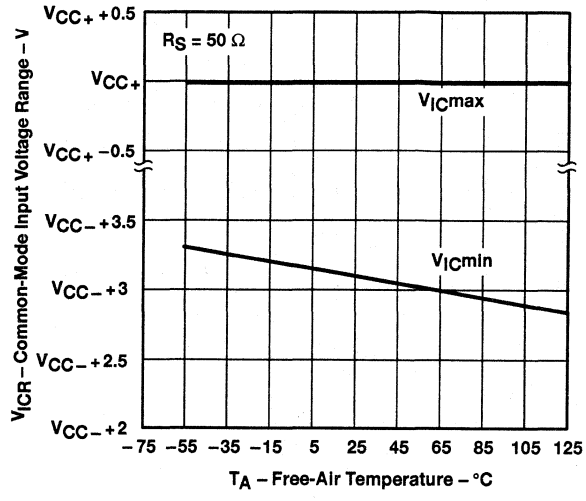


Figure 13

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

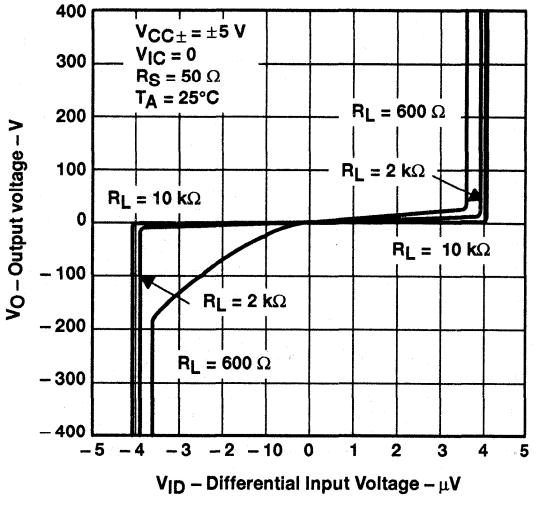


Figure 14

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

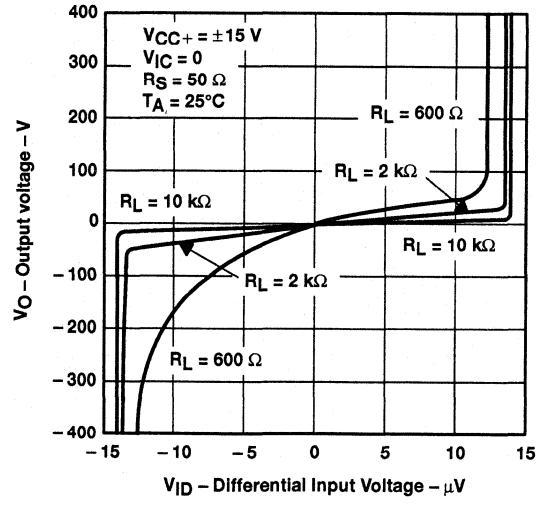


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

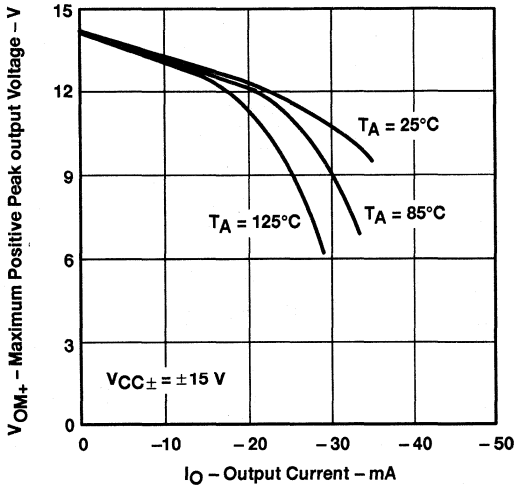


Figure 16

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

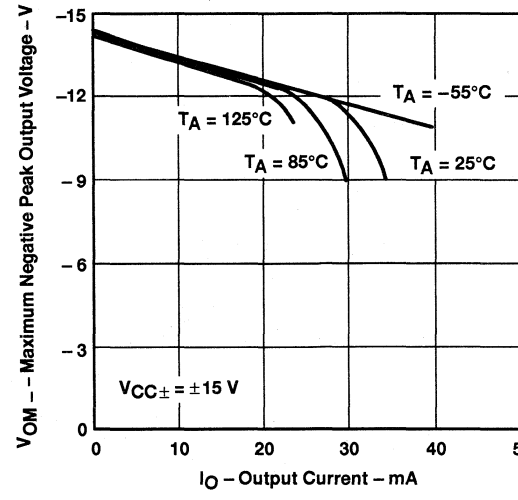


Figure 17

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

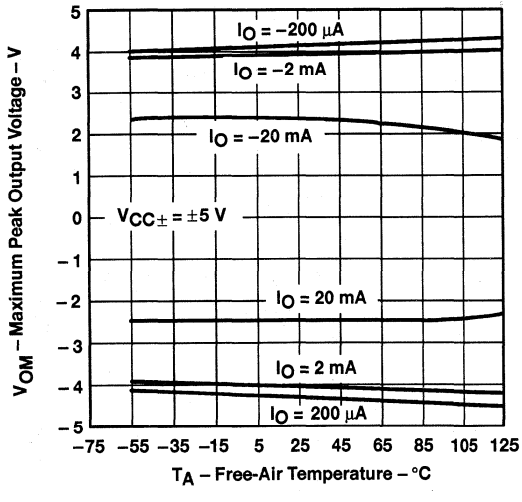


Figure 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

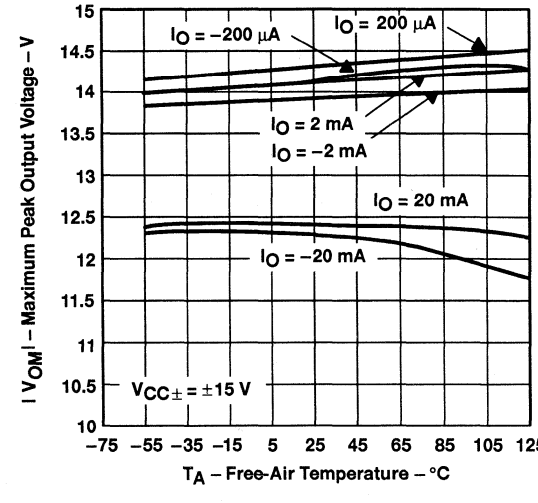


Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

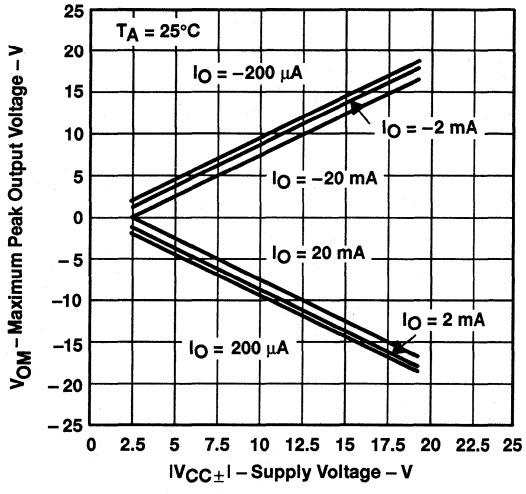


Figure 20

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

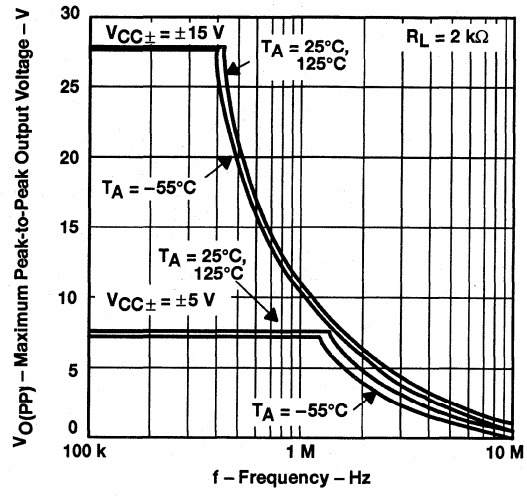


Figure 21

OUTPUT VOLTAGE
vs
SETTLING TIME

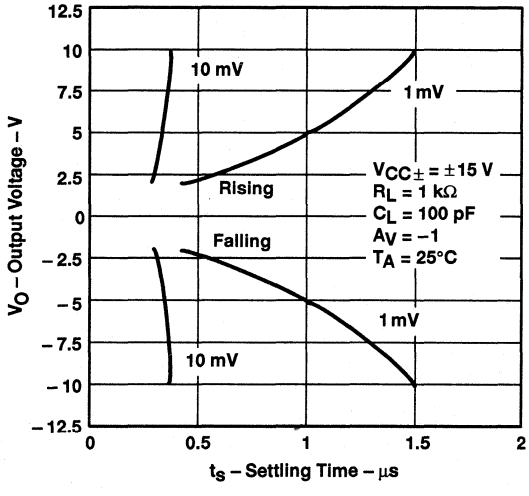


Figure 22

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

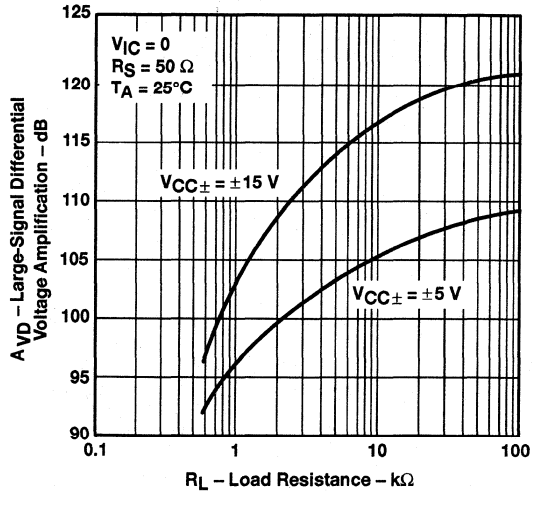


Figure 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

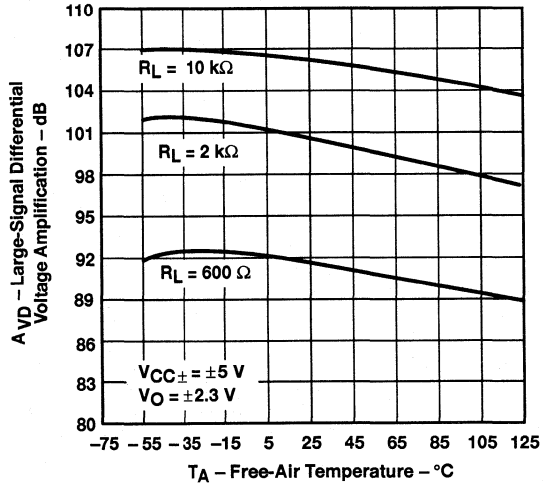


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

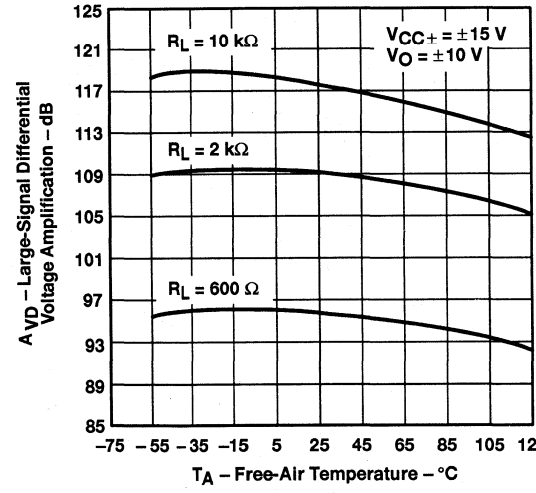


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

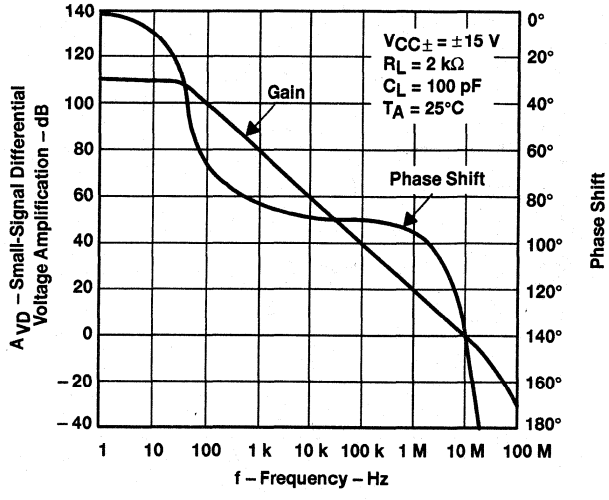


Figure 26

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

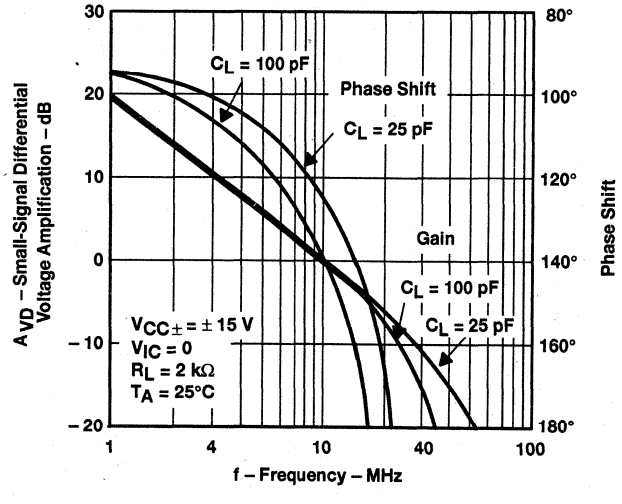


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

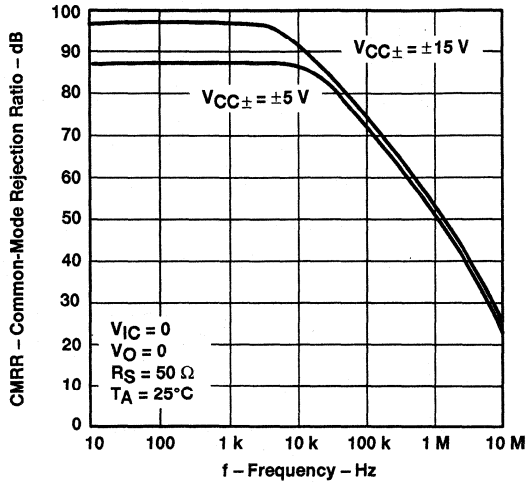


Figure 28

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

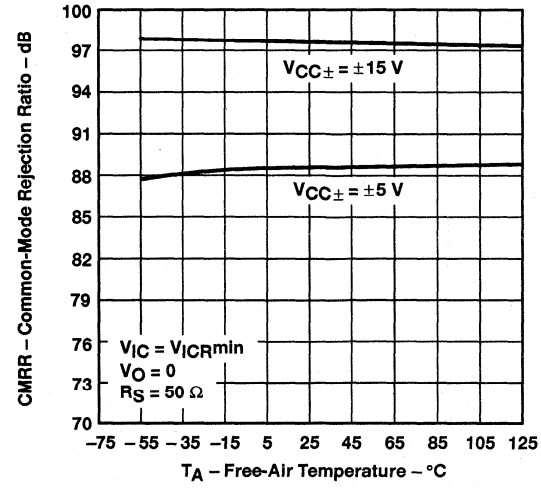


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

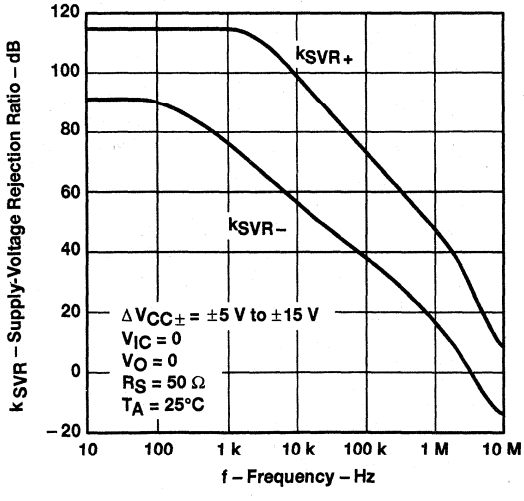


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

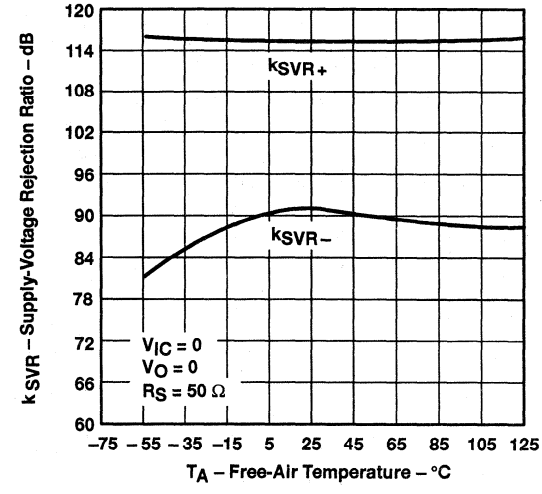


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

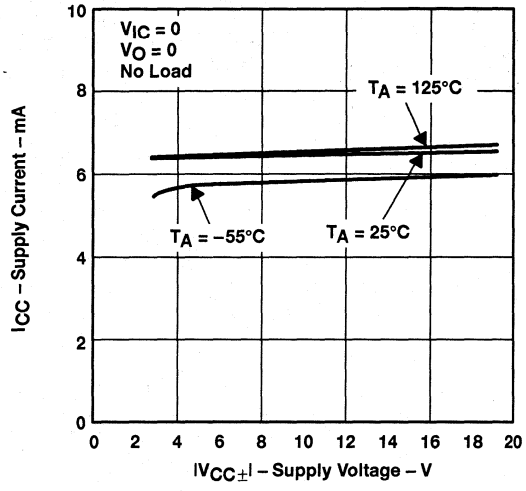


Figure 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

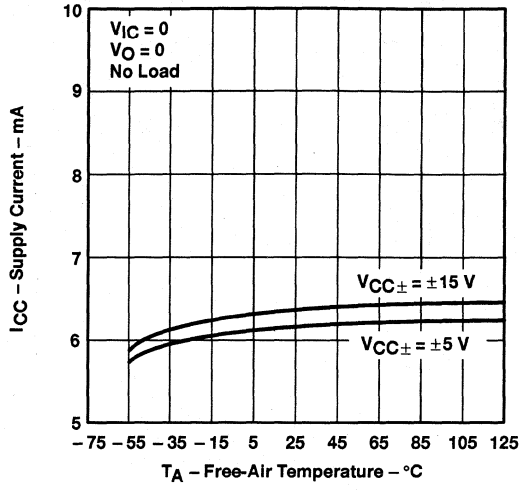


Figure 33

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

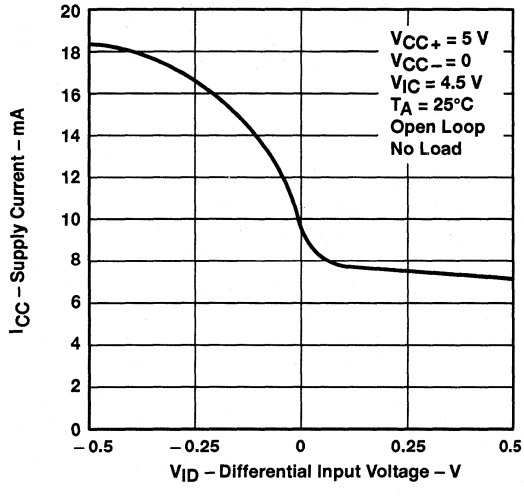


Figure 34

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

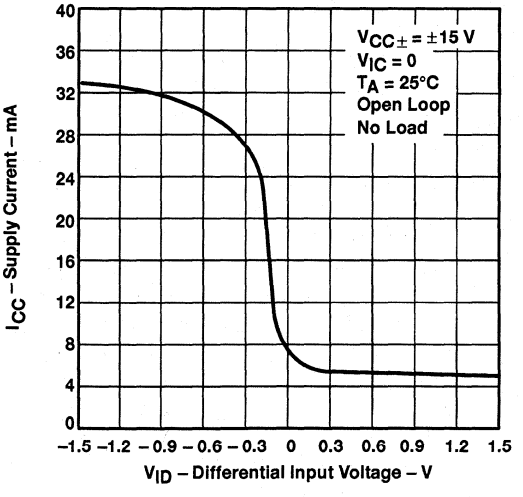


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

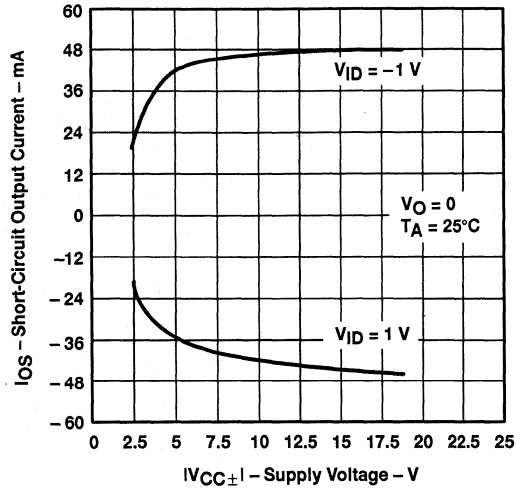


Figure 36

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

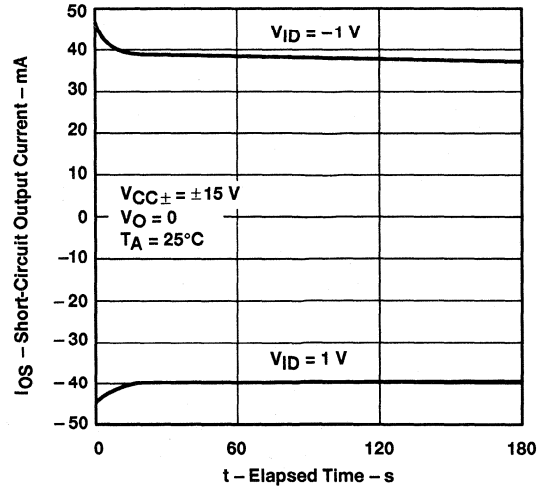


Figure 37

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

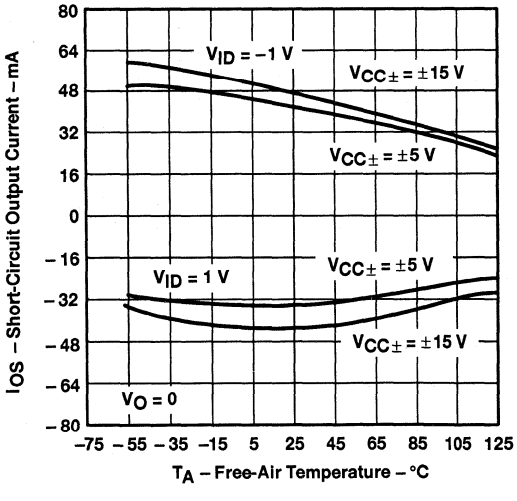


Figure 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

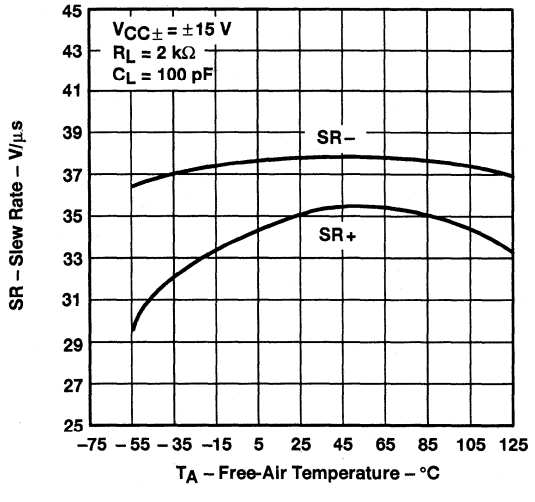


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs FREE-AIR TEMPERATURE

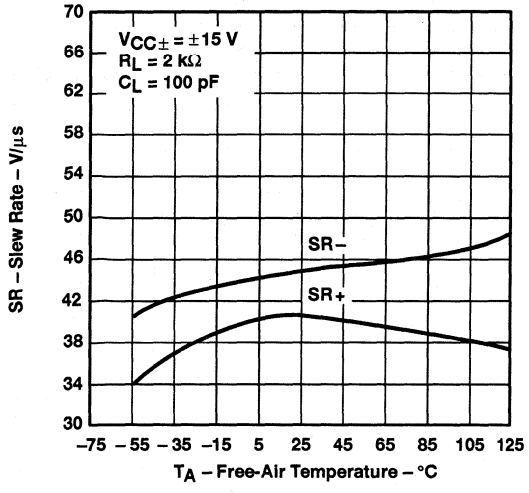


Figure 40

SLEW RATE vs LOAD RESISTANCE

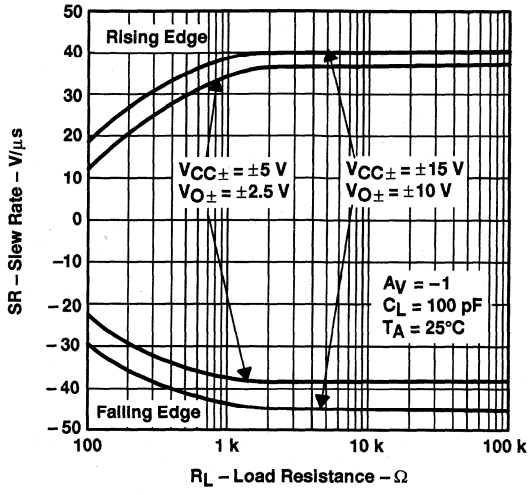


Figure 41

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

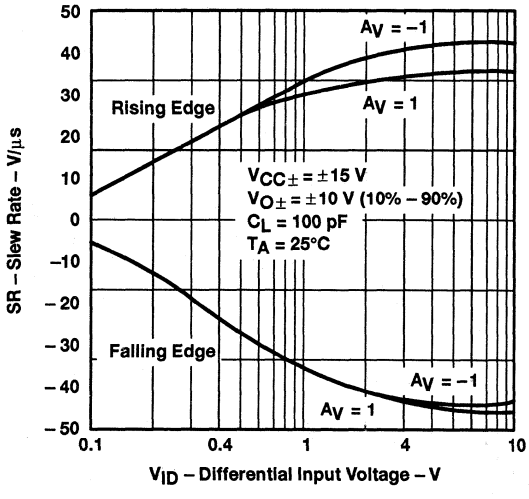


Figure 42

EQUIVALENT INPUT NOISE VOLTAGE (SPECTRAL DENSITY) vs FREQUENCY

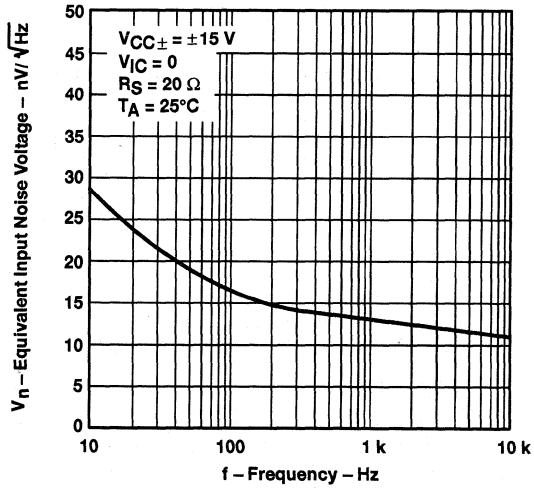


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT-REFERRED NOISE VOLTAGE
vs
NOISE BANDWIDTH

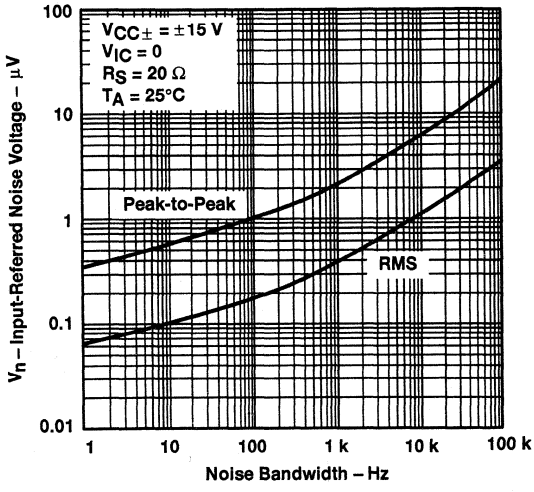


Figure 44

INPUT-REFERRED NOISE VOLTAGE
OVER A 10-SECOND TIME INTERVAL

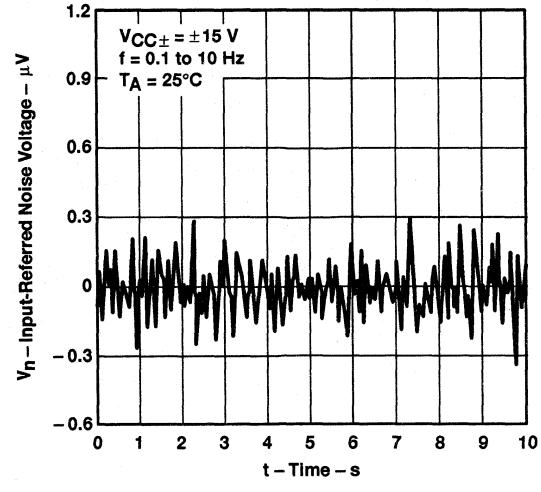


Figure 45

THIRD-OCTAVE SPECTRAL NOISE DENSITY
vs
FREQUENCY

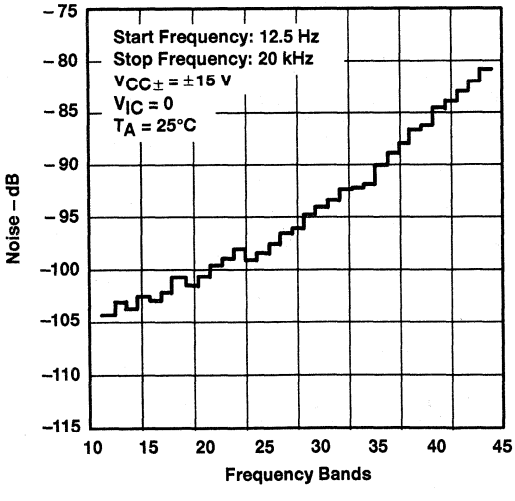


Figure 46

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

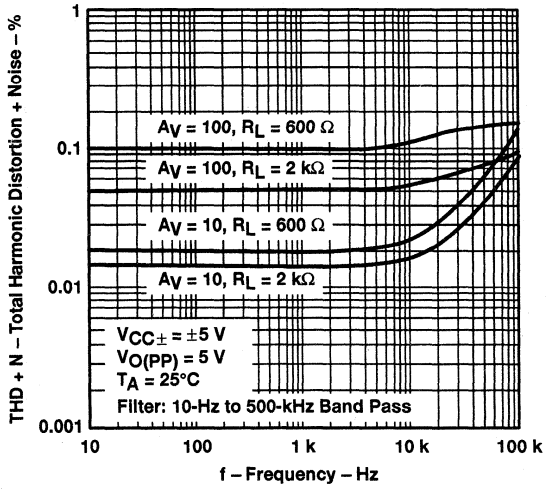


Figure 47

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

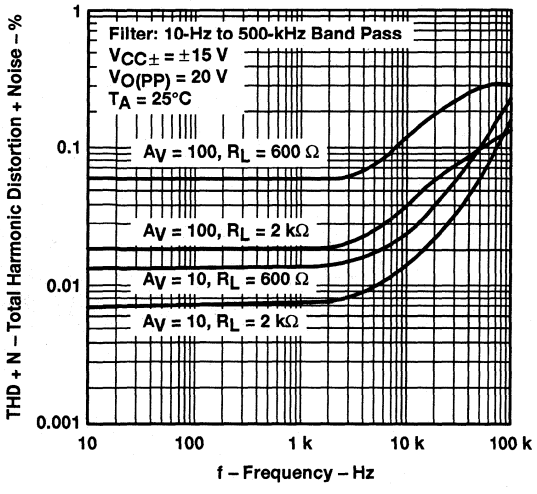


Figure 48

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

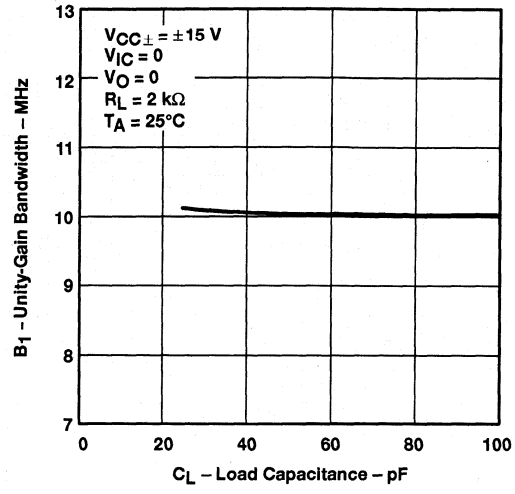


Figure 49

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

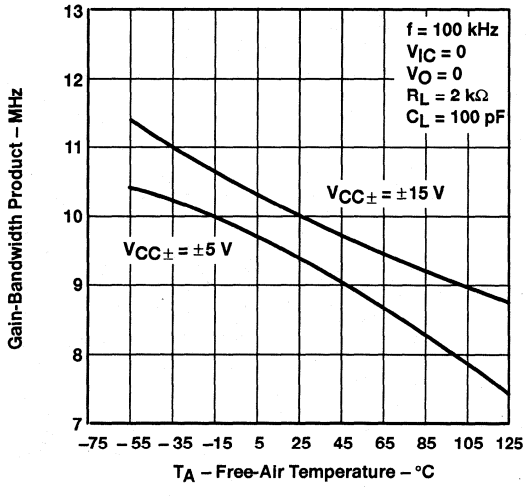


Figure 50

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

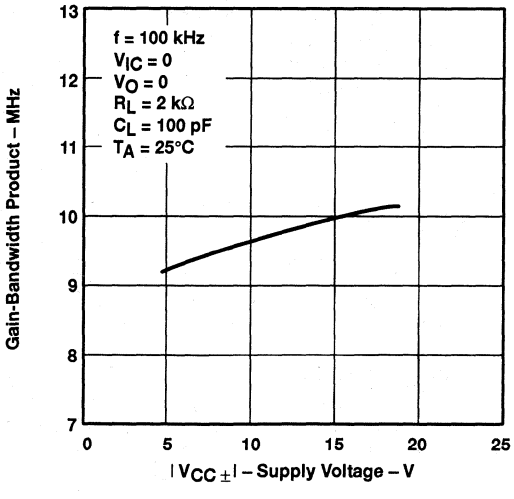


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

GAIN MARGIN
vs
LOAD CAPACITANCE

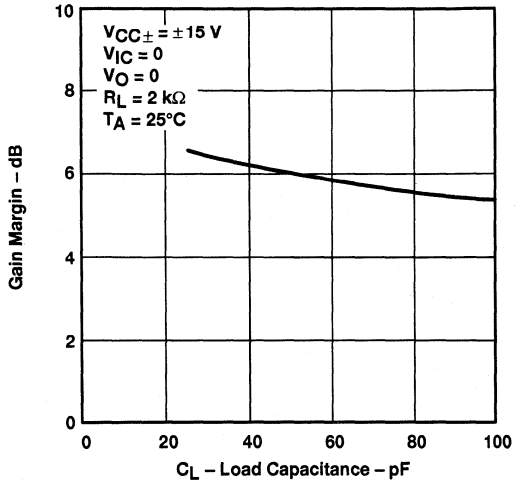


Figure 52

PHASE MARGIN
vs
TEMPERATURE

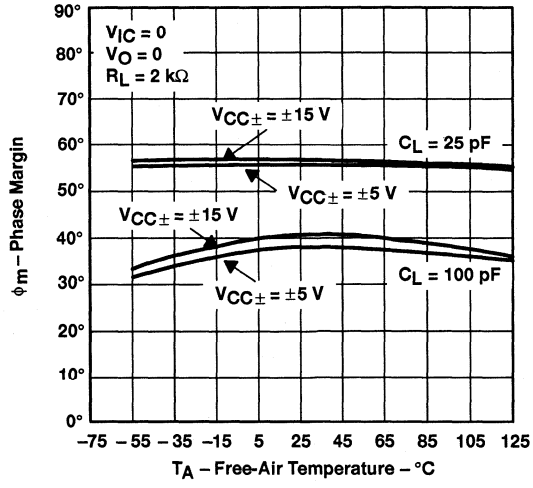


Figure 53

PHASE MARGIN
vs
SUPPLY VOLTAGE

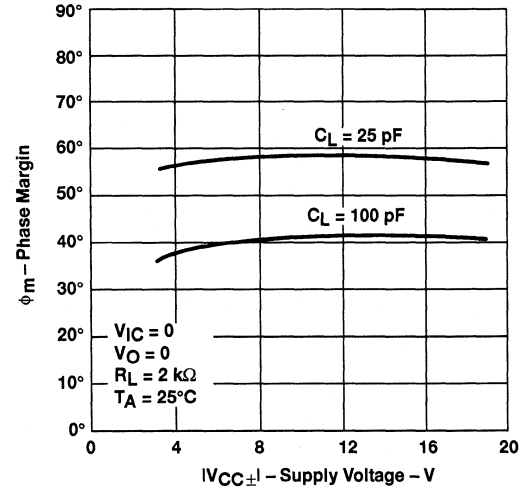


Figure 54

PHASE MARGIN
vs
LOAD CAPACITANCE

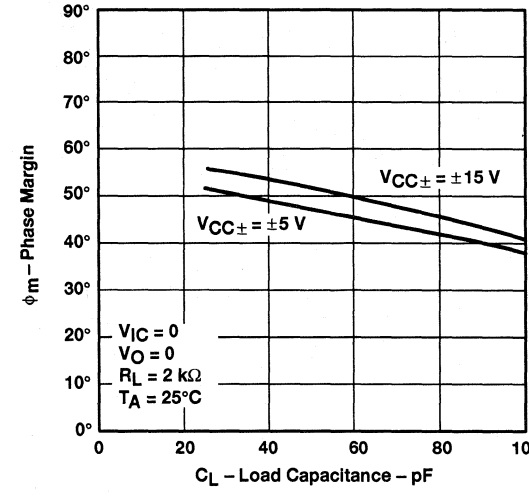


Figure 55

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

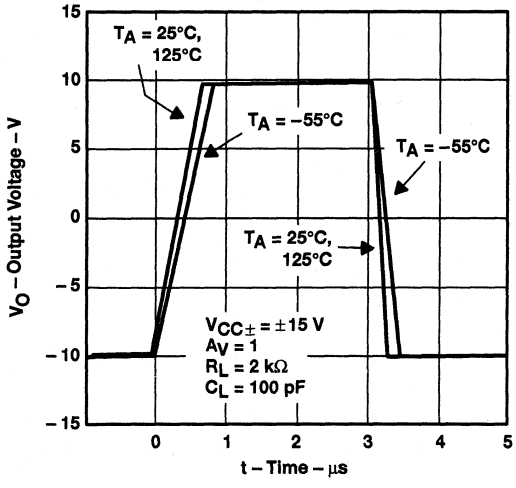


Figure 56

SMALL-SIGNAL PULSE RESPONSE

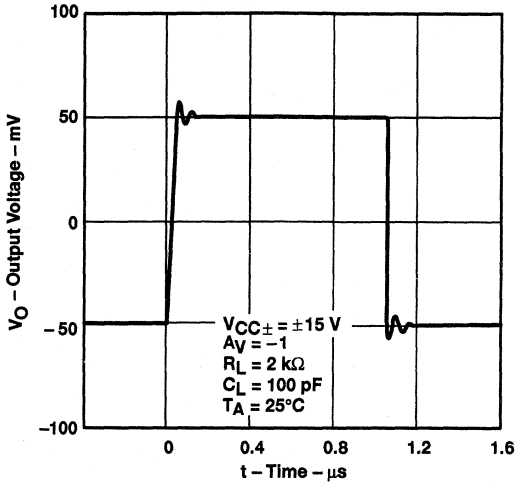


Figure 57

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

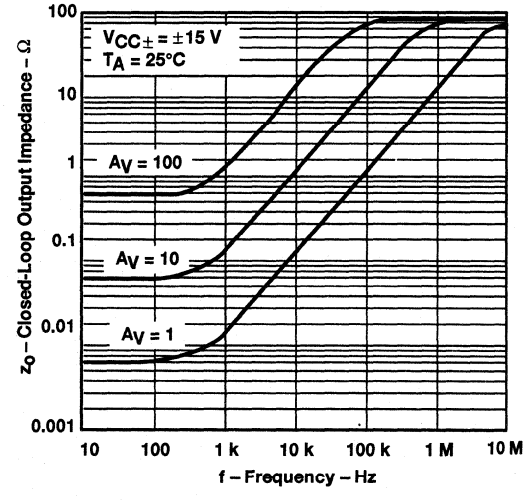


Figure 58

CROSSTALK ATTENUATION
vs
FREQUENCY

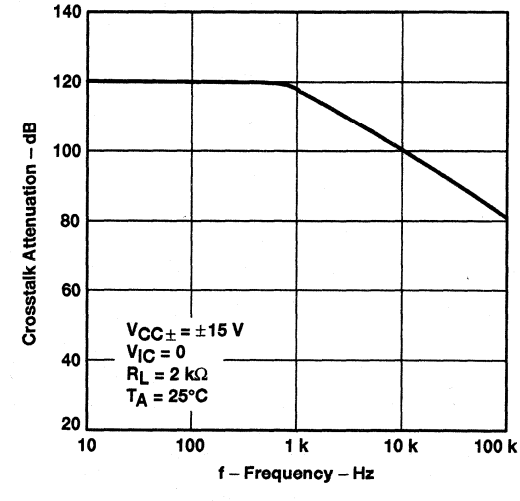


Figure 59

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

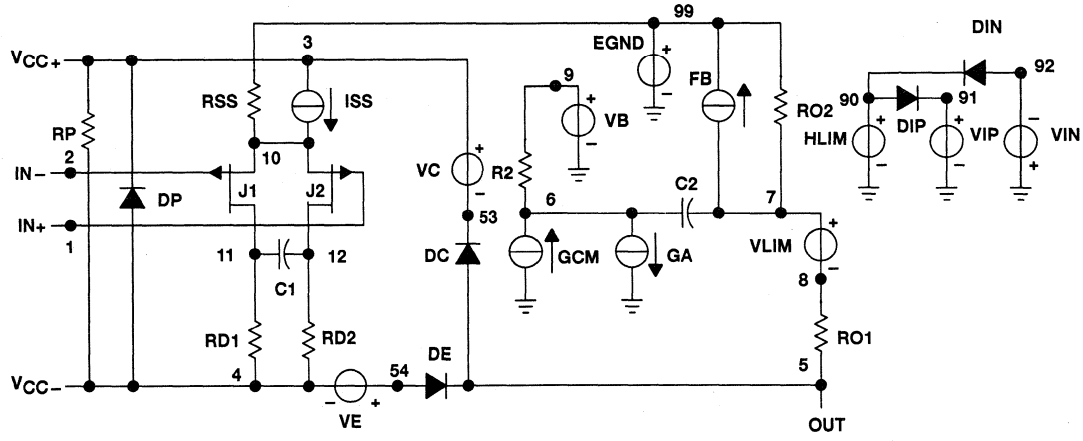
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 4) and subcircuit in Figure 60 were generated using the TLE2074 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G.R. Boyle, B.M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLE2074 1 2 3 4 5
C1      11      12      2.2E-12
C2      6       7       10.00E-12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
FB      7       99      POLY (5) VB VC VE VLP VLN 0
+ 5.607E6 –6E6 6E6 6E6 –6E6
GA      6       0       11 12 333.0E–6
GCM     0       6       10 99 7.43E–9
ISS     3       10      DC 400.0E–6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.0E3
RD1     4       11      3.003E3
RD2     4       12      3.003E3
RO1     8       5       80
RO2     7       99      80
RP      3       4       27.30E3
RSS     10      99      500.0E3
VB      9       0       DC 0
VC      3       53      DC 2.20
VE      54      4       DC 2.20
VLIM    7       8       DC 0
VLP     91      0       DC 45
VLN     0       92      DC 45
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=15.00E–12 BETA=554.5E–6
+ VTO=–.6)
.ENDS
```

Figure 60. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

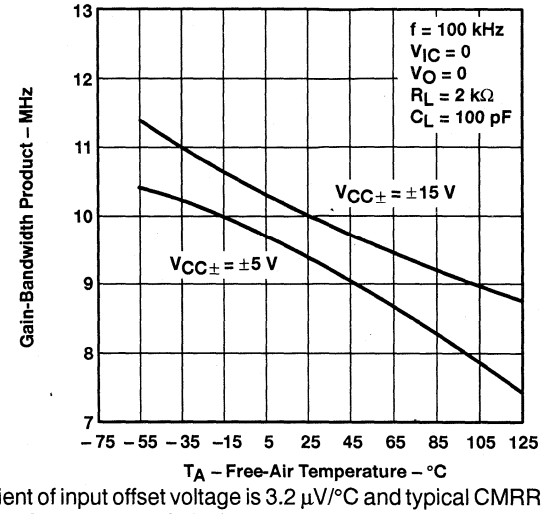
- **40-V/μs Slew Rate Typ**
- **High-Gain Bandwidth Product . . . 10 MHz**
- **±30-mA Minimum Short-Circuit Output Current**
- **Wide Supply Range . . . ±2.25 V to ±19 V**
- **Input Range Includes the Positive Supply**
- **Macromodel Included**
- **Fast Settling Time Using 10-V Step**
  400 ns to 10 mV Typ
  1.5 μs to 1 mV Typ

description

The TLE2081 and TLE2081A are high-speed, high-performance, internally-compensated, JFET-input operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2081A has a lower input offset voltage than the TLE2081. Both are pin-compatible upgrades to standard industry products.

The design features a 30-V/μs minimum slew rate, which results in a high-power bandwidth. Settling time to 0.1% of a 10-V step (1-kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8 MHz minimum. As such, the TLE2081 and TLE2081A offer significant speed and noise advantages at a low 1.7-mA typical supply current.

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE



The input current characteristics traditionally associated with JFET-input amplifiers have been maintained. Input offset voltage is graded to a 6 mV and 3 mV maximum for the TLE2081 and TLE2081A, respectively. Typically, temperature coefficient of input offset voltage is 3.2 μV/°C and typical CMRR and k_{SVR} are 98 dB and 99 dB, respectively. Device performance is relatively independent of supply voltage over the wide ±2.25-V to ±19-V range. The input common-mode voltage range extends from the positive supply down to V_{CC-} + 4 V without significant degradation to dynamic performance. Maximum peak output voltage swing is from V_{CC+} – 1 V to V_{CC-} + 1 V under light loading conditions. The output is capable of sourcing and sinking currents to at least 30 mA and can sustain shorts to either supply. Care must be taken to ensure that maximum power dissipation is not exceeded.

AVAILABLE OPTIONS

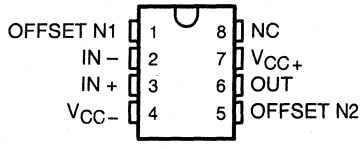
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	3 mV 6 mV	TLE2081ACD TLE2081CD	—	—	TLE2081ACP TLE2081CP	— TLE2081Y
–55°C to 125°C	3 mV 6 mV	—	TLE2081AMFK TLE2081MFK	TLE2081AMJG TLE2081MJG	—	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2081ACDR). Chip-form versions are tested at T_A = 25°C. For chip-form orders, contact your local TI sales office.

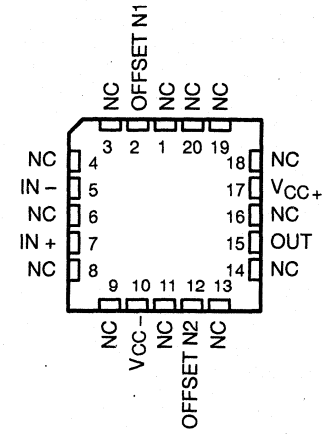
description (continued)

Both the TLE2081 and TLE2081A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C and the M-suffix over the full military temperature range of −55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

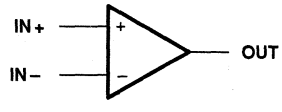


FK PACKAGE
(TOP VIEW)



NC – No internal connection

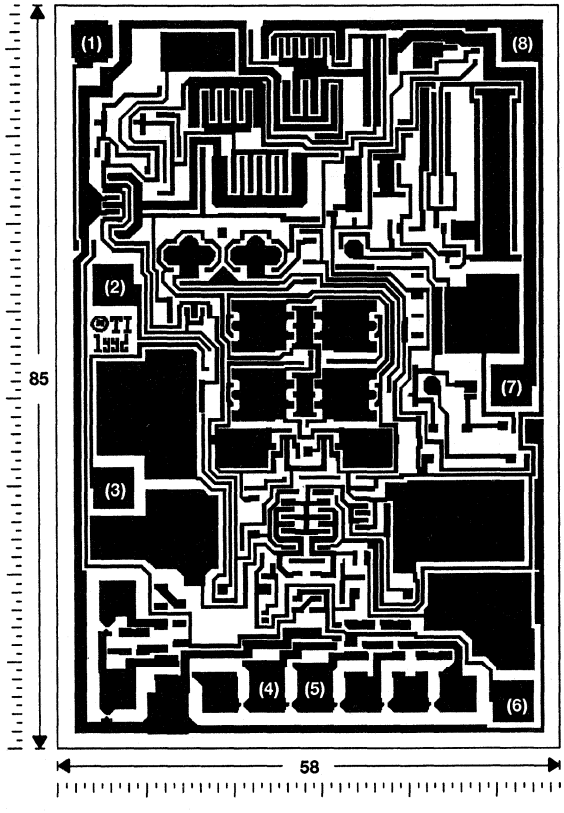
symbol

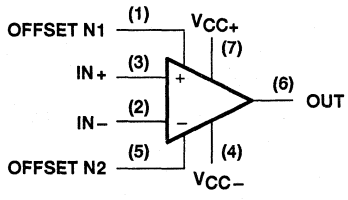


TLE2081Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2081. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

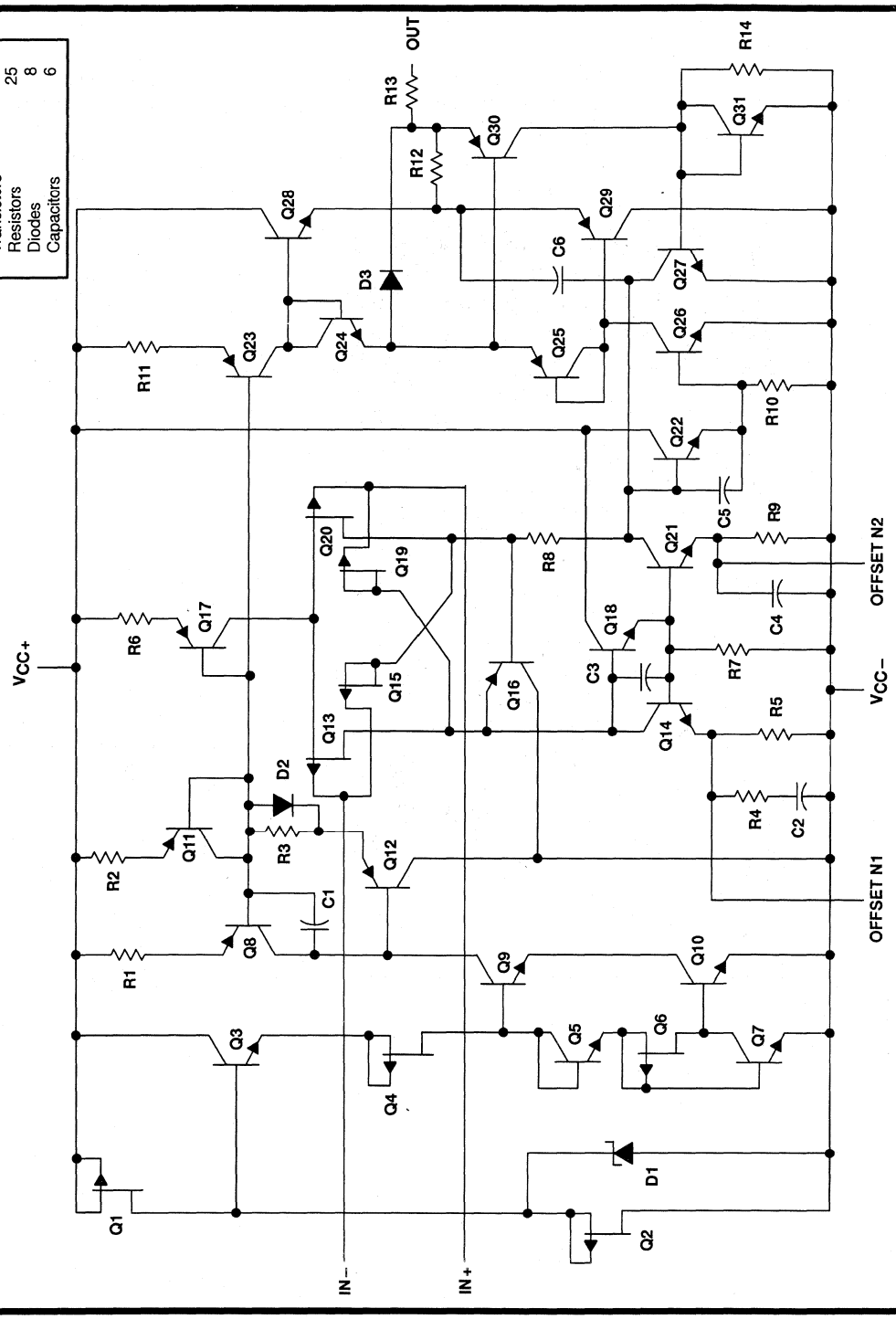
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic

ACTUAL DEVICE COMPONENT COUNT	
Transistors	33
Resistors	25
Diodes	8
Capacitors	6



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} (see Note 1) ..... −19 V
Differential input voltage range, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-}
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	344 mW	200 mW

recommended operating conditions

		C SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2.25	±19	±2.25	±19	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−0.9	5	−0.8	5	V
	$V_{CC\pm} = \pm15$ V	−10.9	15	−10.8	15	
Operating free-air temperature, T_A		0	70	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081C			TLE2081AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.34	6		0.3	3	mV
				Full range			8			5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29		3.2	29	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	nA
				Full range			1.4			1.4	
I_{IB}	Input bias current			25°C		15	175		15	175	nA
				Full range			5			5	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.9			5 to −0.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.5	−4.2		−3.5	−4.2		V
				Full range	−3.4			−3.4			
		I_O = 2 mA		25°C	−3.7	−4.1		−3.7	−4.1		
				Full range	−3.6			−3.6			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081C			TLE2081AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0,	No load	25°C	1.35	1.6	2.2	1.35	1.6	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2081C			TLE2081AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	23			23			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	23			23			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 Hz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081C			TLE2081AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.49	6		0.47	3	mV
				Full range			8			5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29		3.2	29	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	nA
				Full range			1.4			1.4	
I_{IB}	Input bias current			25°C		20	175		20	175	nA
				Full range			5			5	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.9			15 to −10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.4			−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			81			

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081C			TLE2081AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.7	2.2	1.35	1.7	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2081C			TLE2081AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		25°C	30	40		30	40		V/μs
				Full range	27			27			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	27			27			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10, f = 1 kHz, R_L = 2 kΩ, R_S = 25 Ω		25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = −1, R_L = 2 kΩ, C_L = 25 pF		25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 2		25°C		57°			57°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081M			TLE2081AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50Ω		25°C		0.34	6		0.3	3	mV
				Full range			11.2			8.2	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29*		3.2	29*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.6			3.6			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.3			3.3			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.6			−3.6			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.3			−3.3			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081M			TLE2081AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load		25°C	1.35	1.6	2.2	1.35	1.6	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2081M			TLE2081AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		25°C		35			35		V/μs
				Full range	20*			20*			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	20*			20*			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0, f = 10 kHz		25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF, R_L = 2 kΩ, See Figure 2		25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF, R_L = 2 kΩ, See Figure 2		25°C		56°			56°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081M			TLE2081AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.49	6		0.47	3	mV
				Full range			11.2			8.2	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		3.2	29*		3.2	29*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.3			13.3			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.6			−13.6			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.3			−13.3			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)(continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2081M			TLE2081AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0,	No load	25°C	1.35	1.7	2.2	1.35	1.7	2.2	mA
				Full range			2.2			2.2	
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2081M			TLE2081AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C	30	40		30	40		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8*	10		8*	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478*	637		478*	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLE2081Y MIN	TLE2081Y TYP	TLE2081Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0,	V_O = 0,	R_S = 50 Ω		0.49	6	mV
I_{IO}	Input offset current	V_{IC} = 0,	V_O = 0,	See Figure 4		6	100	pA
I_{IB}	Input bias current					20	175	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω			15 to −11	15 to 11.9		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA			13.8	14.1		V
		I_O = −2 mA			13.5	13.9		
		I_O = −20 mA			11.5	12.3		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA			−13.8	−14.2		V
		I_O = 2 mA			−13.5	−14		
		I_O = 20 mA			−11.5	−12.4		
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω		80	96		dB
			R_L = 2 kΩ		90	109		
			R_L = 10 kΩ		95	118		
r_i	Input resistance	V_{IC} = 0				10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode			7.5		pF
			Differential			2.5		
z_o	Open-loop output impedance	f = 1 MHz				80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	V_O = 0,	R_S = 50 Ω	80	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$= ±5 V to ±15 V,	V_O = 0,	R_S = 50 Ω	82	99		dB
I_{CC}	Supply current	V_O = 0,	No load		1.35	1.7	2.2	mA
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V		−30	−45		mA
			V_{ID} = −1 V		30	48		

PARAMETER MEASUREMENT INFORMATION

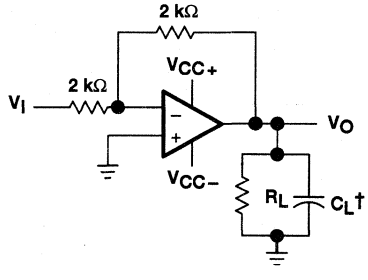


Figure 1. Slew-Rate Test Circuit

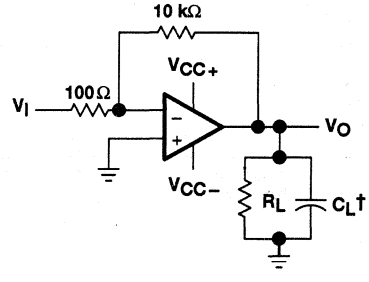


Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

† Includes fixture capacitance

PARAMETER MEASUREMENT INFORMATION

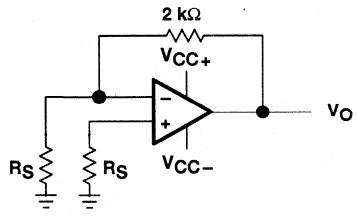


Figure 3. Noise-Voltage Test Circuit

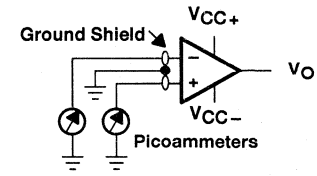


Figure 4. Input-Bias and Offset-Current Test Circuit

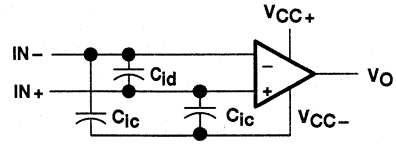


Figure 5. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TLE2081 and TLE2081A, accurate measurement of the bias becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Free-air temperature	8, 9
I_{IB}	Input bias current	vs Free-air temperature vs Supply voltage	8, 9 10
V_{ICR}	Common-mode input voltage range	vs Free-air temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13

TYPICAL CHARACTERISTICS

Table of Graphs (Continued)

			FIGURE
V_{OM+}	Maximum positive peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	14 16, 17 18
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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
V_O	Output voltage	vs Settling time	20
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Free-air temperature	21 22, 23
A_{vd}	Small-signal differential voltage amplification	vs Frequency	24, 25
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	26 27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	28 29
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	30 31 32, 33
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	34 35 36
SR	Slew rate	vs Free-air temperature vs Load resistance vs Differential input voltage	37, 38 39 40
V_n	Equivalent input noise voltage	vs Frequency	41
V_n	Input-referred noise voltage	vs Noise bandwidth Over a 10-second time interval	42 43
	Third-octave spectral noise density	vs Frequency	44
THD + N	Total harmonic distortion plus noise	vs Frequency	45, 46
B_1	Unity-gain bandwidth	vs Load capacitance	47
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	48 49
A_m	Gain margin	vs Load capacitance	50
ϕ_m	Phase margin	vs Free-air temperature vs Supply voltage vs Load capacitance	51 52 53
	Phase shift	vs Frequency	24, 25
	Large-signal pulse response, noninverting	vs Time	54
	Small-signal pulse response	vs Time	55
z_o	Output impedance	vs Frequency	56

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLE2081
INPUT OFFSET VOLTAGE

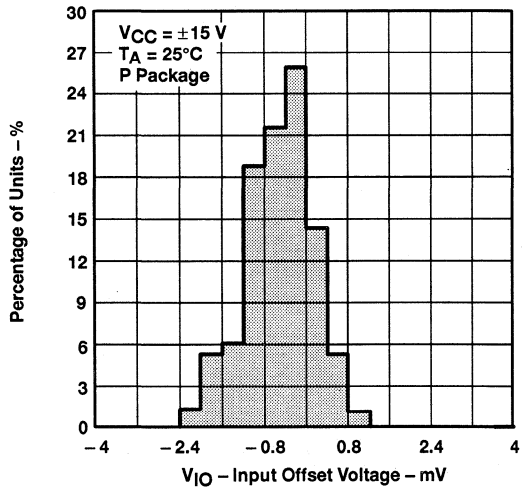


Figure 6

DISTRIBUTION OF TLE2081 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

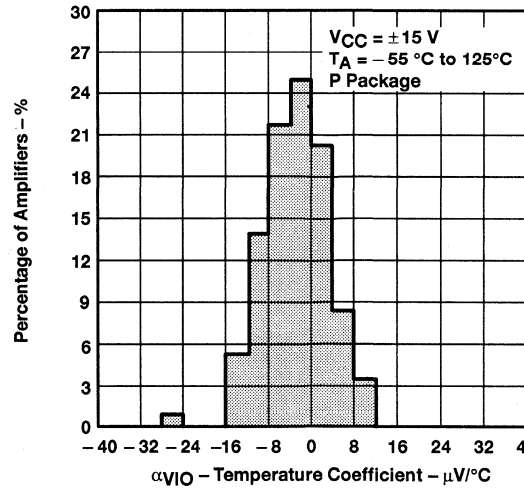


Figure 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

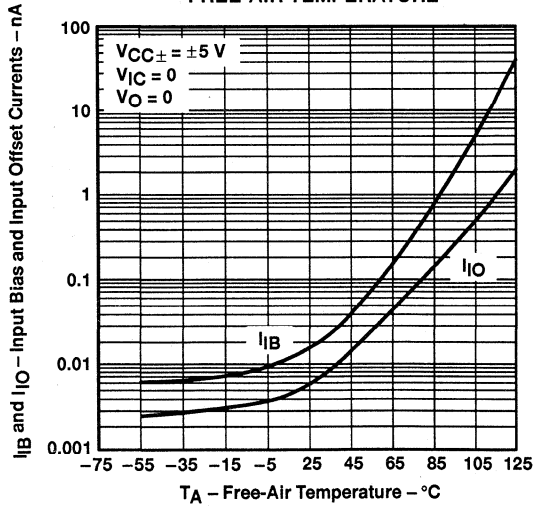


Figure 8

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

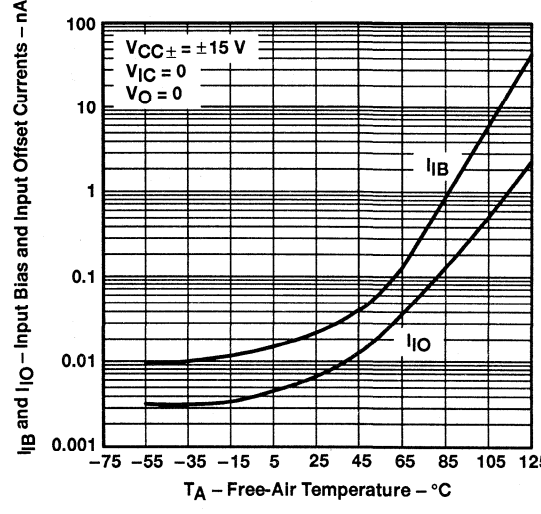


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

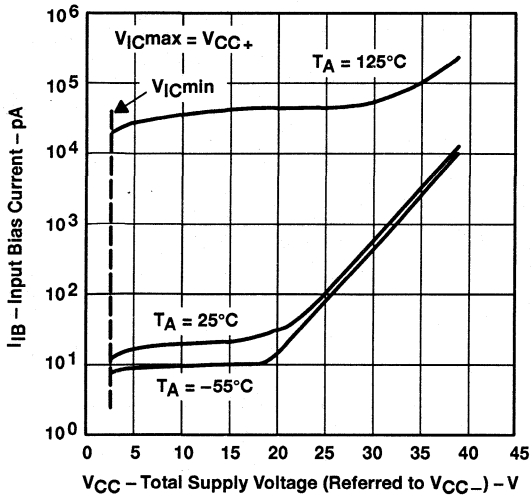


Figure 10

COMMON-MODE INPUT VOLTAGE RANGE vs TEMPERATURE

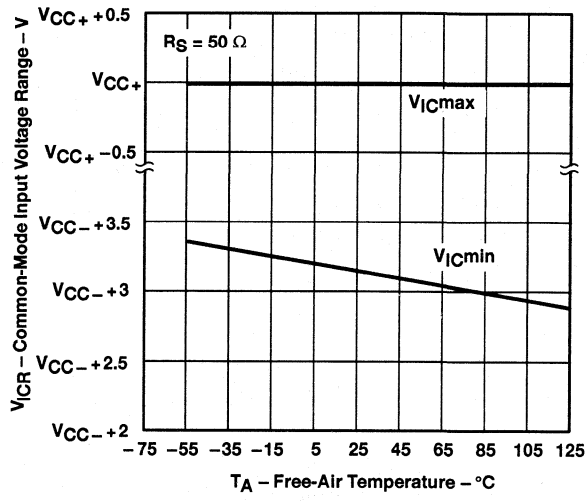


Figure 11

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

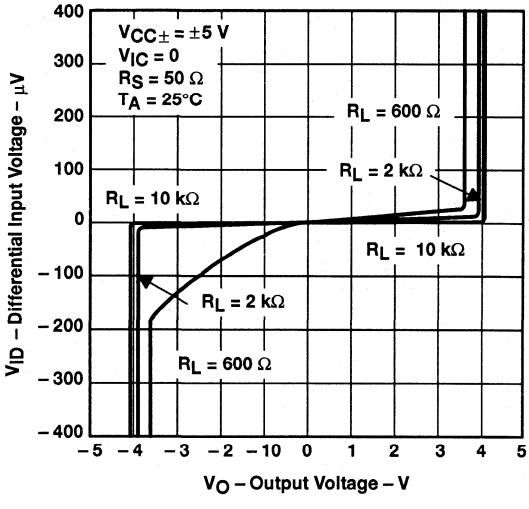


Figure 12

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

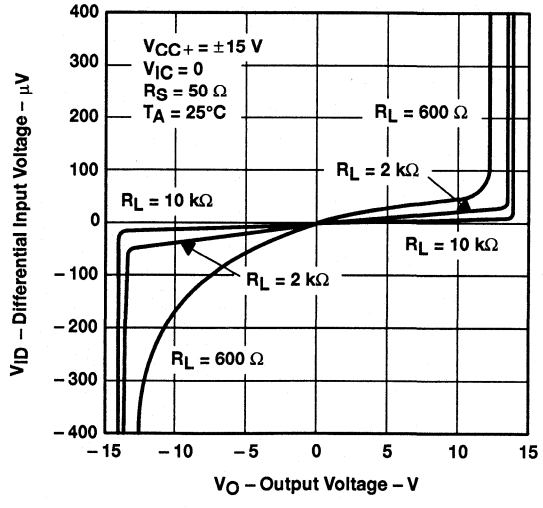


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

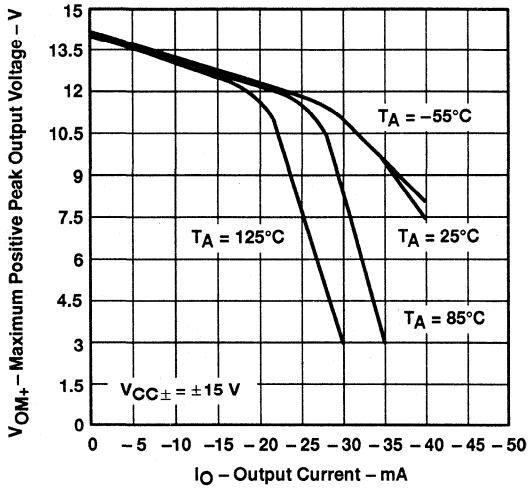


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

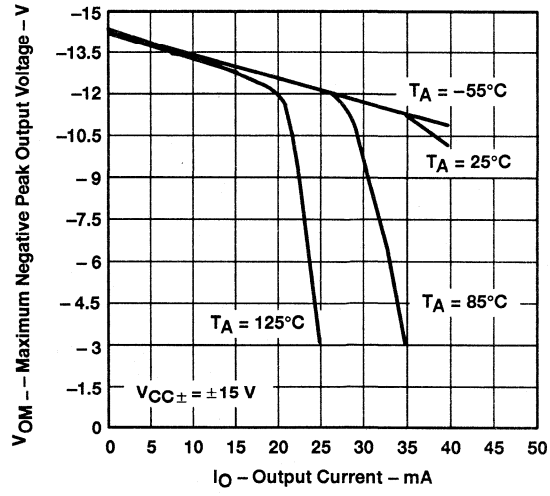


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

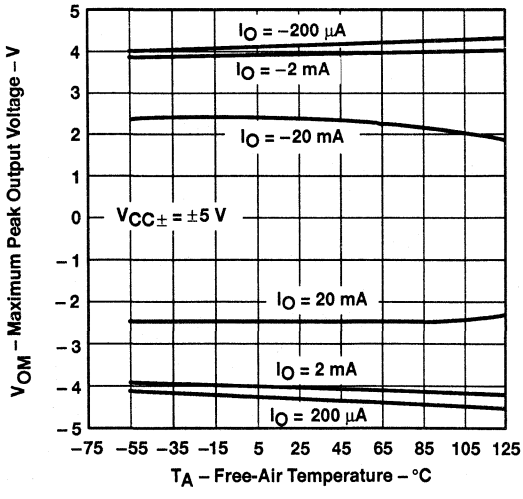


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

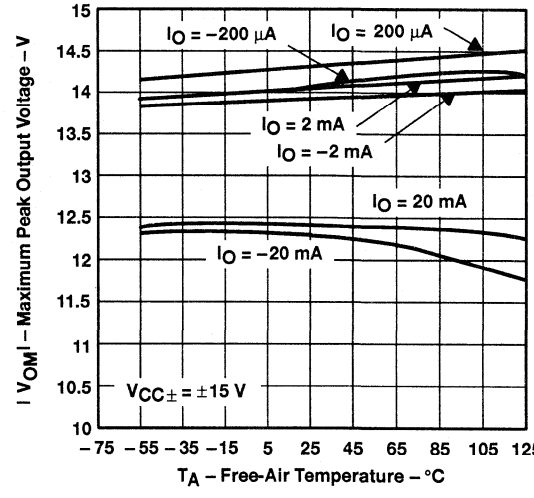


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

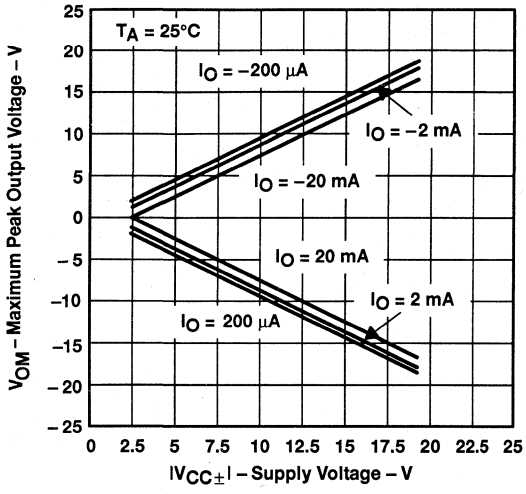


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

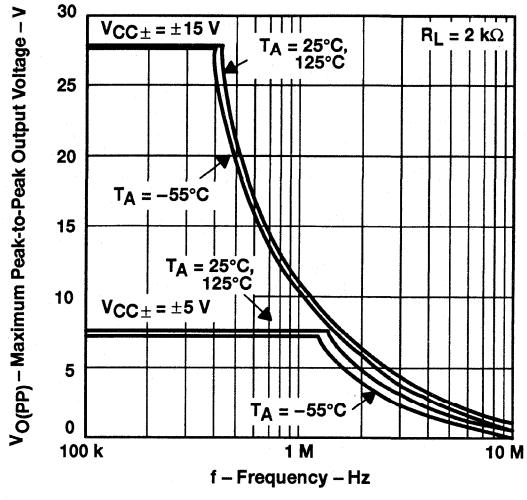


Figure 19

OUTPUT VOLTAGE
vs
SETTLING TIME

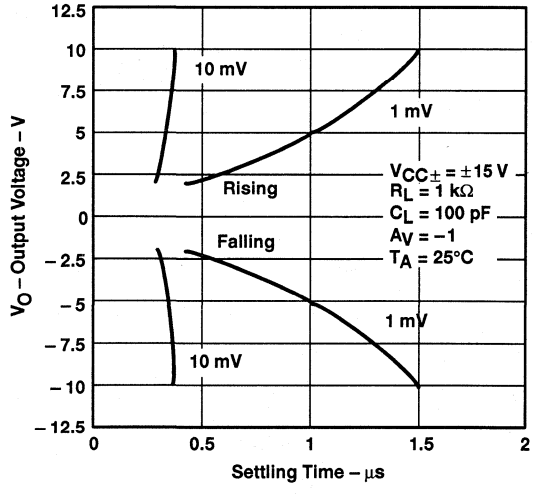


Figure 20

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

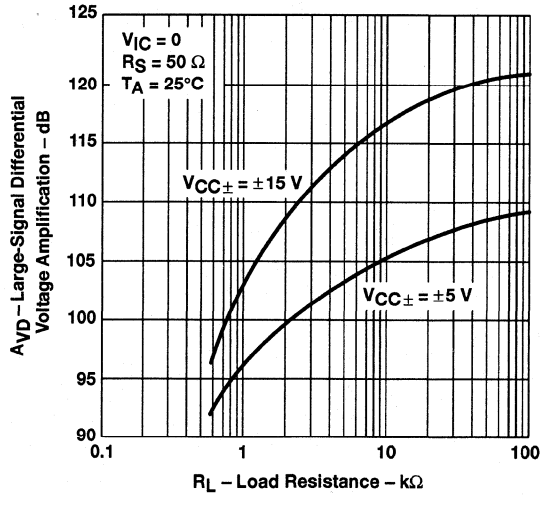


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

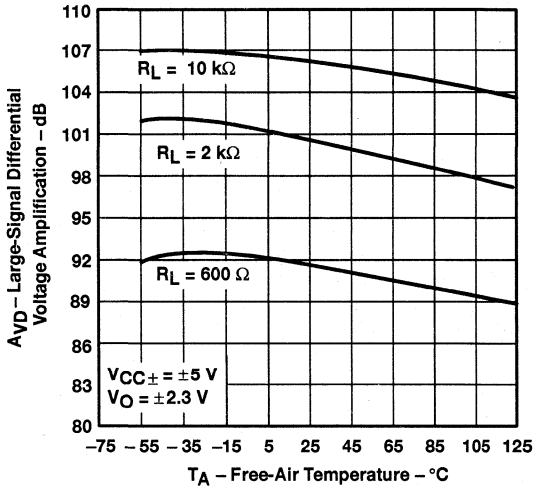


Figure 22

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

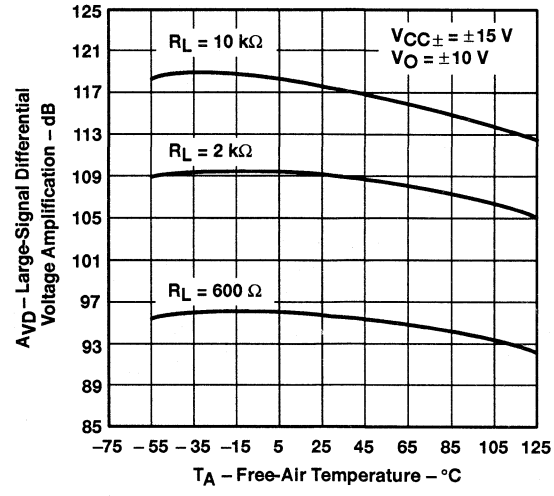


Figure 23

SMALL-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

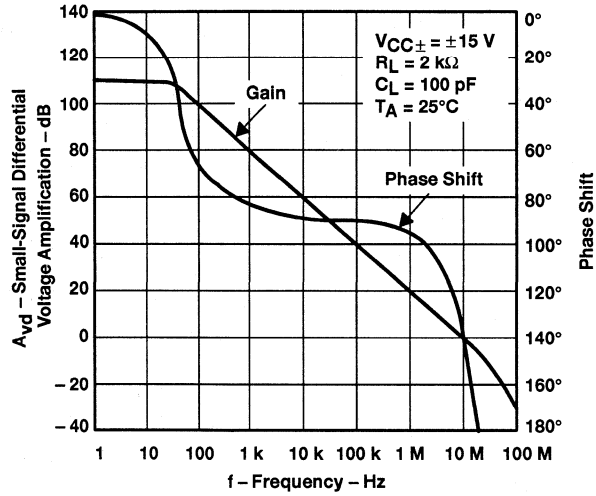


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

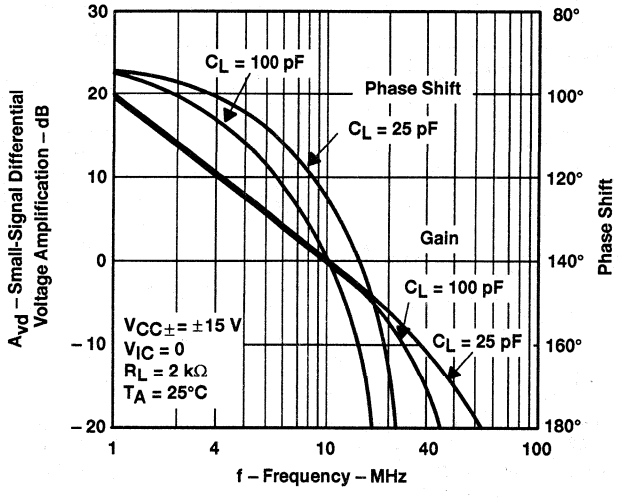


Figure 25

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

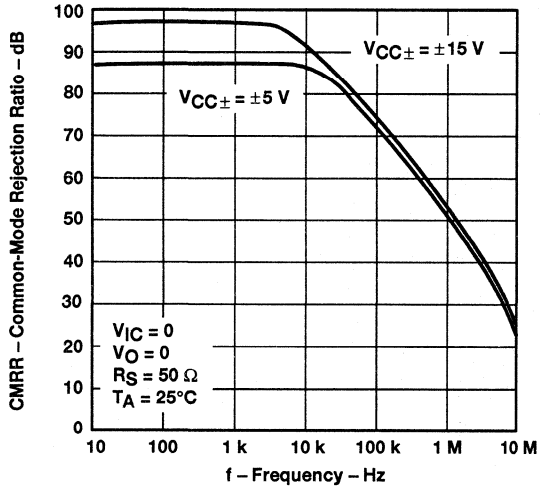


Figure 26

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

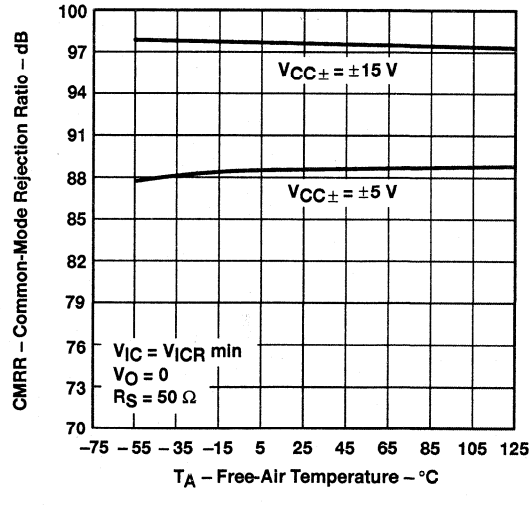


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

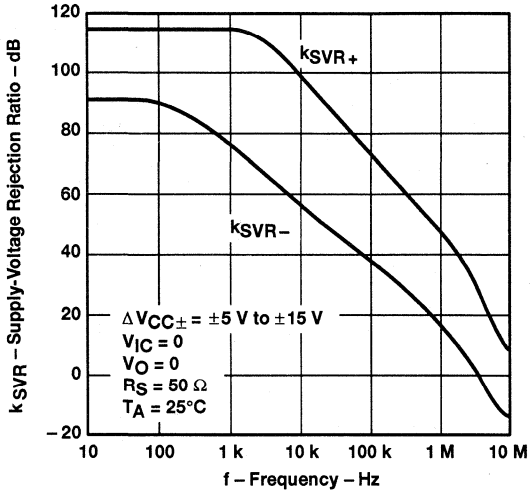


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

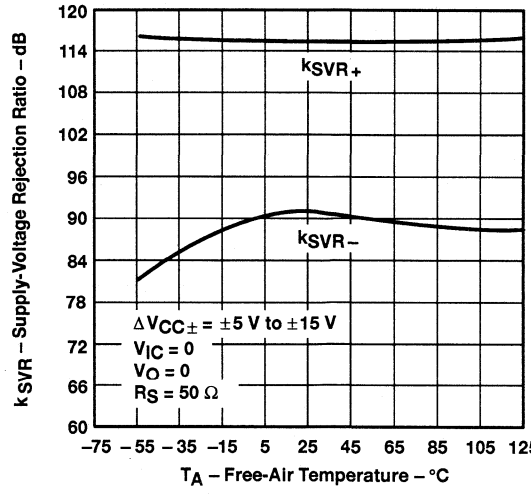


Figure 29

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

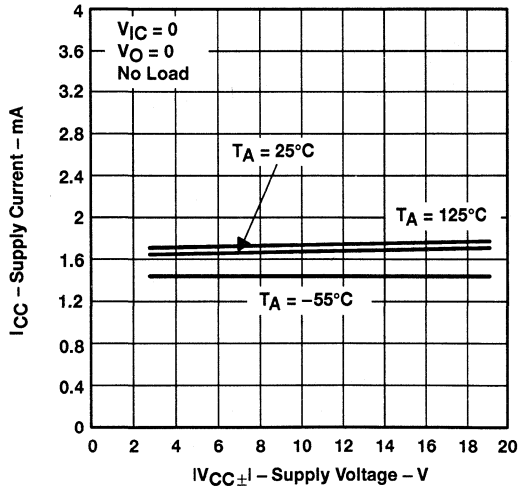


Figure 30

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

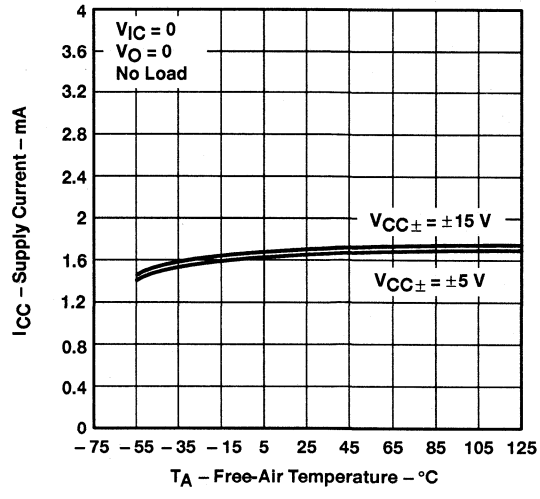


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

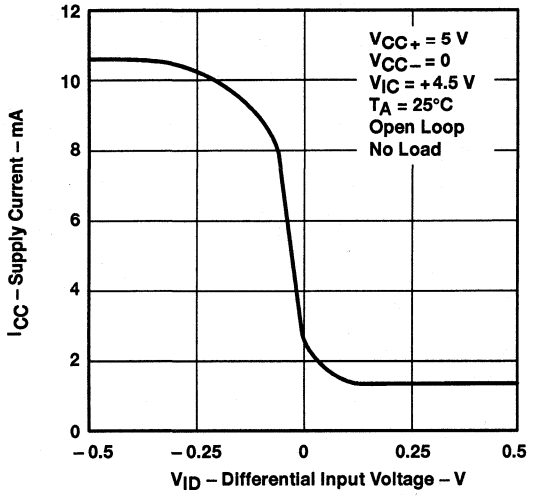


Figure 32

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

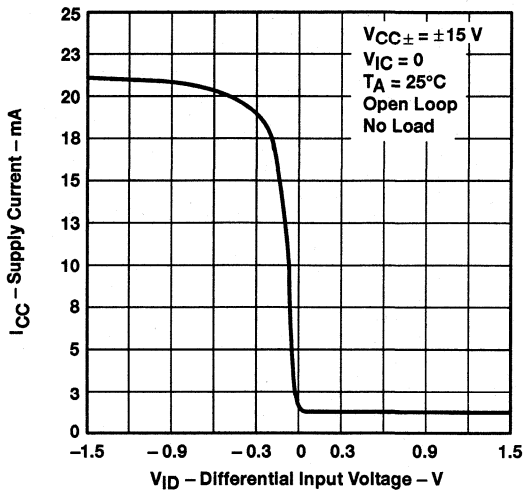


Figure 33

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

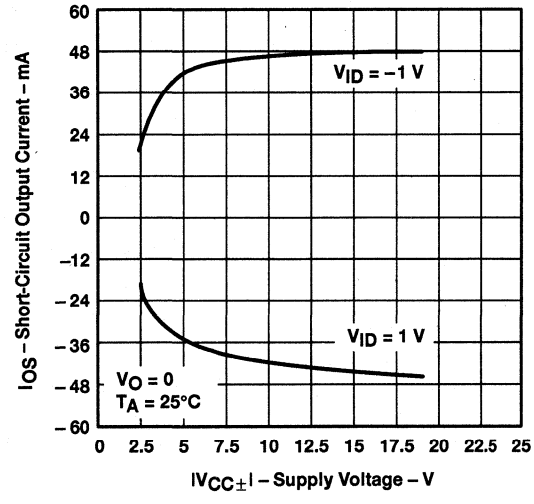


Figure 34

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

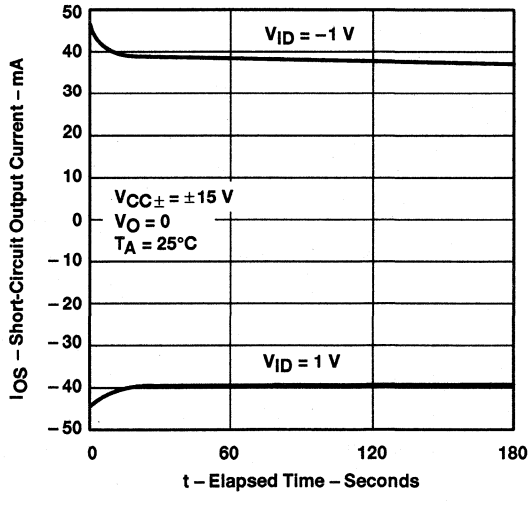


Figure 35

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

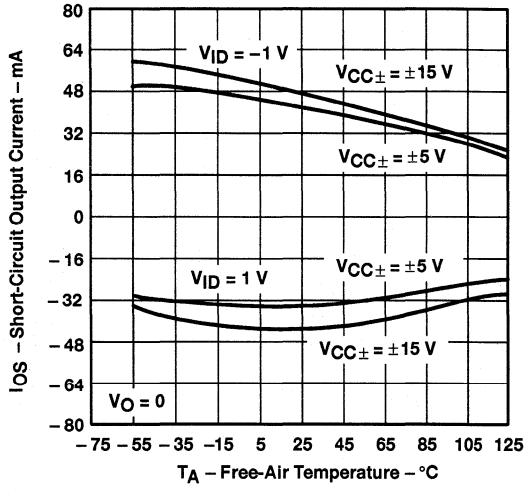


Figure 36

SLEW RATE vs FREE-AIR TEMPERATURE

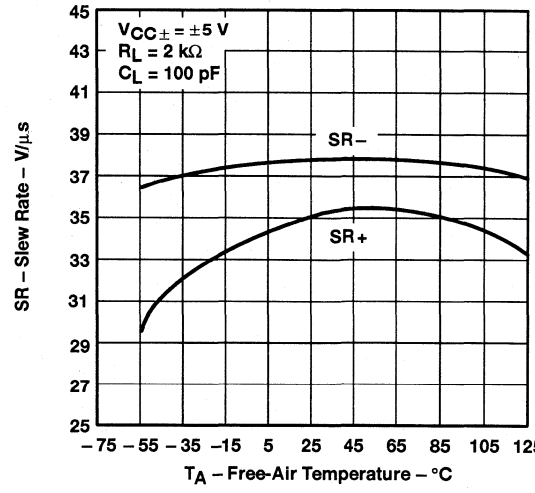


Figure 37

SLEW RATE vs FREE-AIR TEMPERATURE

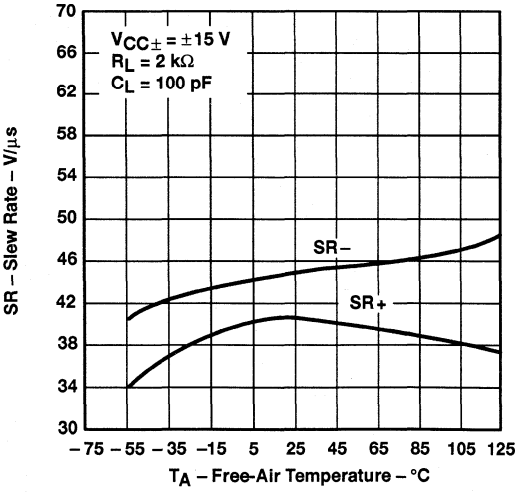


Figure 38

SLEW RATE vs LOAD RESISTANCE

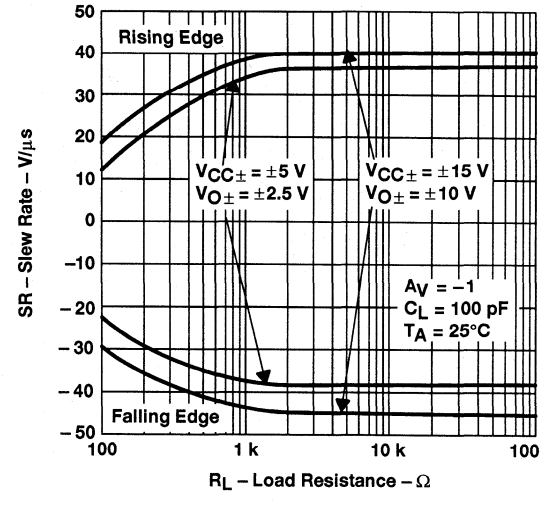


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

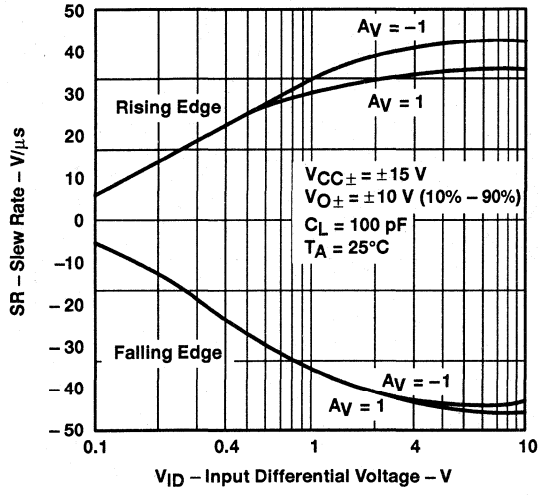


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

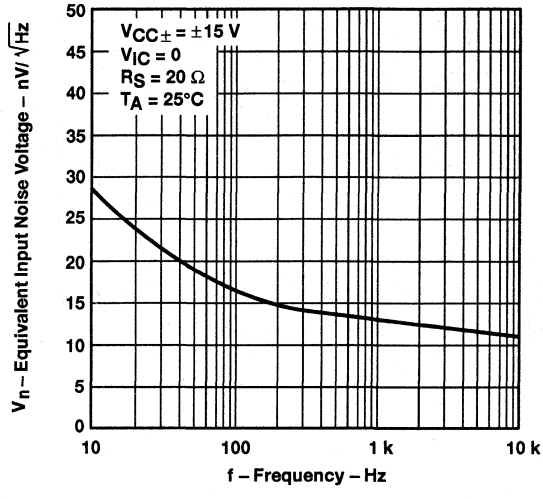


Figure 41

INPUT-REFERRED NOISE VOLTAGE vs NOISE BANDWIDTH

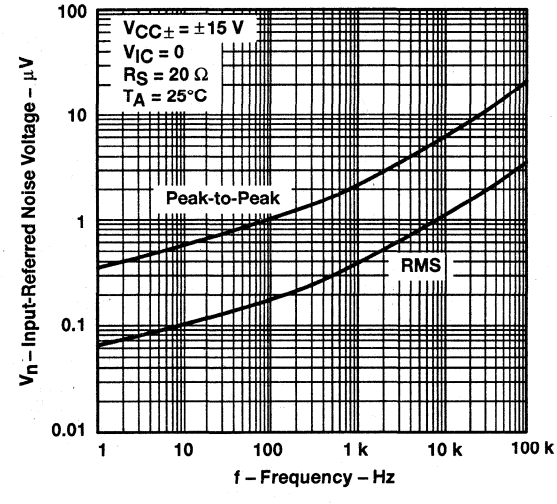


Figure 42

INPUT-REFERRED NOISE VOLTAGE OVER A 10-SECOND TIME INTERVAL

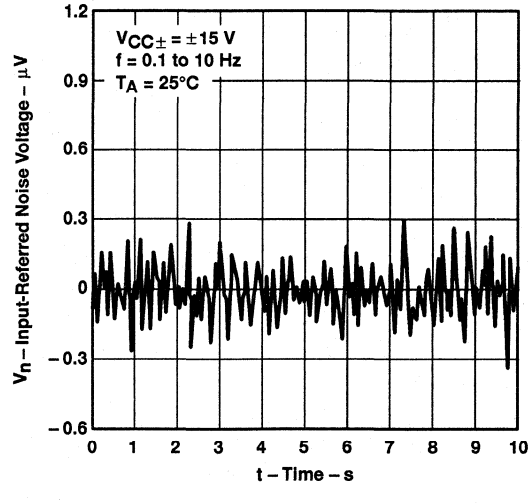


Figure 43

TYPICAL CHARACTERISTICS

THIRD-OCTAVE SPECTRAL NOISE DENSITY
vs
FREQUENCY

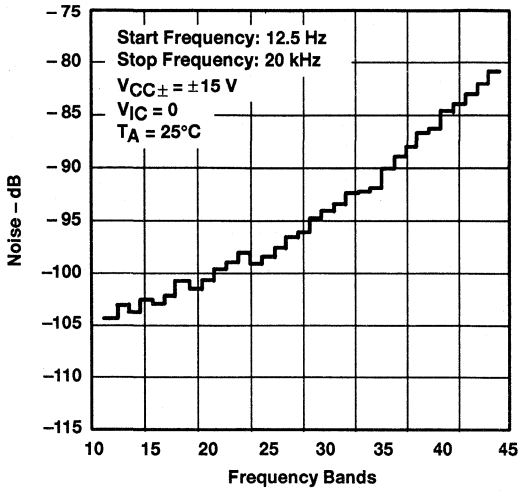


Figure 44

TOTAL HARMONIC DISTORTION PLUS
NOISE
vs
FREQUENCY

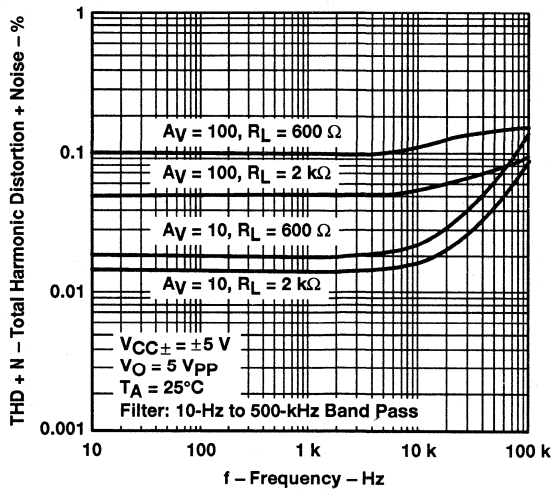


Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

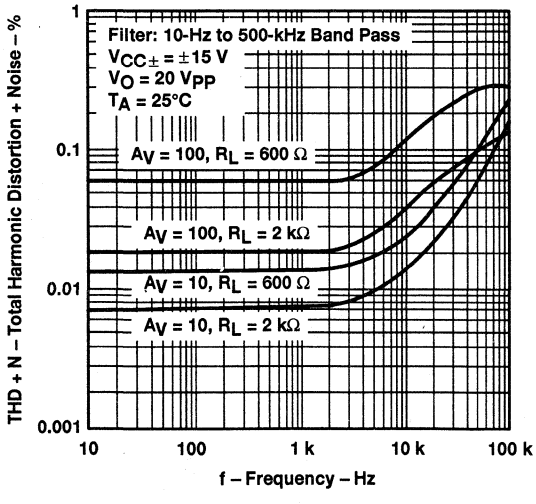


Figure 46

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

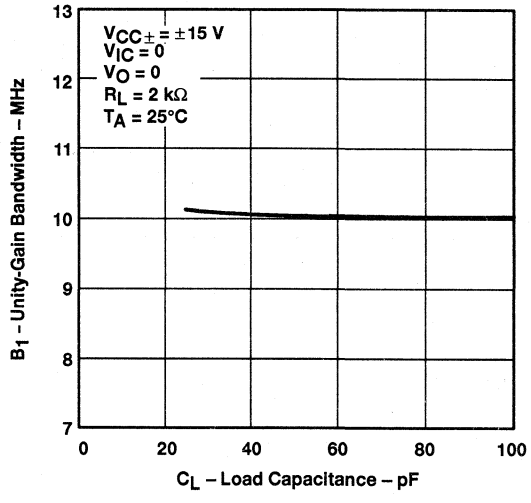


Figure 47

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

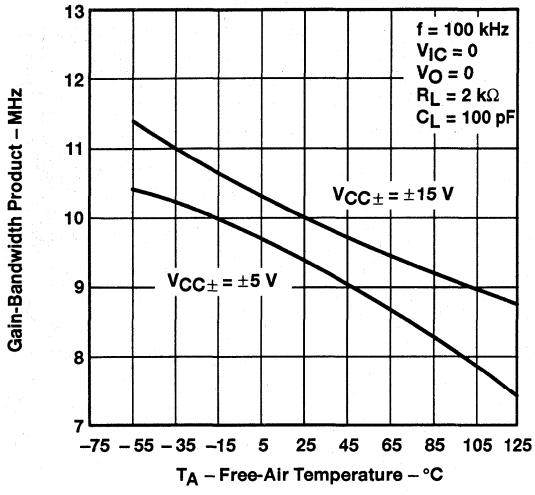


Figure 48

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

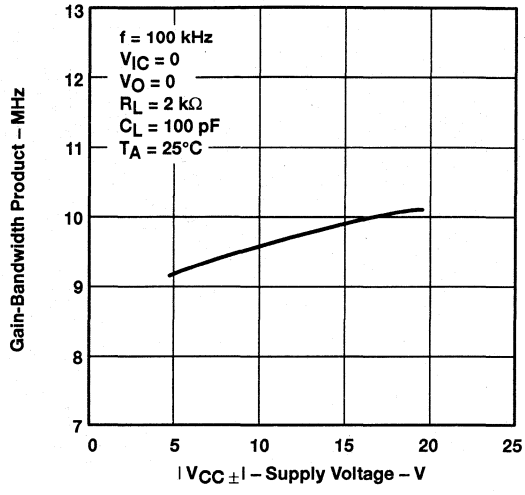


Figure 49

GAIN MARGIN vs LOAD CAPACITANCE

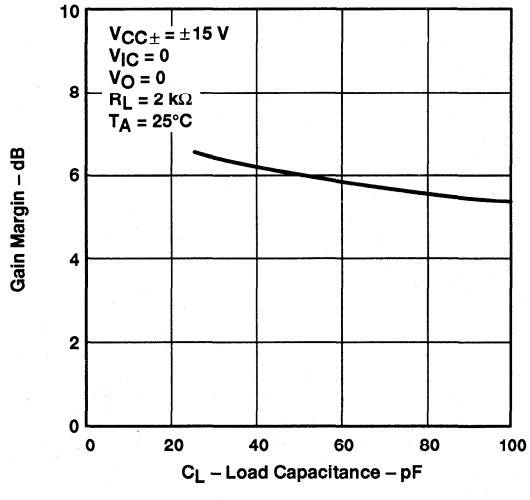


Figure 50

PHASE MARGIN vs TEMPERATURE

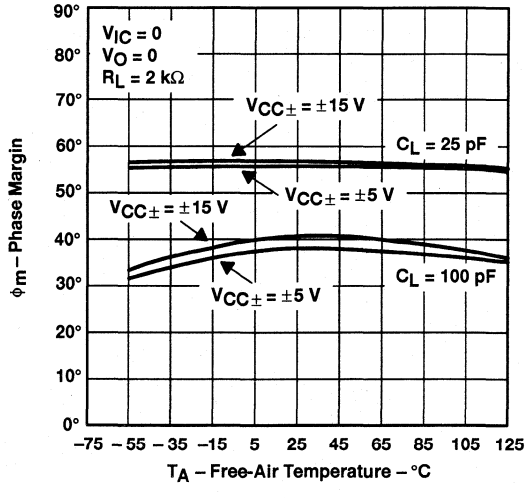


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

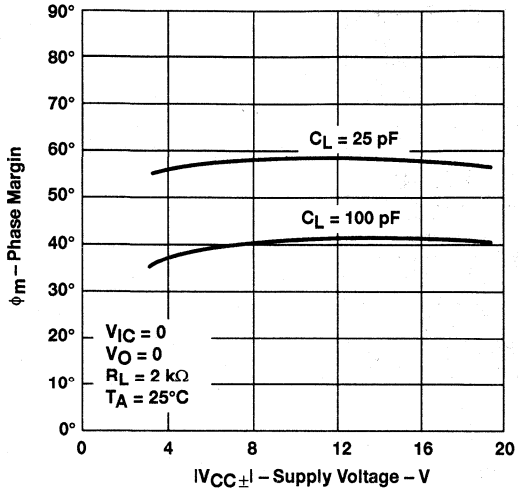


Figure 52

PHASE MARGIN
vs
LOAD CAPACITANCE

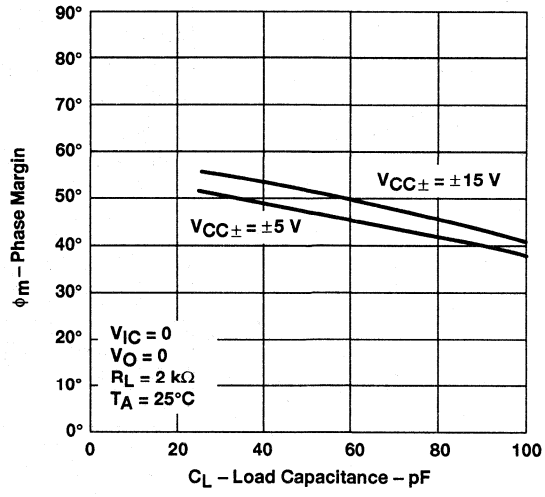


Figure 53

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

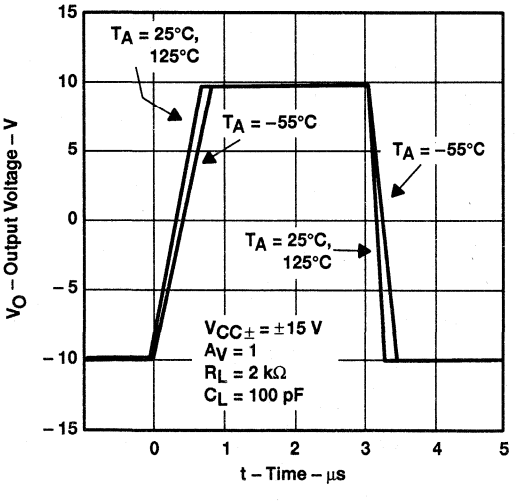


Figure 54

SMALL-SIGNAL PULSE RESPONSE

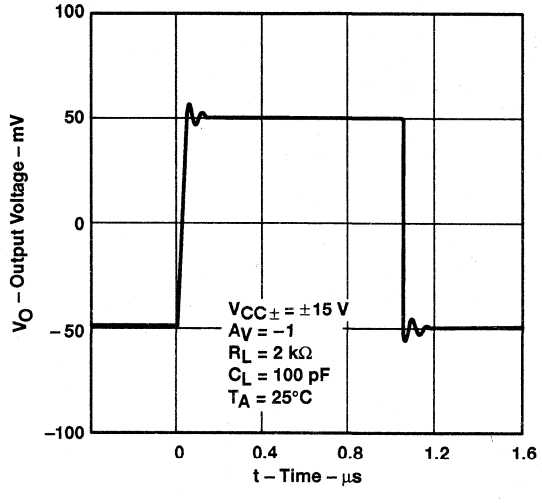


Figure 55

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

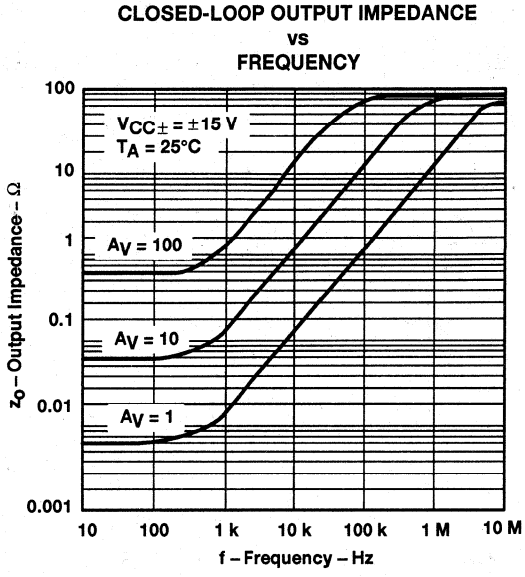


Figure 56

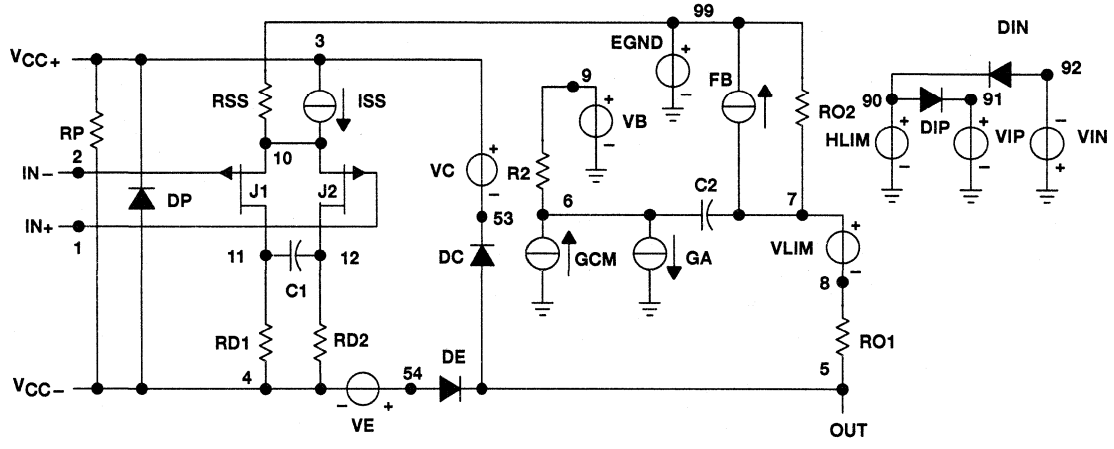
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 4) and subcircuit in Figure 58 were generated using the TLE2081 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G.R. Boyle, B.M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



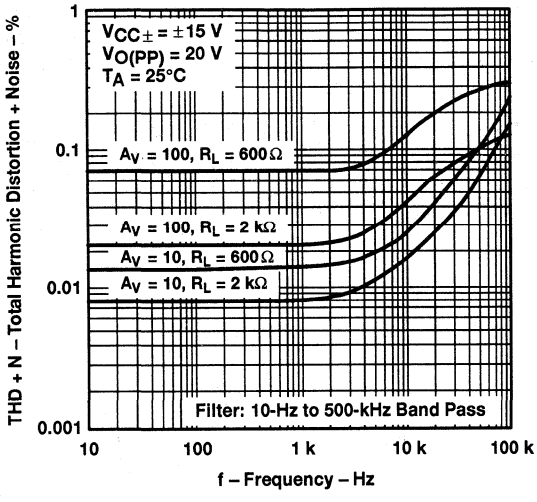

```
.SUBCKT TLE2081 1 2 3 4 5
  C1    11   12    2.2E-12
  C2    6    7     10.00E-12
  DC    5    53    DX
  DE    54   5     DX
  DLP   90   91    DX
  DLN   92   90    DX
  DP    4    3     DX
  EGND  99   0     POLY (2) (3,0) (4,0) 0 .5 .5
  FB    7    99    POLY (5) VB VC VE VLP VLN 0
+ 5.607E6 -6E6 6E6 6E6 -6E6
  GA    6    0     11 12 333.0E-6
  GCM   0    6     10 99 7.43E-9
  ISS   3    10    DC 400.0E-6
  HLIM  90   0     VLIM 1K
  J1    11   2     10 JX
  J2    12   1     10 JX
  R2    6    9     100.0E3
  RD1   4    11    3.003E3
  RD2   4    12    3.003E3
  RO1   8    5     80
  RO2   7    99    80
  RP    3    4     27.30E3
  RSS   10   99    500.0E3
  VB    9    0     DC 0
  VC    3    53    DC 2.20
  VE    54   4     DC 2.20
  VLIM  7    8     DC 0
  VLP   91   0     DC 45
  VLN   0    92    DC 45
.MODEL DX D (IS=800.0E-18)
.MODEL JX PJF (IS=15.00E-12 BETA=554.5E-6
+ VTO=-.6)
.ENDS
```

Figure 57. Boyle Macromodel and Subcircuit

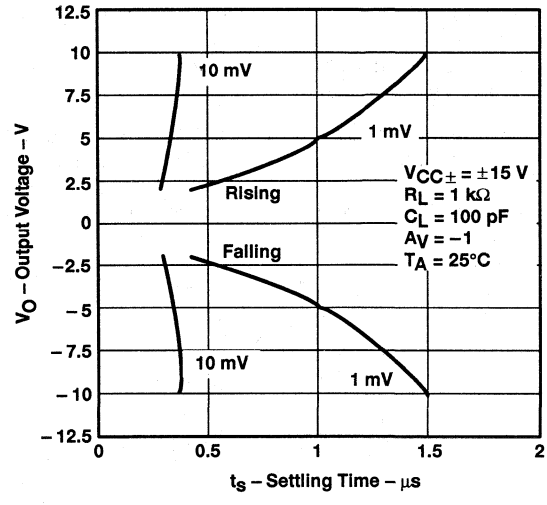
PSpice and *Parts* are registered trademarks of MicroSim Corporation.

- 40-V/μs Slew Rate Typ
- High-Gain Bandwidth Product . . . 10 MHz
- ±30-mA Minimum Short-Circuit Output Current
- Wide Supply Range . . . ±2.25 V to ±19 V
- Fast Settling Time Using 10-V Step
  400 ns to 10 mV Typ
  1.5 μs to 1 mV Typ
- Input Range Includes the Positive Supply
- Macromodel Included

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



OUTPUT VOLTAGE vs SETTLING TIME



description

The TLE2082 and TLE2082A are high-performance, high-speed, internally compensated JFET-input dual operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2082A has a lower input offset voltage than the TLE2082. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	4 mV 7 mV	TLE2082ACD TLE2082CD	—	—	TLE2082ACP TLE2082CP	—
–40°C to 85°C	4 mV 7 mV	TLE2082AID TLE2082ID	—	—	TLE2082AIP TLE2082IP	TLE2082Y
–55°C to 125°C	4 mV 7 mV	TLE2082AMD TLE2082MD	TLE2082AMFK TLE2082MFK	TLE2082AMJG TLE2082MJG	TLE2082AMP TLE2082MP	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2082ACDR). Chip-form versions are tested at T_A = 25°C. For chip-form orders, contact your local TI sales office.

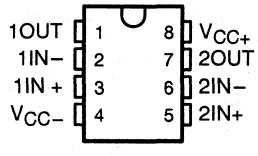
description (continued)

The design features a 28-V/μs minimum slew rate, which results in a high-power bandwidth. Settling time to 0.1% of a 10-V step (1 kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8-MHz minimum. As such, the TLE2082 and TLE2082A offer significant speed and noise advantages at a low 1.5-mA typical supply current per channel.

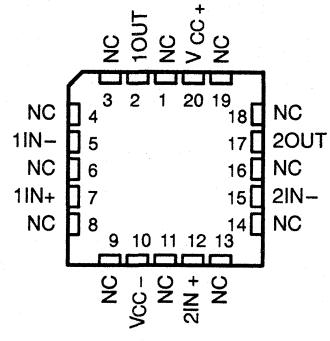
The input current characteristics traditionally associated with JFET-input amplifiers have been maintained. The input offset voltage is graded to a 7-mV and a 4-mV maximum for the TLE2082 and the TLE2082A, respectively. Typically, temperature coefficient of input offset voltage is 2.4 μV/°C and typical CMRR and k_{SVR} are 98 dB and 99 dB, respectively. Device performance is relatively independent of supply voltage over the wide ±2.25-V to ±19-V range. The input common-mode voltage range extends from the positive supply down to V_{CC-} + 4 V without significant degradation to dynamic performance. Maximum peak output voltage swing is from V_{CC+} – 1 V to V_{CC-} + 1 V under light loading conditions. The output is capable of sourcing and sinking currents to at least 30 mA and can sustain shorts to either supply. Care must be taken to ensure that maximum power dissipation is not exceeded.

Both the TLE2082 and TLE2082A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, the I-suffix devices over the –40°C to 85°C range, and the M-suffix devices over the full military temperature range of –55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

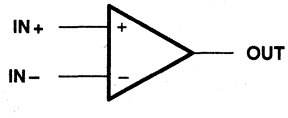


FK PACKAGE
(TOP VIEW)



NC – No internal connection

symbol

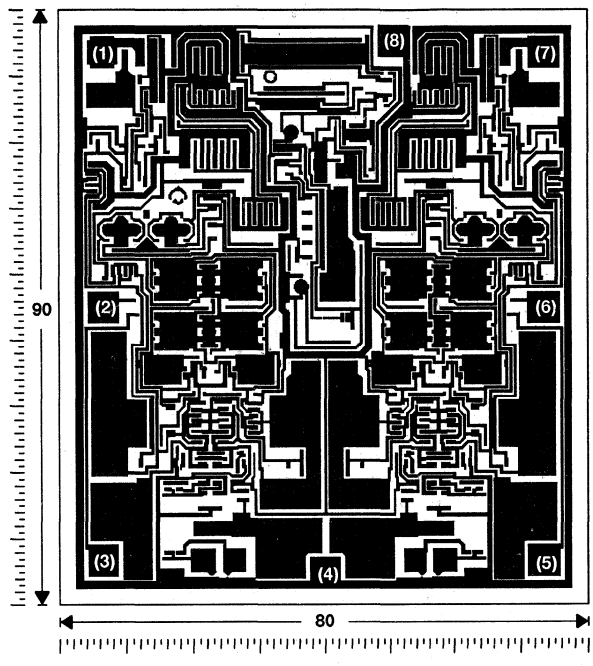


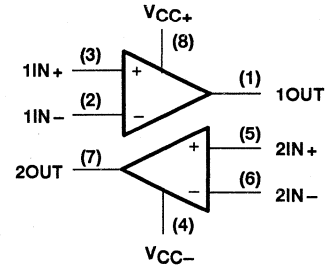
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLE2082Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2082. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

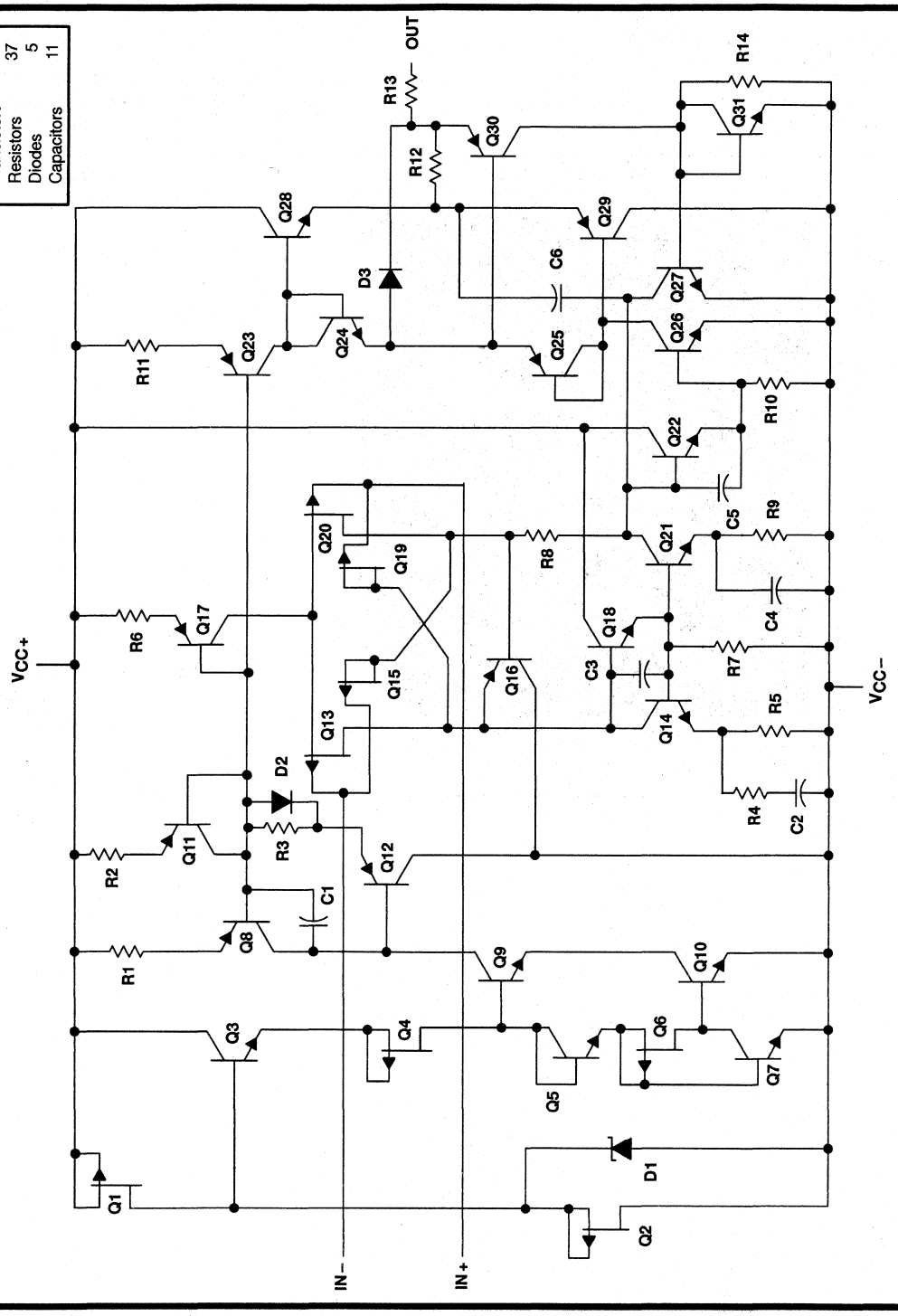
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each channel)

ACTUAL DEVICE COMPONENT COUNT	
Transistors	57
Resistors	37
Diodes	5
Capacitors	11



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} (see Note 1) ..... −19 V
Differential input voltage range, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-}
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	344 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2.25	±19	±2.25	±19	±2.25	±19	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−0.9	5	−0.8	5	−0.8	5	V
	$V_{CC\pm} = \pm15$ V	−10.9	15	−10.8	15	−10.8	15	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.9	6		0.65	4	mV
				Full range			8.1			5.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.3	25		2.3	25	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		15	175		15	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.9			5 to −0.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.7			−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.4			−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance, Common mode	V_{IC} = 0, See Figure 5		25°C		11			11		pF
	Input capacitance, Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	2.9	3.6	2.7	2.9	3.6	mA
				Full range			3.6			3.6	

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	7		0.7	4	mV
				Full range			8.1			5.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25		2.4	25	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.9			15 to −10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.4			−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance, Common mode	V_{IC} = 0, See Figure 5		25°C		7.5			7.5		pF
	Input capacitance, Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	81			81			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	3.1	3.6	2.7	3.1	3.6	mA
				Full range			3.6			3.6	

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082C			TLE2082AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	28	40		28	40		V/μs
				Full range	25			25			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	25			25			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.9	7		0.65	4	mV
					Full range			8.5			5.5	
α_{VIO}	Temperature coefficient of input offset voltage				Full range		2.4	25		2.4	25	µV/°C
I_{IO}	Input offset current		V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
					Full range			5			5	nA
I_{IB}	Input bias current				25°C		15	175		15	175	pA
					Full range			10			10	nA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
					Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing		I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
					Full range	3.7			3.7			
			I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
					Full range	3.4			3.4			
			I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
					Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
					Full range	−3.7			−3.7			
			I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
					Full range	−3.4			−3.4			
			I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
					Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
					Full range	79			79			
				R_L = 2 kΩ	25°C	90	100		90	100		
					Full range	89			89			
				R_L = 10 kΩ	25°C	95	106		95	106		
					Full range	94			94			
r_i	Input resistance		V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5		25°C		11			11		pF
		Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
					Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
					Full range	80			80			
I_{CC}	Supply current (both channels)		V_O = 0, No load		25°C	2.7	2.9	3.6	2.7	2.9	3.6	mA
					Full range			3.6			3.6	

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Crosstalk attenuation		V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	20			20			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	7		0.7	4	mV
				Full range			8.5			5.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		Full range		2.4	25		2.4	25	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			5			5	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			10			10	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.7			−13.7			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.4			−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.5			−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5	25°C		7.5			7.5		pF
		Differential		25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	3.1	3.6	2.7	3.1	3.6	mA
				Full range			3.6			3.6	

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082I			TLE2082AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	28	40		28	40		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.9	7		0.65	4	mV
					Full range			9.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage				Full range		2.3	25*		2.3	25*	µV/°C
I_{IO}	Input offset current		V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100		5	100	pA
					Full range			20			20	nA
I_{IB}	Input bias current				25°C		15	175		15	175	pA
					Full range			60			60	nA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
					Full range	5 to −0.8			5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing		I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
					Full range	3.6			3.6			
			I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
					Full range	3.3			3.3			
			I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
					Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
					Full range	−3.6			−3.6			
			I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
					Full range	−3.3			−3.3			
			I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
					Full range	−1.4			−1.4			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
					Full range	78			78			
				R_L = 2 kΩ	25°C	90	100		90	100		
					Full range	88			88			
				R_L = 10 kΩ	25°C	95	106		95	106		
					Full range	93			93			
r_i	Input resistance		V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5		25°C		11			11		pF
		Differential			25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
					Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
					Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (both channels)	V_O = 0,	No load	25°C	2.7	2.9	3.6	2.7	2.9	3.6	mA
				Full range			3.6			3.6	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	18*			18*			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	18*			18*			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	7		0.7	4	mV
				Full range			9.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		Full range		2.4	25*		2.4	25*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100		6	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		20	175		20	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		15 to −11	15 to −11.9		V
				Full range	15 to −10.8			15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = −2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.3			13.3			
		I_O = −20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−13.8	−14.2		−13.8	−14.2		V
				Full range	−13.6			−13.6			
		I_O = 2 mA		25°C	−13.5	−14		−13.5	−14		
				Full range	−13.3			−13.3			
		I_O = 20 mA		25°C	−11.5	−12.4		−11.5	−12.4		
				Full range	−11.4			−11.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance		V_{IC} = 0	25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	Common mode	V_{IC} = 0, See Figure 5	25°C		7.5			7.5		pF
		Differential		25°C		2.5			2.5		
z_o	Open-loop output impedance		f = 1 MHz	25°C		80			80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	82	99		82	99		dB
				Full range	80			80			

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current (both channels)	V_O = 0,	No load	25°C	2.7	3.1	3.6	2.7	3.1	3.6	mA
				Full range			3.6			3.6	
	Crosstalk attenuation	V_{IC} = 0,	R_L = 2 kΩ	25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		−30	−45		mA
			V_{ID} = −1 V		30	48		30	48		

† Full range is −55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

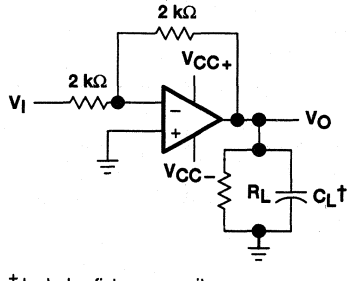
PARAMETER		TEST CONDITIONS		T_A†	TLE2082M			TLE2082AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	28	40		28	40		V/μs
				Full range	20			20			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8*	10		8*	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478*	637		478*	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

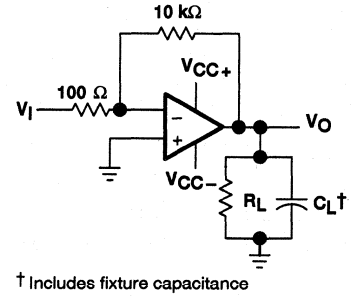
PARAMETER			TEST CONDITIONS			TLE2082Y MIN	TLE2082Y TYP	TLE2082Y MAX	UNIT
V_{IO}	Input offset voltage		V_{IC} = 0,	V_O = 0,	R_S = 50 Ω		1.1	6	mV
I_{IO}	Input offset current		V_{IC} = 0,	V_O = 0,	See Figure 4		6	100	pA
I_{IB}	Input bias current						20	175	pA
V_{ICR}	Common-mode input voltage range		R_S = 50 Ω			15 to −11	15 to 11.9		V
V_{OM+}	Maximum positive peak output voltage swing		I_O = −200 µA			13.8	14.1		V
			I_O = −2 mA			13.5	13.9		
			I_O = −20 mA			11.5	12.3		
V_{OM-}	Maximum negative peak output voltage swing		I_O = 200 µA			−13.8	−14.2		V
			I_O = 2 mA			−13.5	−14		
			I_O = 20 mA			−11.5	−12.4		
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V	R_L = 600 Ω		80	96		dB
				R_L = 2 kΩ		90	109		
				R_L = 10 kΩ		95	118		
r_i	Input resistance		V_{IC} = 0				10^{12}		Ω
c_i	Input capacitance	Common mode	V_O = 0,	See Figure 5			7.5		pF
		Differential					2.5		
z_o	Open-loop output impedance		f = 1 MHz				80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min,	V_O = 0,	R_S = 50 Ω	80	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	V_O = 0,		82	99		dB
I_{CC}	Supply current (both channels)		V_O = 0,	No load			2.7	3.1	3.6	mA
I_{OS}	Short-circuit output current		V_O = 0	V_{ID} = 1 V		−30	−45		mA
				V_{ID} = −1 V		30	48		

PARAMETER MEASUREMENT INFORMATION



† Includes fixture capacitance

Figure 1. Slew-Rate Test Circuit



† Includes fixture capacitance

Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

PARAMETER MEASUREMENT INFORMATION

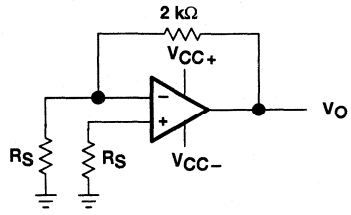


Figure 3. Noise-Voltage Test Circuit

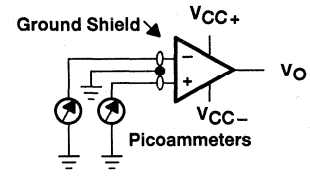


Figure 4. Input-Bias and Offset-Current Test Circuit

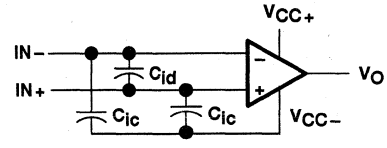


Figure 5. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2082 and TLE2082A, accurate measurement of the bias becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket, and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient	Distribution	7
I_{IO}	Input offset current	vs Free-air temperature	8, 9
I_{IB}	Input bias current	vs Free-air temperature vs Total supply voltage	8, 9 10
V_{ICR}	Common-mode input voltage range	vs Free-air temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13

TYPICAL CHARACTERISTICS

Table of Graphs (Continued)

			FIGURE
V_{OM+}	Maximum positive peak output voltage	vs Output current	14
V_{OM-}	Maximum negative peak output voltage	vs Output current	15
$\lvert V_{OM} \rvert$	Maximum peak output voltage	vs Free-air temperature vs Supply voltage	16, 17 18
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
V_O	Output voltage	vs Settling time	20
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Free-air temperature	21 22, 23
A_{VD}	Small-signal differential voltage amplification	vs Frequency	24, 25
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	26 27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	28 29
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	30 31 32, 33
I_{OS}	Short-circuit output current	vs Supply voltage vs Elapsed time vs Free-air temperature	34 35 36
SR	Slew rate	vs Free-air temperature vs Load resistance vs Differential input voltage	37, 38 39 40
V_n	Equivalent input noise voltage	vs Frequency	41
V_n	Input-referred noise voltage	vs Noise bandwidth Over a 10-second time interval	42 43
	Third-octave spectral noise density	vs Frequency bands	44
THD + N	Total harmonic distortion plus noise	vs Frequency	45, 46
B_1	Unity-gain bandwidth	vs Load capacitance	47
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	48 49
	Gain margin	vs Load capacitance	50
ϕ_m	Phase margin	vs Free-air temperature vs Supply voltage vs Load capacitance	51 52 53
	Phase shift	vs Frequency	24, 25
	Large-signal pulse response, noninverting	vs Time	54
	Small-signal pulse response	vs Time	55
z_o	Closed-loop output impedance	vs Frequency	56
	Crosstalk attenuation	vs Frequency	57

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLE2082 INPUT OFFSET VOLTAGE

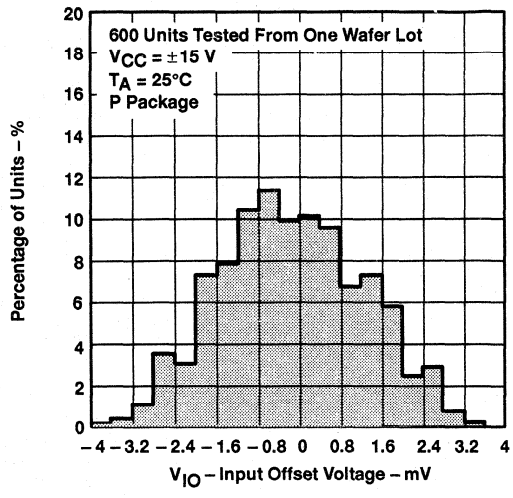


Figure 6

DISTRIBUTION OF TLE2082 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

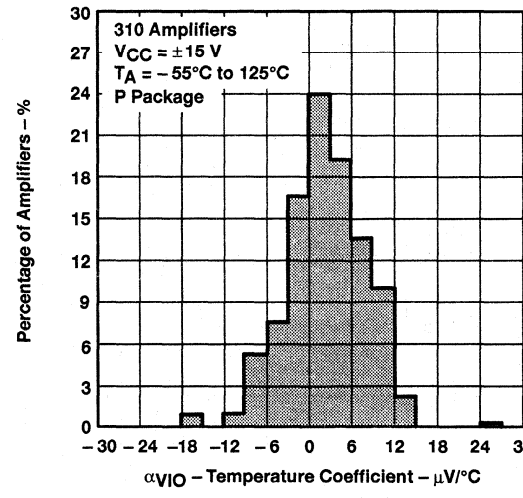


Figure 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

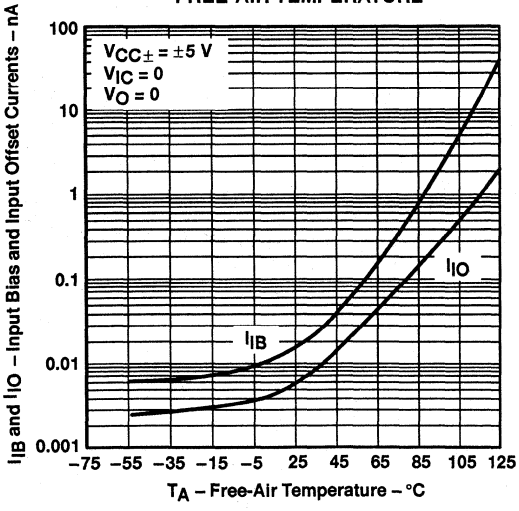


Figure 8

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

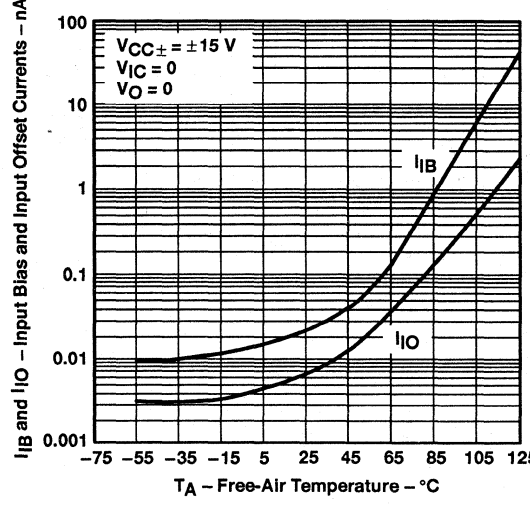


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

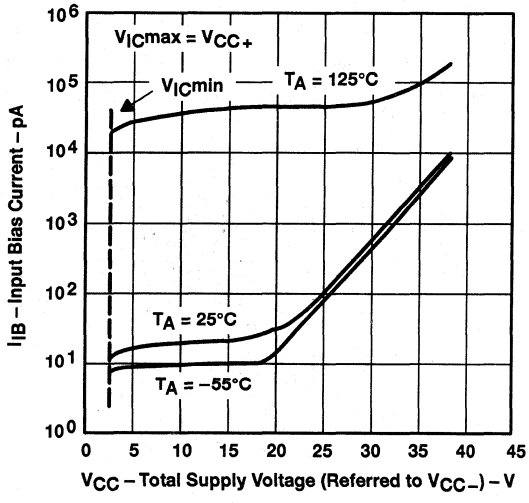


Figure 10

COMMON-MODE INPUT VOLTAGE RANGE vs FREE-AIR TEMPERATURE

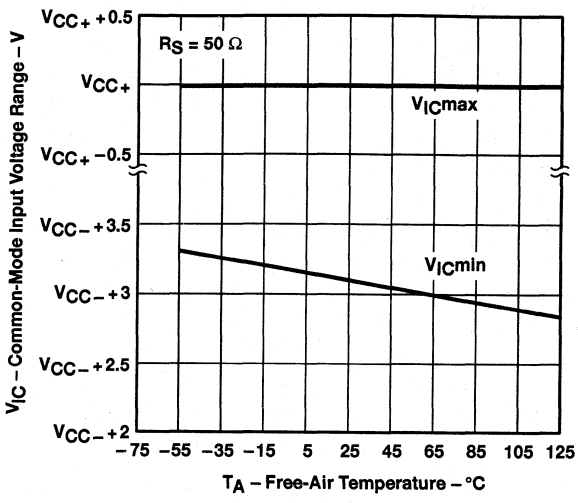


Figure 11

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

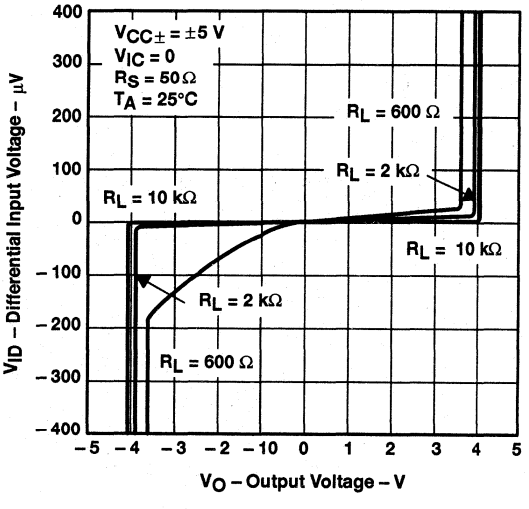


Figure 12

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

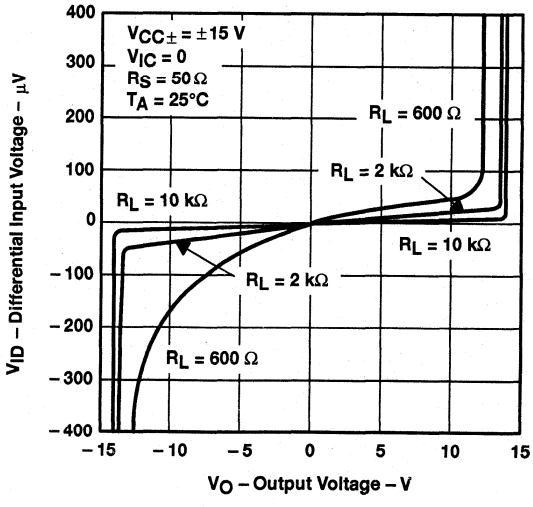


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

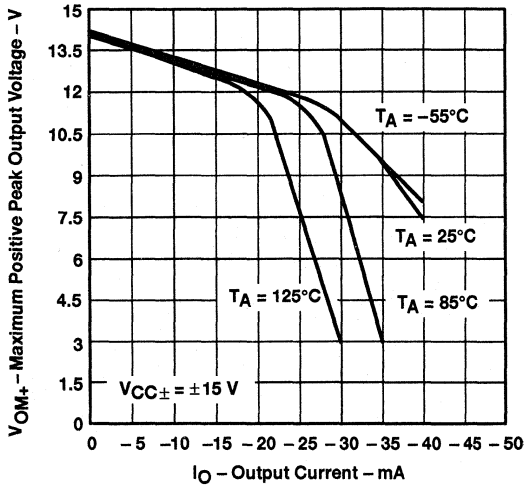


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

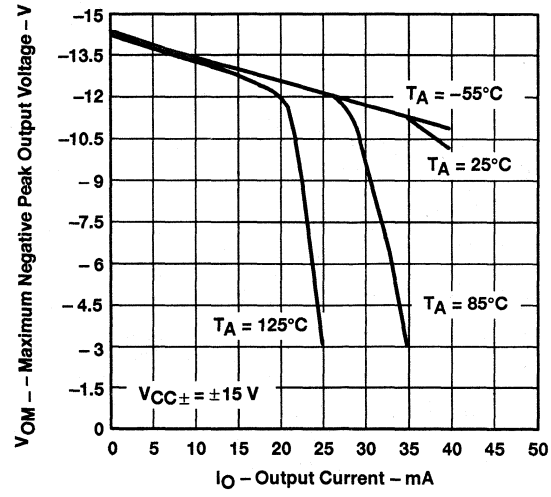


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

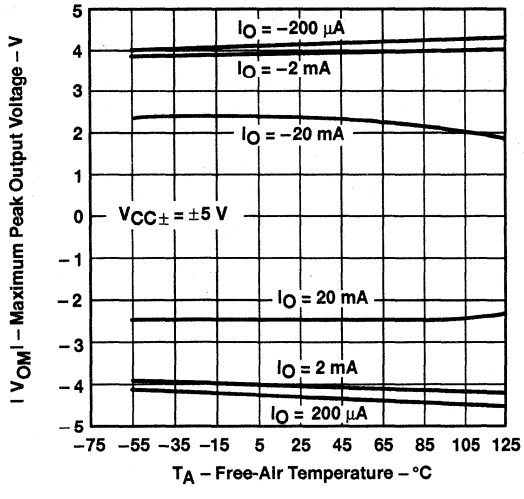


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

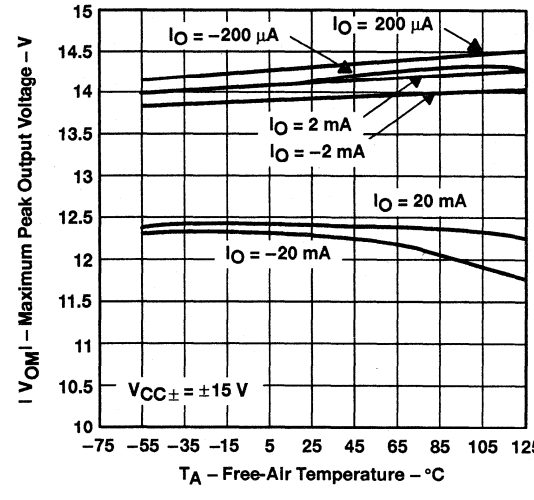


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

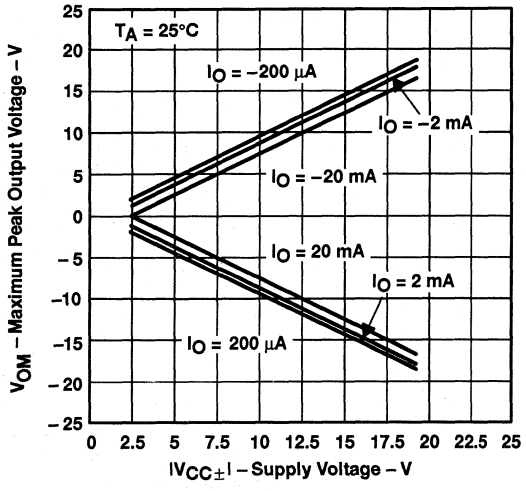


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

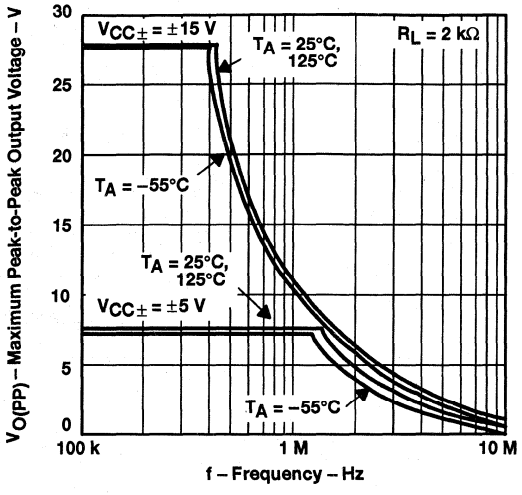


Figure 19

OUTPUT VOLTAGE
vs
SETTLING TIME

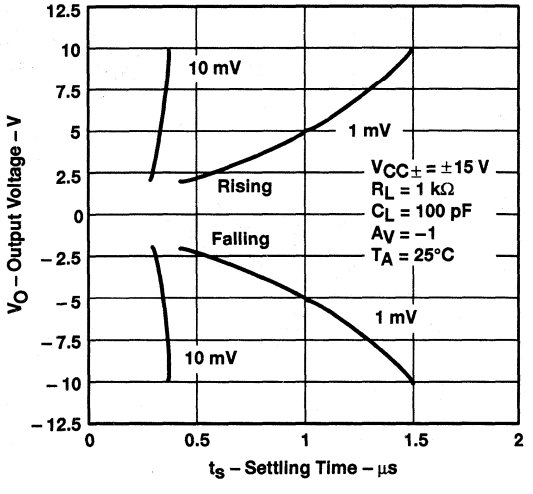


Figure 20

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

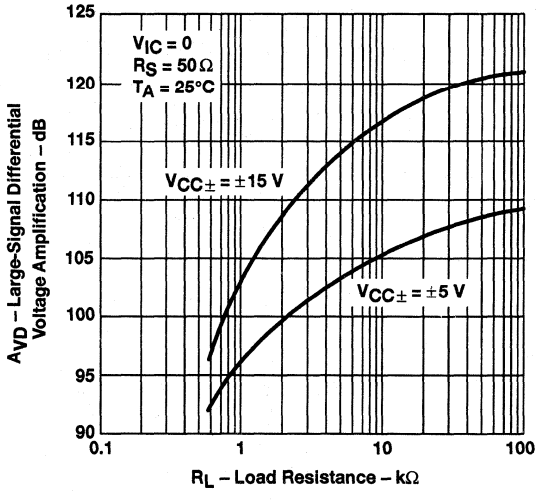


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

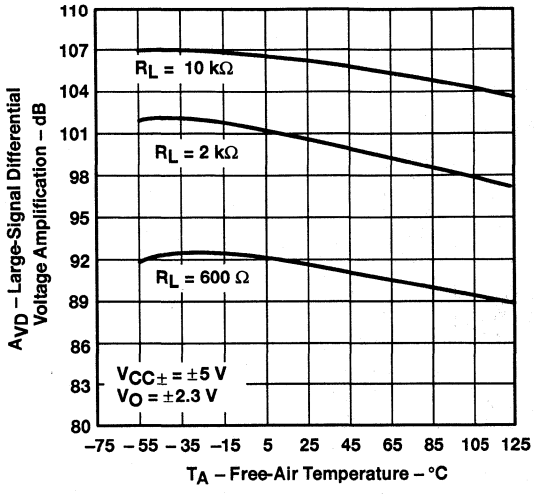


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

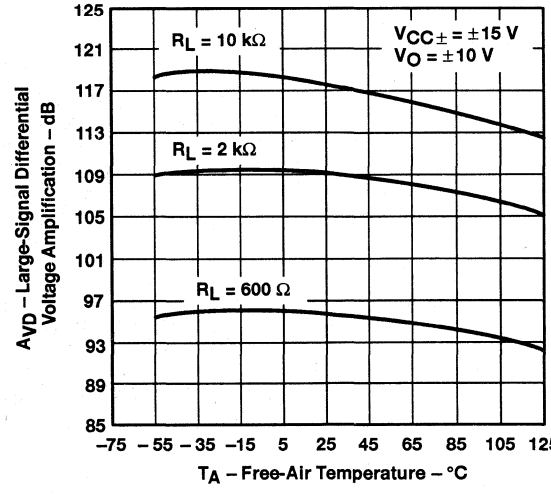


Figure 23

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

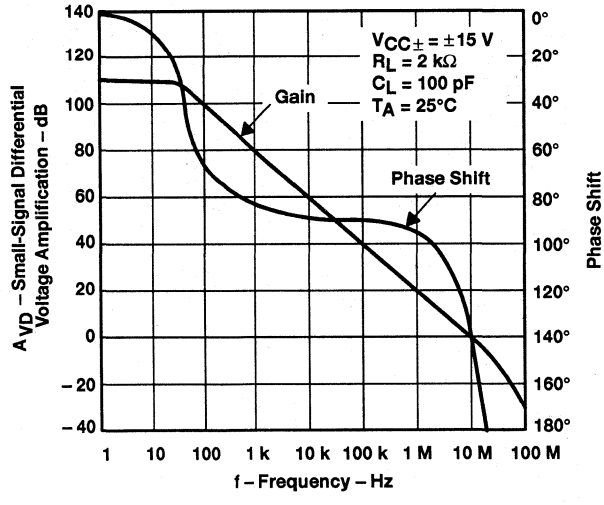


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

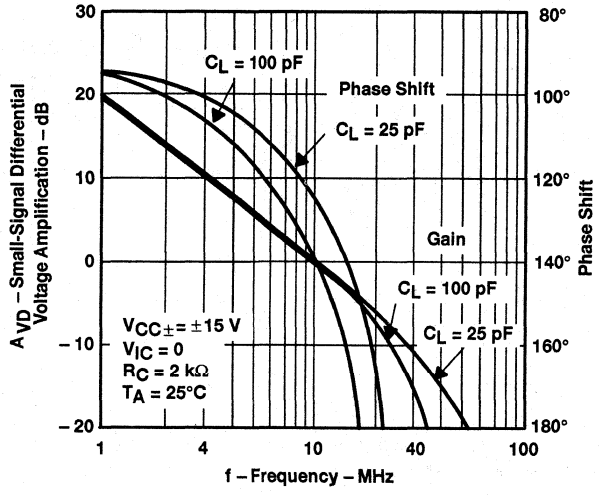


Figure 25

COMMON-MODE REJECTION RATIO vs FREQUENCY

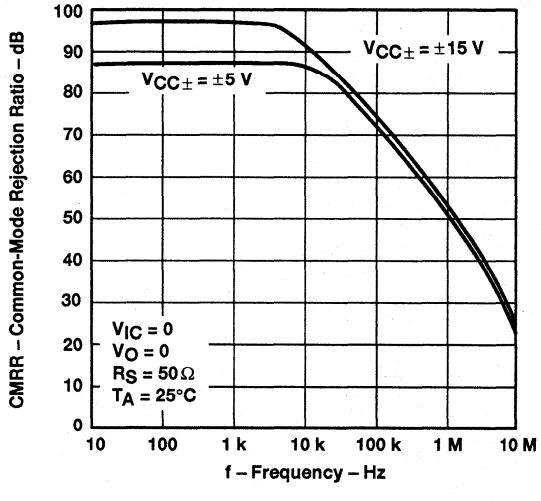


Figure 26

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

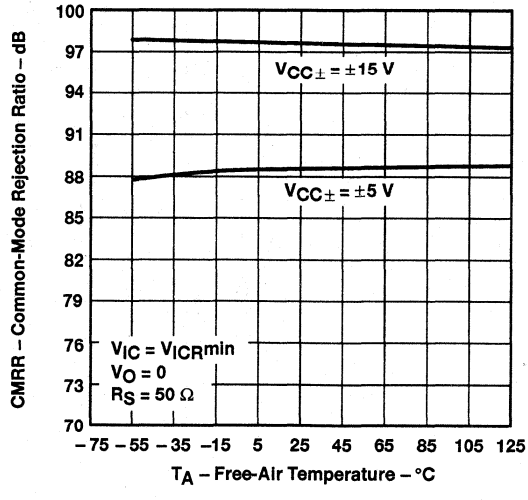


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

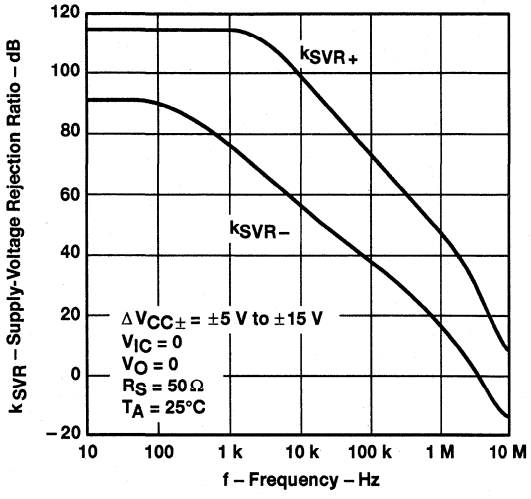


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

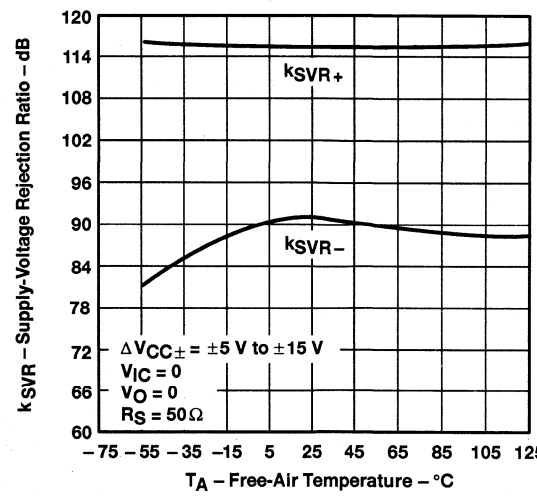


Figure 29

SUPPLY CURRENT vs SUPPLY VOLTAGE

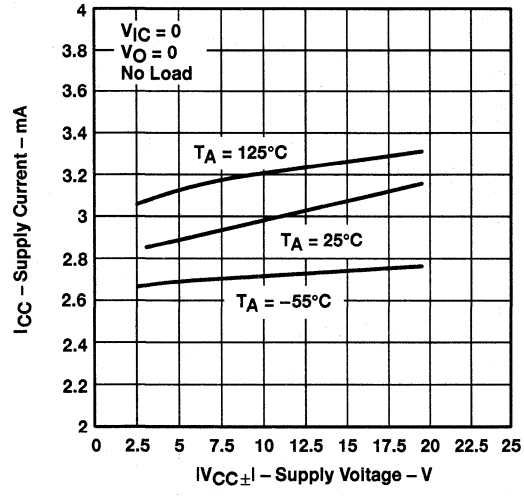


Figure 30

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

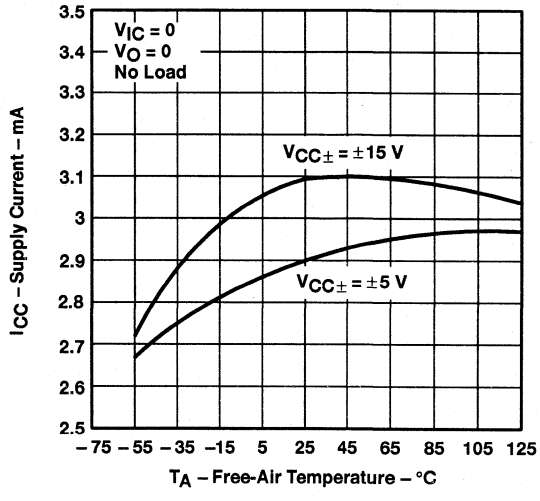


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

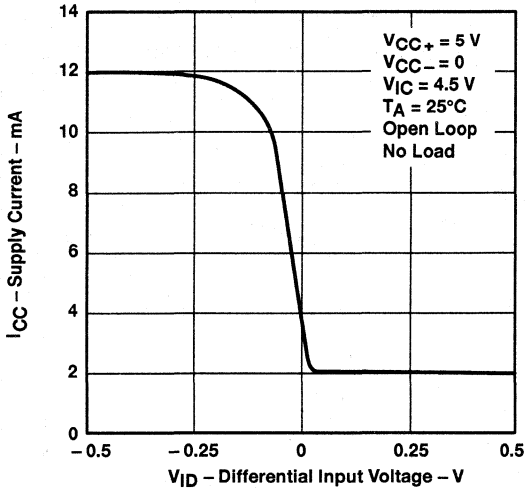


Figure 32

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

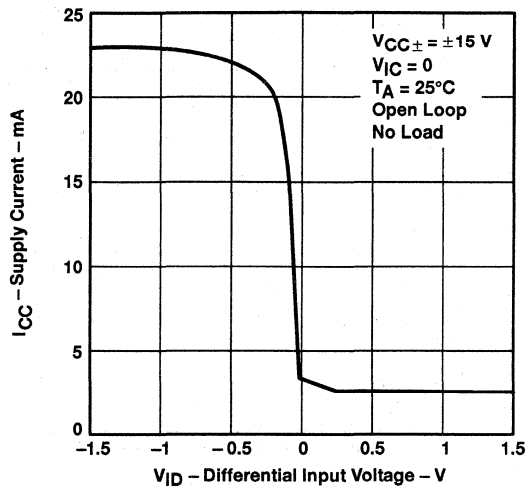


Figure 33

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

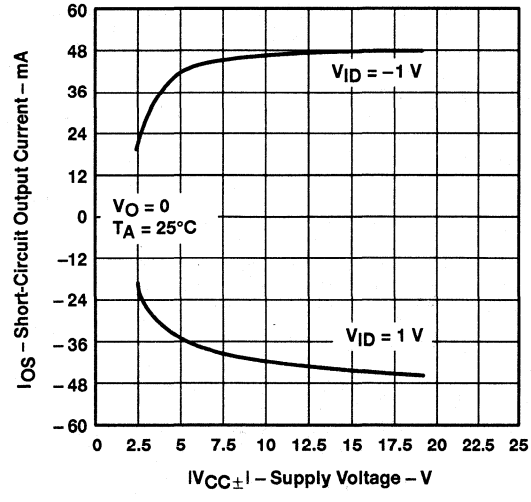


Figure 34

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

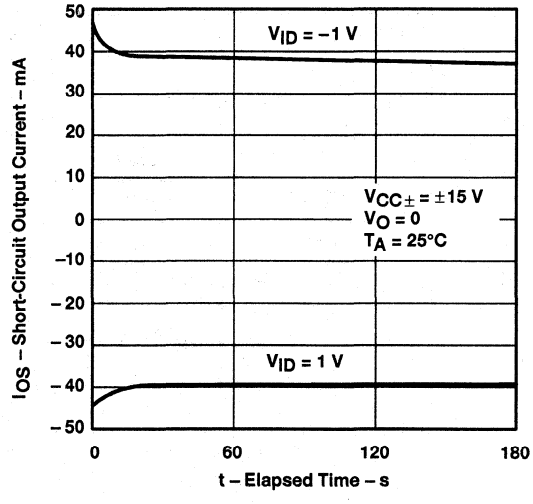


Figure 35

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

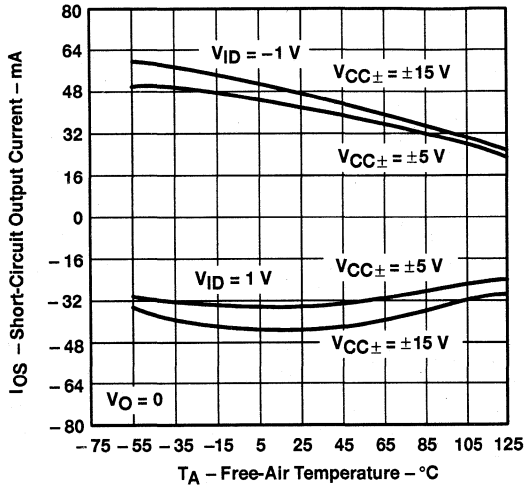


Figure 36

SLEW RATE vs FREE-AIR TEMPERATURE

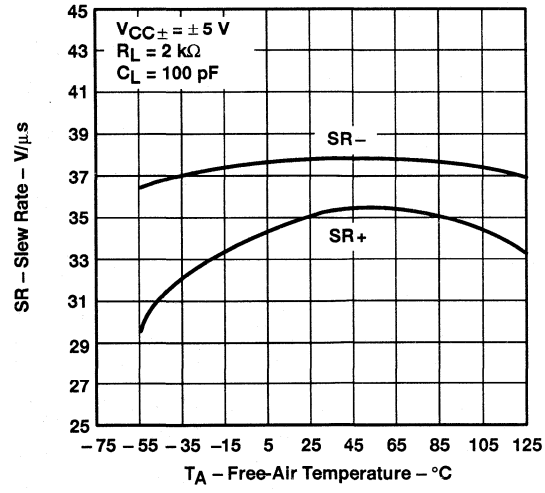


Figure 37

SLEW RATE vs FREE-AIR TEMPERATURE

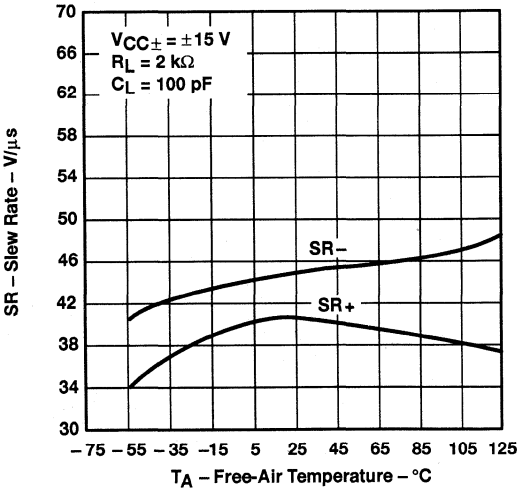


Figure 38

SLEW RATE vs LOAD RESISTANCE

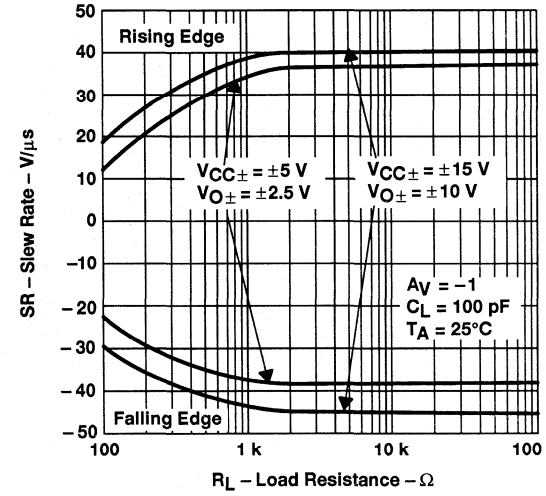


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

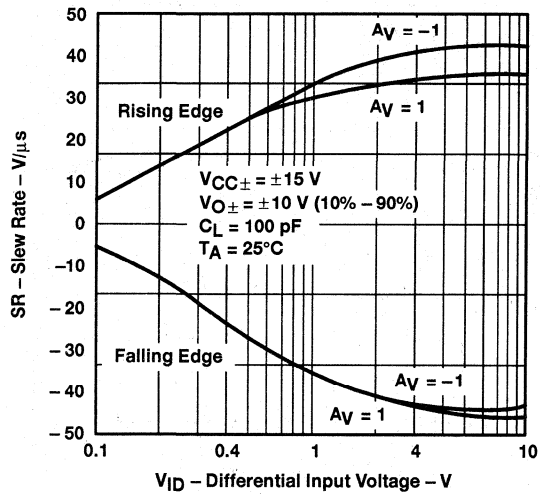


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

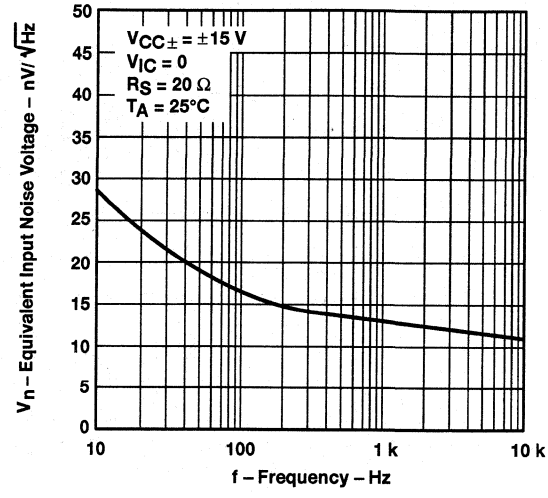


Figure 41

INPUT-REFERRED NOISE VOLTAGE vs NOISE BANDWIDTH

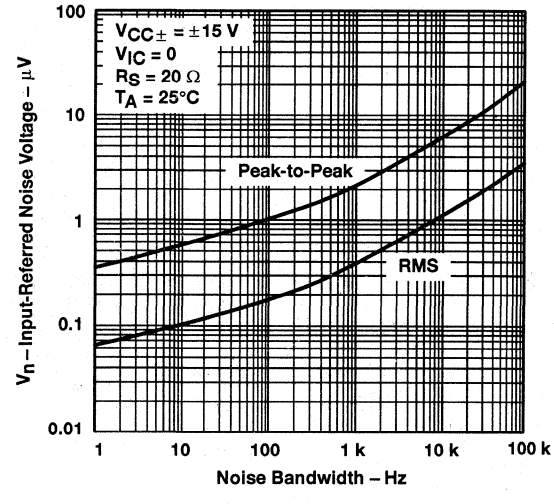


Figure 42

INPUT-REFERRED NOISE VOLTAGE OVER A 10-SECOND TIME INTERVAL

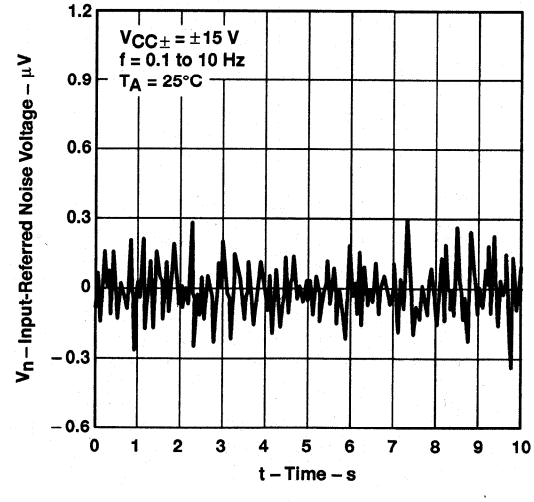


Figure 43

TYPICAL CHARACTERISTICS

THIRD-OCTAVE SPECTRAL NOISE DENSITY
vs
FREQUENCY BANDS

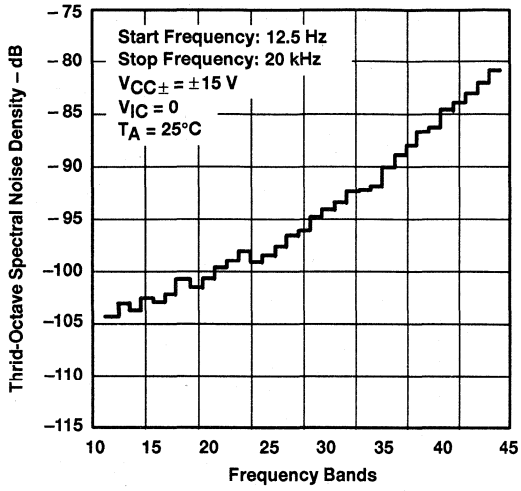


Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

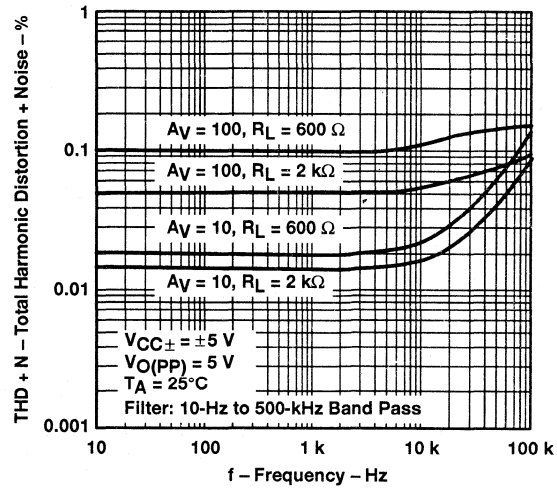


Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

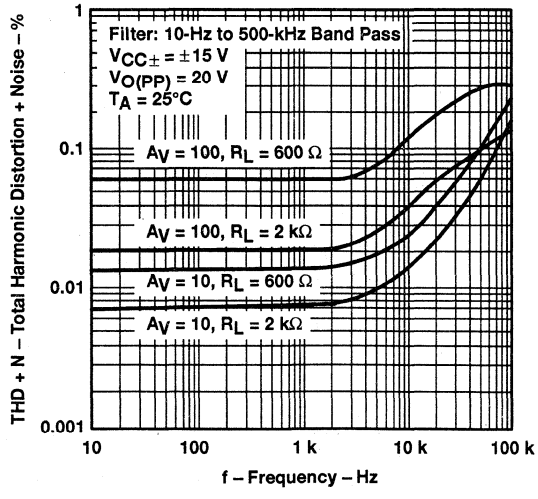


Figure 46

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

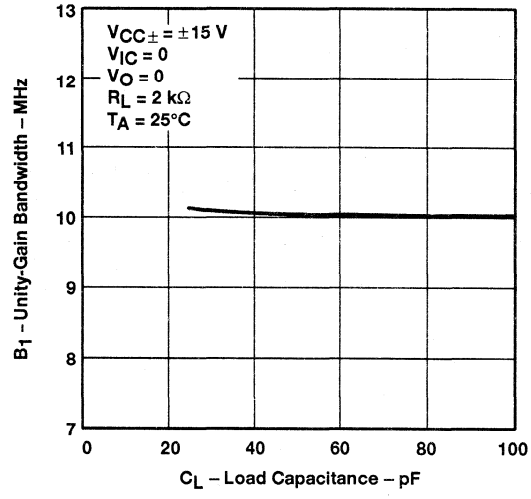


Figure 47

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

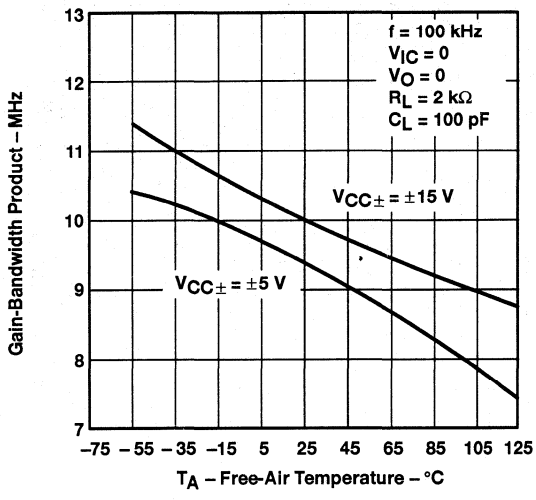


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

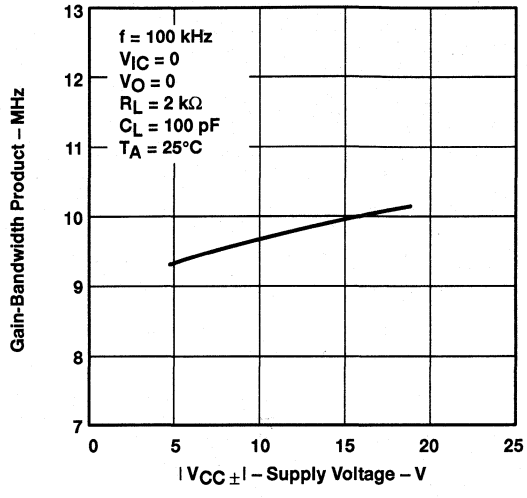


Figure 49

GAIN MARGIN
vs
LOAD CAPACITANCE

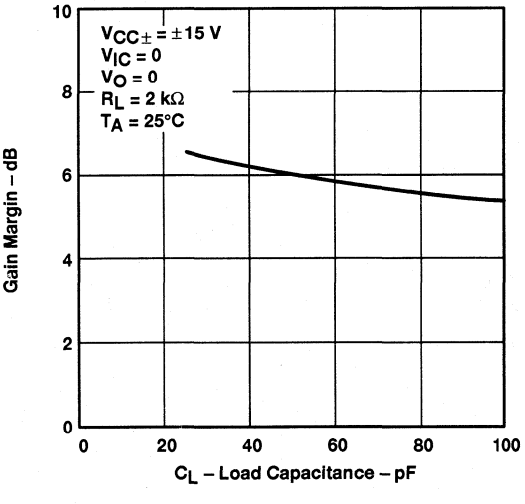


Figure 50

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

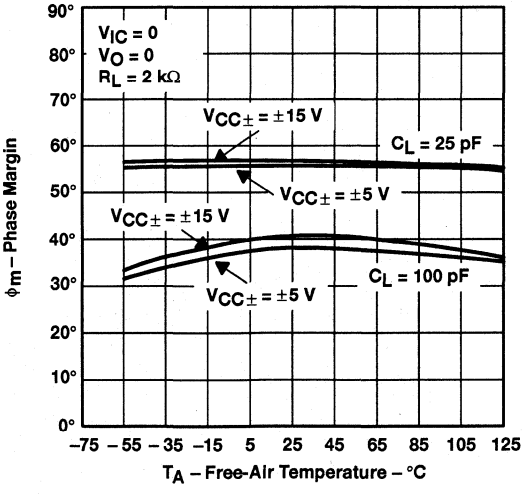


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

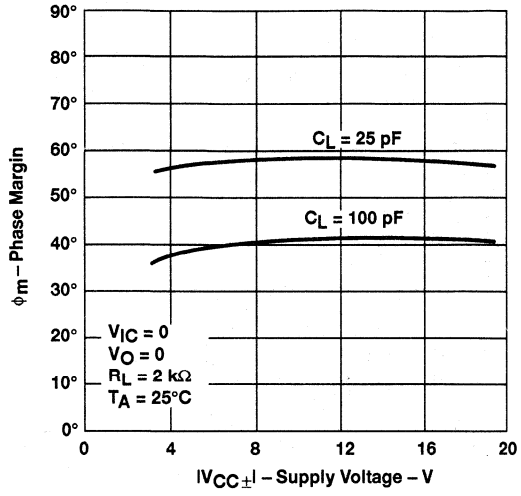


Figure 52

PHASE MARGIN
vs
LOAD CAPACITANCE

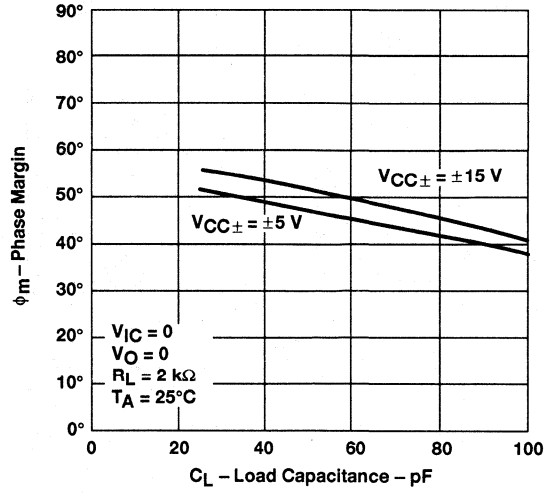


Figure 53

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

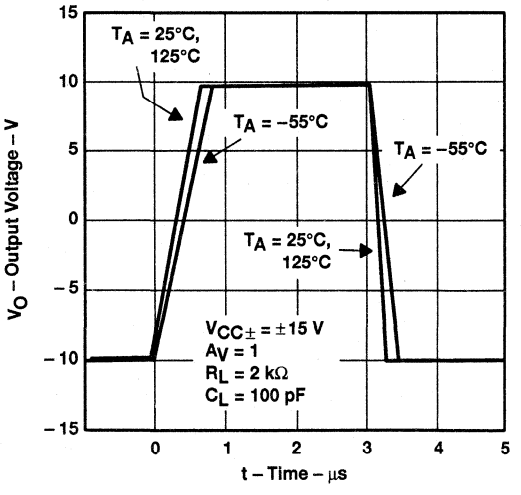


Figure 54

SMALL-SIGNAL PULSE RESPONSE

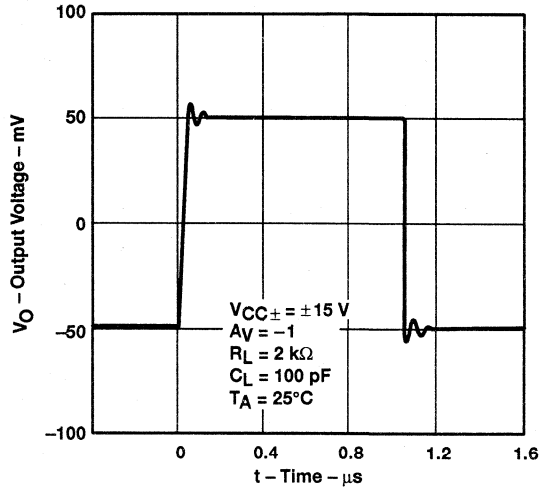


Figure 55

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

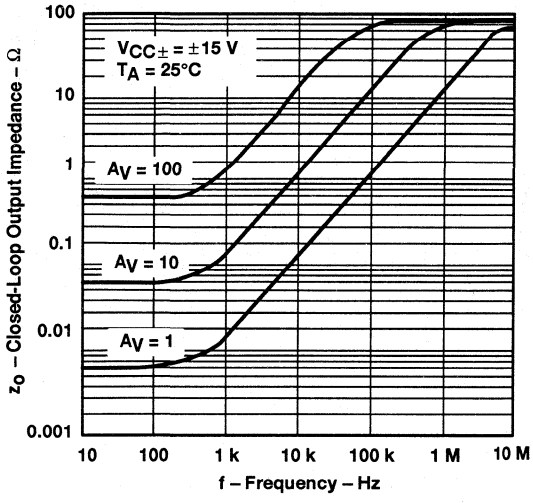


Figure 56

CROSSTALK ATTENUATION vs FREQUENCY

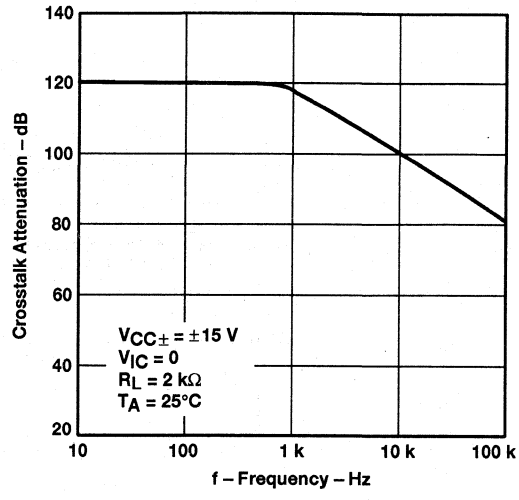


Figure 57

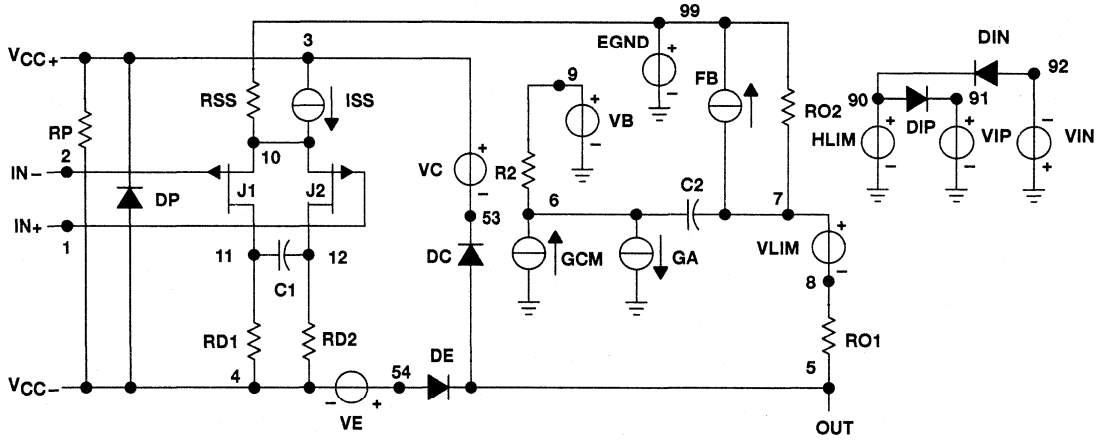
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 4) and subcircuit in Figure 58 are generated using the TLE2082 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G.R. Boyle, B.M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLE2082 1 2 3 4 5
C1      11      12      2.2E-12
C2      6       7       10.00E-12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
FB      7       99      POLY (5) VB VC VE VLP
+ VLN 0 5.607E6 –6E6 6E6 6E6 –6E6
GA      6       0       11 12 333.0E–6
GCM     0       6       10 99 7.43E–9
ISS     3       10      DC 400.0E–6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.0E3
RD1     4       11      3.003E3
RD2     4       12      3.003E3
R01     8       5       80
R02     7       99      80
RP      3       4       27.30E3
RSS     10      99      500.0E3
VB      9       0       DC 0
VC      3       53      DC 2.20
VE      54      4       DC 2.20
VLIM    7       8       DC 0
VLP     91      0       DC 45
VLN     0       92      DC 45
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=15.00E–12 BETA=554.5E–6
+ VTO= –.6)
.ENDS
```

Figure 58. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

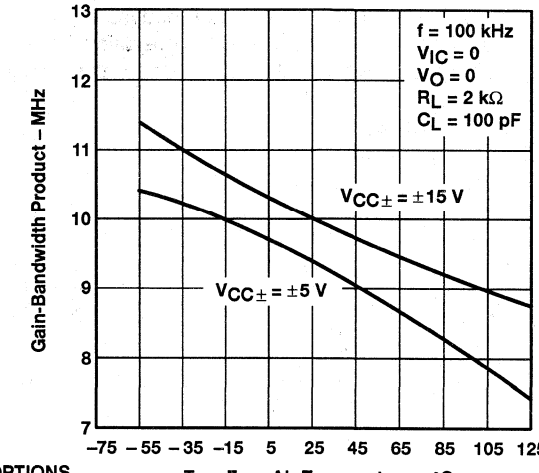
- **25-V/μs Slew Rate Min**
- **High Gain-Bandwidth Product . . . 10 MHz**
- **±30-mA Minimum Short-Circuit Output Current**
- **Wide Supply Voltage Range ±2.25 V to ±19 V**
- **Input Range Includes the Positive Supply**
- **Macromodel Included**
- **Fast Settling Time Using 10-V Step 400 ns to 10 mV Typ 1.5 μs to 1 mV Typ**

description

The TLE2084 and TLE2084A are high-speed, high-performance, internally-compensated, JFET-input quadruple operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2084A has a lower input offset voltage than the TLE2084. Both are pin-compatible upgrades to standard industry products.

This design features a 25-V/μs minimum slew rate, which results in the low distortion and high-power bandwidth necessary for high-fidelity audio applications. Settling time to 0.1% of a 10-V step (1-kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8 MHz minimum. As such, the TLE2084 and TLE2084A offer significant speed and noise advantages at a low 1.6-mA typical supply current per channel.

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	4 mV 7 mV	TLE2084ACDW TLE2084CDW	—	—	TLE2084ACN TLE2084CN	— TLE2084Y
–55°C to 125°C	4 mV 7 mV	—	TLE2084AMFK TLE2084MFK	TLE2084AMJ TLE2084MJ	—	—

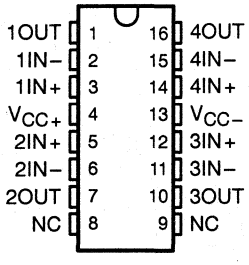
The DW packages are available taped and reeled. Add R suffix to device type (e.g., TLE2084ACDWR). Chip-form versions are tested at T_A = 25°C. For chip-form orders, contact your local TI sales office.

description (continued)

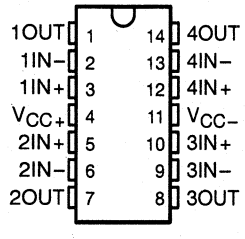
The input current characteristics traditionally associated with JFET-input amplifiers have been maintained. Input offset voltage is graded to a 7 mV and 4 mV maximum for the TLE2084 and TLE2084A, respectively. Typically, temperature coefficient of input offset voltage is 10.1 μV/°C and typical CMRR and k_{SVR} are 98 dB and 99 dB, respectively. Device performance is relatively independent of supply voltage over the wide ±2.25-V to ±19-V range. The input common-mode voltage range extends from the positive supply down to V_{CC-} + 4 V without significant degradation to dynamic performance. Maximum peak output voltage swing is from V_{CC+} – 1 V to V_{CC-} + 1 V under light loading conditions. The output is capable of sourcing and sinking a minimum of 30 mA and can sustain shorts to either supply. Care must be taken to ensure that maximum power dissipation is not exceeded.

Both the TLE2084 and TLE2084A are available in a wide variety of packages, including both the industry-standard 16-pin wide-body SOIC and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C and the M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

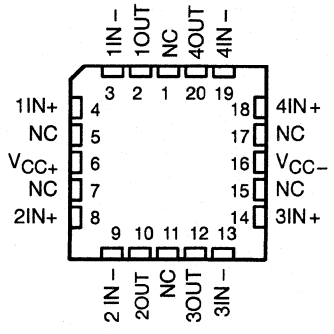
DW PACKAGE
(TOP VIEW)



J OR N PACKAGE
(TOP VIEW)

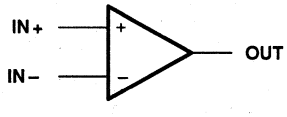


FK PACKAGE
(TOP VIEW)



NC – No internal connection

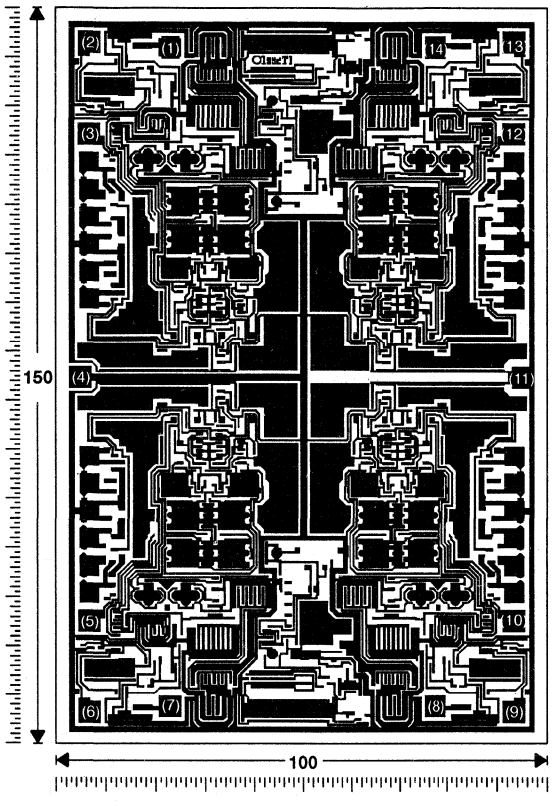
symbol

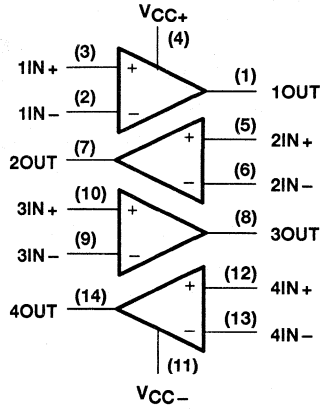


TLE2084Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2084. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

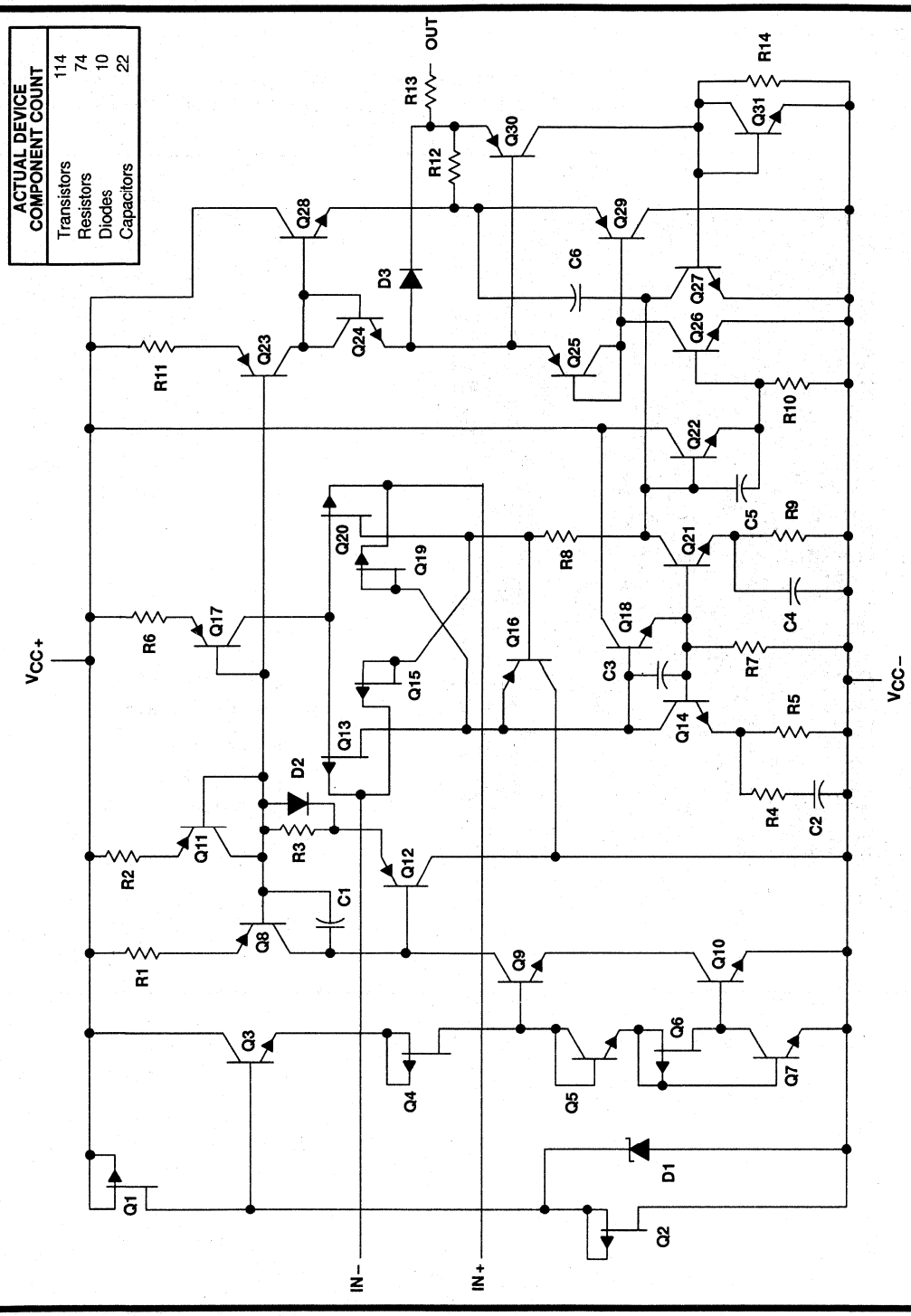
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} (see Note 1) ..... −19 V
Differential input voltage range, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-}
Input current, I_I (each input) ..... ±1 mA
Output current, I_O (each output) ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output can be shorted to either supply. Temperatures and/or supply voltages must be limited to ensure that the maximum dissipation rate is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		C SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2.25	±19	±2.25	±19	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm5$ V	−0.9	5	−0.8	5	V
	$V_{CC\pm} = \pm15$ V	−10.9	15	−10.8	15	
Operating free-air temperature, T_A		0	70	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2084C			TLE2084AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		−1.6	7		−0.5	4	mV
				Full range			9.1			6.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		10.1	30		10.1	30	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		5 to −1	5 to −1.9		V
				Full range	5 to −0.9			5 to −0.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.7			3.7			
		I_O = −2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.4			3.4			
		I_O = −20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.5			1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	−3.8	−4.2		−3.8	−4.2		V
				Full range	−3.7			−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.4			−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		−1.5	−2.4		
				Full range	−1.5			−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (four amplifiers)	V_O = 0, No load		25°C	5.2	6.3	7.5	5.2	6.3	7.5	mA
				Full range			7.5			7.5	
a_x	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35			−35		mA
			V_{ID} = −1 V			45			45		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2084C			TLE2084AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	22			22			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2084C			TLE2084AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		–1.6	7		–0.5	4	mV
				Full range			9.1			6.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		10.1	30		10.1	30	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
				Full range			1.4			1.4	nA
I_{IB}	Input bias current			25°C		25	175		25	175	pA
				Full range			5			5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to –11	15 to –11.9		15 to –11	15 to –11.9		V
				Full range	15 to –10.9			15 to –10.9			
V_{OM+}	Maximum positive peak output voltage swing	I_O = –200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = –2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.4			13.4			
		I_O = –20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	–13.8	–14.2		–13.8	–14.2		V
				Full range	–13.7			–13.7			
		I_O = 2 mA		25°C	–13.7	–14		–13.7	–14		
				Full range	–13.6			–13.6			
		I_O = 20 mA		25°C	–11.5	–12.4		–11.5	–12.4		
				Full range	–11.5			–11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	79			79			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	89			89			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	94			94			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	79			79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	81			81			
I_{CC}	Supply current (four amplifiers)	V_O = 0, No load		25°C	5.2	6.5	7.5	5.2	6.5	7.5	mA
				Full range			7.5			7.5	
a_x	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	–30	–45		–30	–45		mA
			V_{ID} = –1 V		30	48		30	48		

† Full range is 0°C to 70°C.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V

PARAMETER		TEST CONDITIONS		T_A†	TLE2084C			TLE2084AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, R_L = 2 kΩ, See Figure 1	A_{VD} = −1, C_L = 100 pF,	25°C	25	40		25	40		V/μs
				Full range	22			22			
SR−	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	25			25			
t_s	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2084M			TLE2084AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		–1.6	7		–0.5	4	mV
				Full range			12.5			9.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		Full range		10.1	30*		10.1	30*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current			25°C		20	175		20	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to –1	5 to –1.9		5 to –1	5 to –1.9		V
				Full range	5 to –0.8			5 to –0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = –200 µA		25°C	3.8	4.1		3.8	4.1		V
				Full range	3.6			3.6			
		I_O = –2 mA		25°C	3.5	3.9		3.5	3.9		
				Full range	3.3			3.3			
		I_O = –20 mA		25°C	1.5	2.3		1.5	2.3		
				Full range	1.4			1.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	–3.8	–4.2		–3.8	–4.2		V
				Full range	–3.6			–3.6			
		I_O = 2 mA		25°C	–3.5	–4.1		–3.5	–4.1		
				Full range	–3.3			–3.3			
		I_O = 20 mA		25°C	–1.5	–2.4		–1.5	–2.4		
				Full range	–1.4			–1.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 2.3 V	R_L = 600 Ω	25°C	80	91		80	91		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	100		90	100		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	106		95	106		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11			11		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		70	89		dB
				Full range	68			68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (four amplifiers)	V_O = 0, No load		25°C	5.2	6.3	7.5	5.2	6.3	7.5	mA
				Full range			7.5			7.5	
a_X	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		–35			–35		mA
			V_{ID} = –1 V			45			45		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is –55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2084M			TLE2084AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35			35		V/μs
				Full range	18*			18*			
SR−	Negative slew rate			25°C		38			38		V/μs
				Full range	18*			18*			
t_s	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25			0.25		μs
			To 1 mV			0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%			0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4			9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8			2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°			56°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2084M			TLE2084AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		–1.6	7		–0.5	4	mV
				Full range			12.5			7.5	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		Full range		10.1	30*		10.1	30*	µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		15	100		15	100	pA
				Full range			20			20	nA
I_{IB}	Input bias current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		25	175		25	175	pA
				Full range			65			65	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to –11	15 to –11.9		15 to –11	15 to –11.9		V
				Full range	15 to –10.8			15 to –10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = –200 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.6			13.6			
		I_O = –2 mA		25°C	13.5	13.9		13.5	13.9		
				Full range	13.3			13.3			
		I_O = –20 mA		25°C	11.5	12.3		11.5	12.3		
				Full range	11.4			11.4			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		25°C	–13.8	–14.2		–13.8	–14.2		V
				Full range	–13.6			–13.6			
		I_O = 2 mA		25°C	–13.5	–14		–13.5	–14		
				Full range	–13.3			–13.3			
		I_O = 20 mA		25°C	–11.5	–12.4		–11.5	–12.4		
				Full range	–11.4			–11.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	25°C	80	96		80	96		dB
				Full range	78			78			
			R_L = 2 kΩ	25°C	90	109		90	109		
				Full range	88			88			
			R_L = 10 kΩ	25°C	95	118		95	118		
				Full range	93			93			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5			7.5		pF
			Differential	25°C		2.5			2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		80	98		dB
				Full range	78			78			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		82	99		dB
				Full range	80			80			
I_{CC}	Supply current (four amplifiers)	V_O = 0, No load		25°C	5.2	6.5	7.5	5.2	6.5	7.5	mA
				Full range			7.5			7.5	
a_x	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120			120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	–30	–45		–30	–45		mA
			V_{ID} = –1 V		30	48		30	48		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is –55°C to 125°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2084M			TLE2084AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$V_{O(PP)}$ = 10 V, A_{VD} = –1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C	25	40		25	40		V/μs
				Full range	17			17			
SR–	Negative slew rate			25°C	30	45		30	45		V/μs
				Full range	20			20			
t_s	Settling time	A_{VD} = –1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4			0.4		μs
			To 1 mV			1.5			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28			28		nV/√Hz
			f = 10 kHz			11.6			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6			6		μV
			f = 0.1 Hz to 10 Hz			0.6			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8			2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%			0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8*	10		8*	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = –1, C_L = 25 pF	25°C	478*	637		478*	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°			57°		

*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† Full range is –55°C to 125°C.

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2084Y MIN	TLE2084Y TYP	TLE2084Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	V_O = 0,			7	mV
I_{IO}	Input offset current	V_{IC} = 0, See Figure 4	V_O = 0,		15	100	pA
I_{IB}	Input bias current				25	175	pA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		15 to −11	15 to 11.9		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 µA		13.8	14.1		V
		I_O = −2 mA		13.5	13.9		
		I_O = −20 mA		11.5	12.3		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 µA		−13.8	−14.2		V
		I_O = 2 mA		−13.5	−14		
		I_O = 20 mA		−11.5	−12.4		
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V	R_L = 600 Ω	80	96		dB
			R_L = 2 kΩ	90	109		
			R_L = 10 kΩ	95	118		
r_i	Input resistance	V_{IC} = 0			10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode		7.5		pF
			Differential		2.5		
z_o	Open-loop output impedance	f = 1 MHz			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	V_O = 0,	80	98		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		82	99		dB
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	5.2	6.5	7.5	mA
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−30	−45		mA
			V_{ID} = −1 V	30	48		

PARAMETER MEASUREMENT INFORMATION

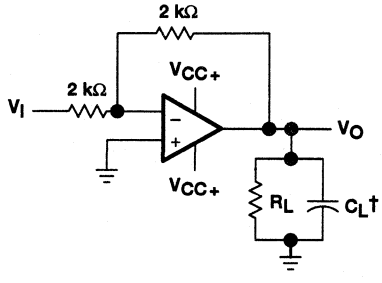


Figure 1. Slew-Rate Test Circuit

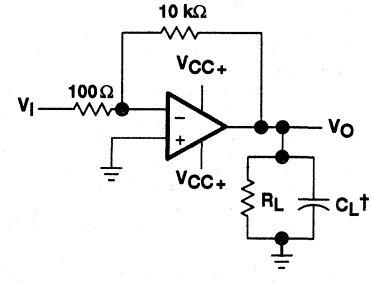


Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

† Includes fixture capacitance

PARAMETER MEASUREMENT INFORMATION

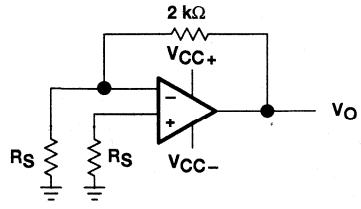


Figure 3. Noise-Voltage Test Circuit

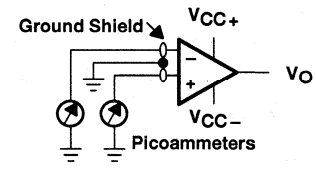


Figure 4. Input-Bias and Offset-Current Test Circuit

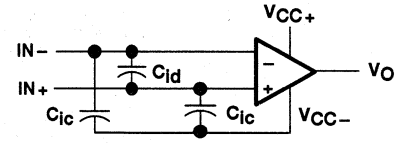


Figure 5. Internal Input Capacitance

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2084 and TLE2084A, accurate measurement of the bias becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test is performed that measures both the socket leakage and the device input bias current. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient	Distribution	7
I_{IO}	Input offset current	vs Free-air temperature	8, 9
I_{IB}	Input bias current	vs Free-air temperature vs Supply voltage	8, 9 10
V_{ICR}	Common-mode input voltage range	vs Free-air temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13

TYPICAL CHARACTERISTICS

Table of Graphs (Continued)

			FIGURE
V_{OM+}	Maximum positive peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	14 16, 17 18
V_{OM-}	Maximum negative peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	15 16, 17 18
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
V_O	Output voltage	vs Settling time	20
A_{VD}	Large-signal differential voltage amplification	vs Load Resistance vs Free-air temperature	21 22, 23
A_{VD}	Small-signal differential voltage amplification	vs Frequency	24, 25
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	26 27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	28 29
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	30 31 32, 33
I_{OS}	Short-circuit output current	vs Supply voltage vs Elasped time vs Free-air temperature	34 35 36
SR	Slew rate	vs Free-air temperature vs Load resistance vs Differential input voltage	37, 38 39 40
V_n	Equivalent input noise voltage	vs Frequency	41
V_n	Input referred noise voltage	vs Noise bandwidth Over a 10-second time interval	42 43
	Third-octave spectral noise density	vs Frequency	44
THD + N	Total harmonic distortion plus noise	vs Frequency	45, 46
B_1	Unity-gain bandwidth	vs Load capacitance	47
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	48 49
	Gain margin	vs Load capacitance	50
ϕ_m	Phase margin	vs Free-air temperature vs Supply voltage vs Load capacitance	51 52 53
	Phase shift	vs Frequency	24, 25
	Large-signal pulse response, noninverting	vs Time	54
	Small-signal pulse response	vs Time	55
z_o	Closed-loop output impedance	vs Frequency	56
a_x	Crosstalk attenuation	vs Frequency	57

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLE2084 INPUT OFFSET VOLTAGE

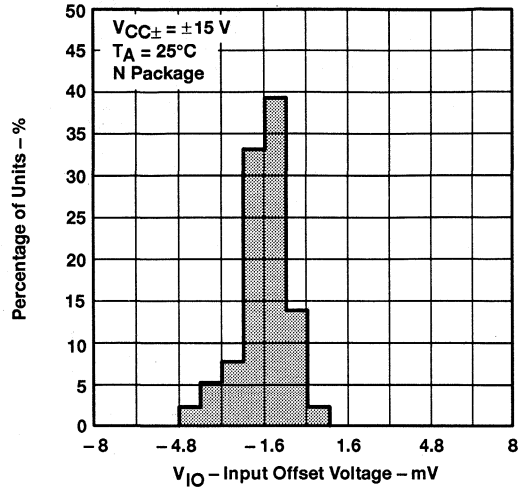


Figure 6

DISTRIBUTION OF TLE2084 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

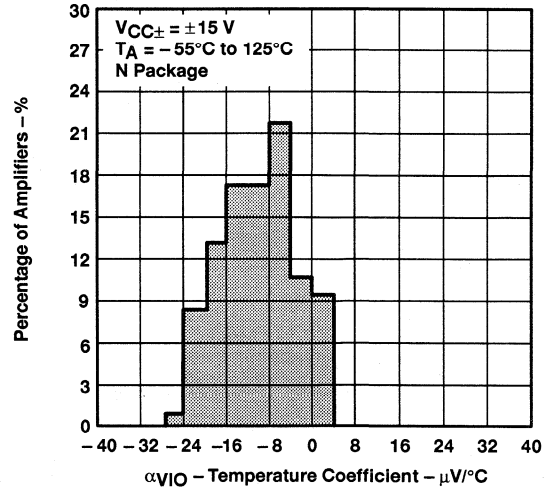


Figure 7

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

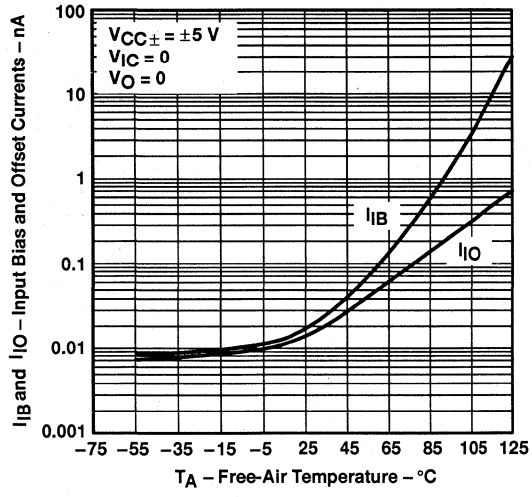


Figure 8

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

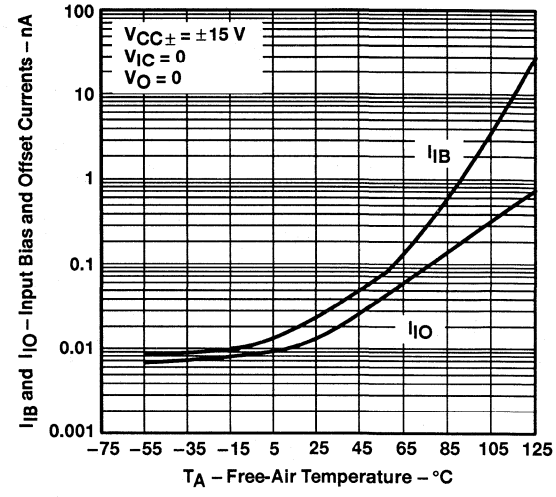


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

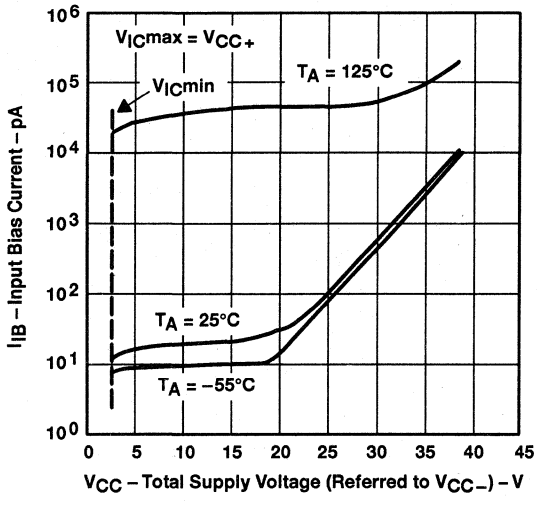


Figure 10

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

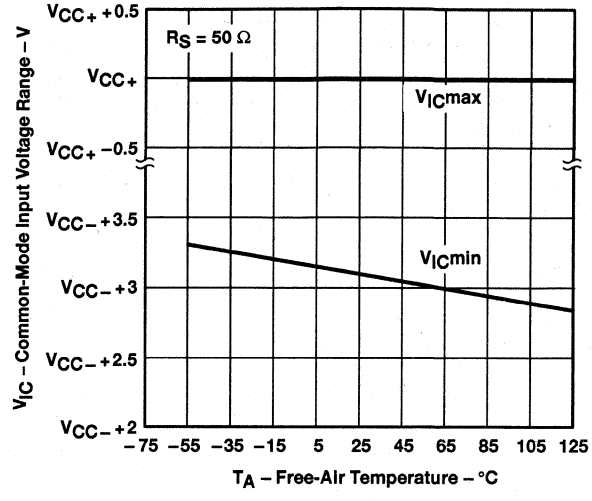


Figure 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

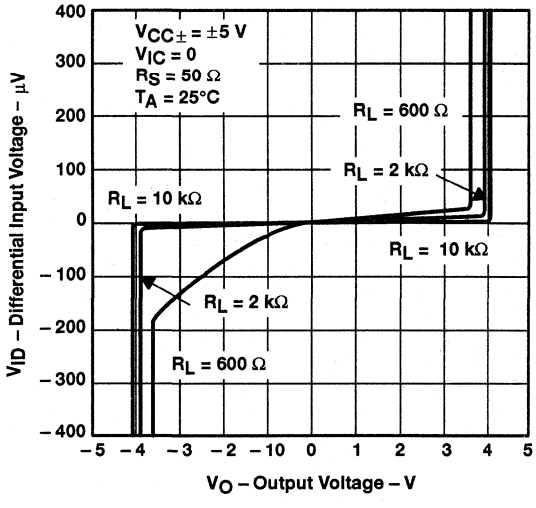


Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

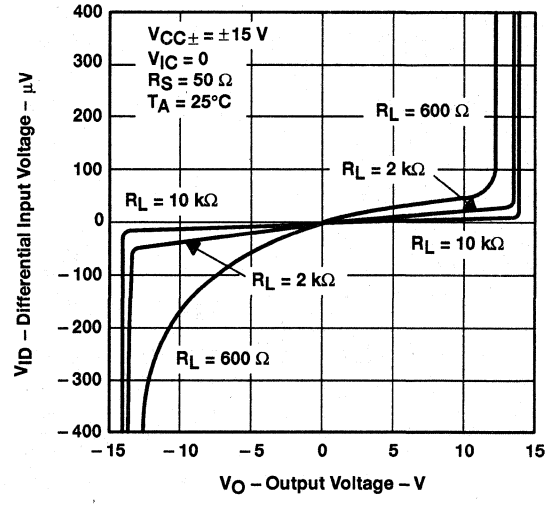


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

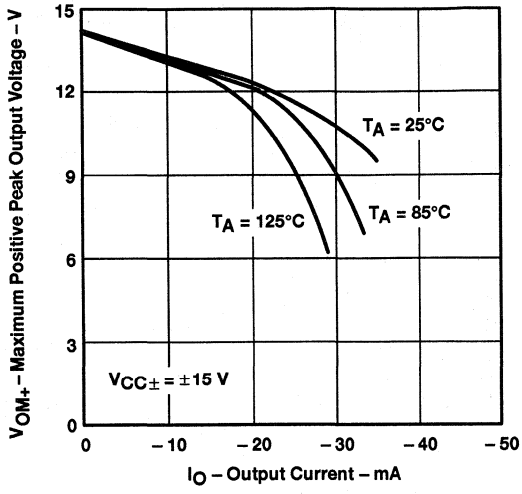


Figure 14

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

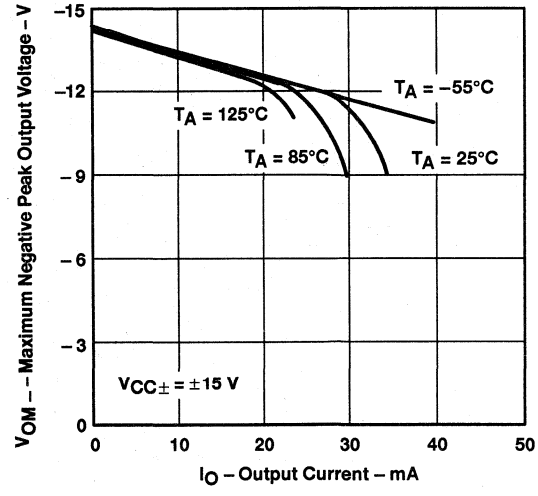


Figure 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

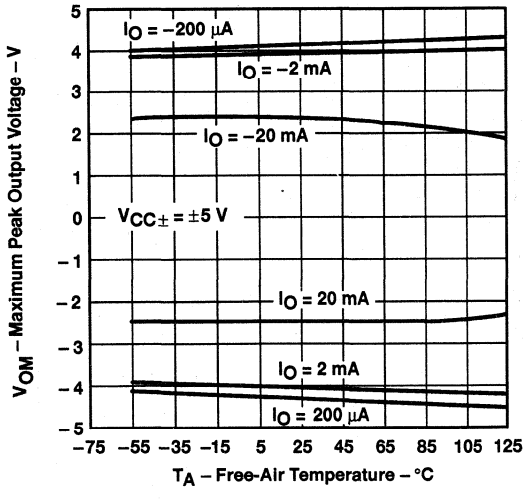


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

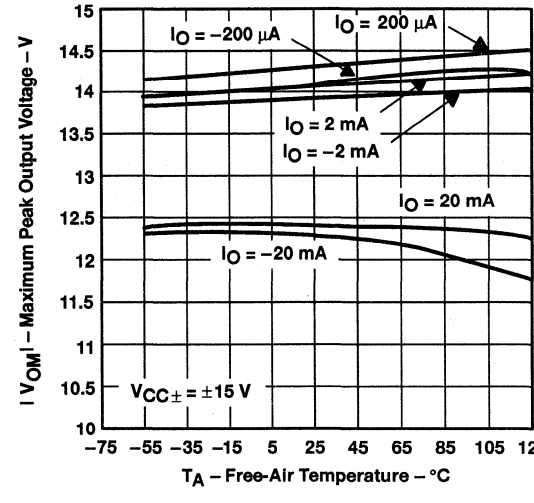


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

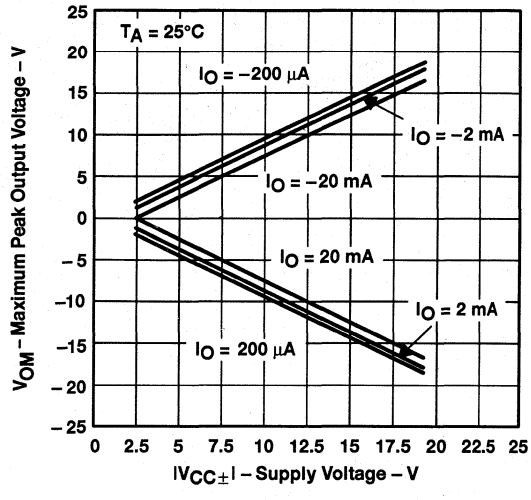


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

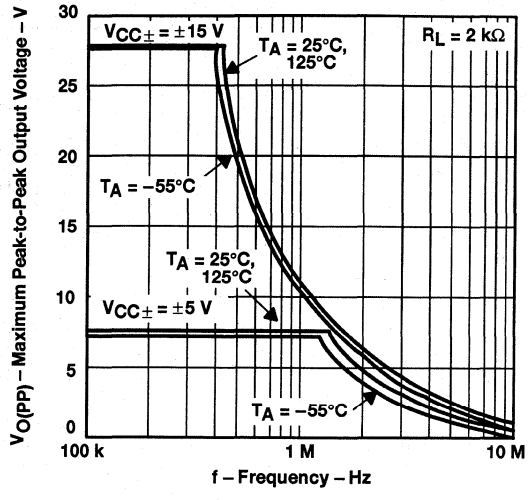


Figure 19

OUTPUT VOLTAGE
vs
SETTLING TIME

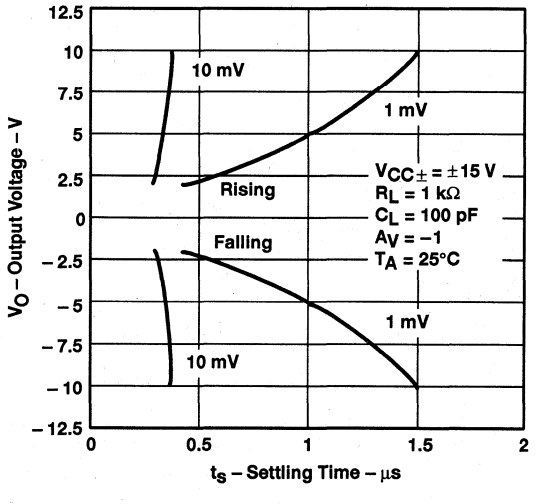


Figure 20

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

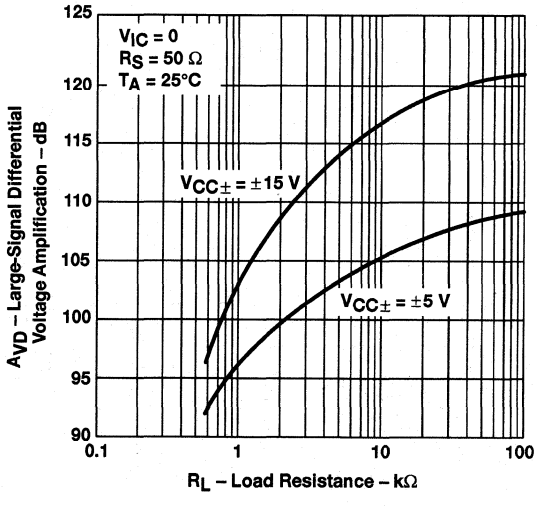


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

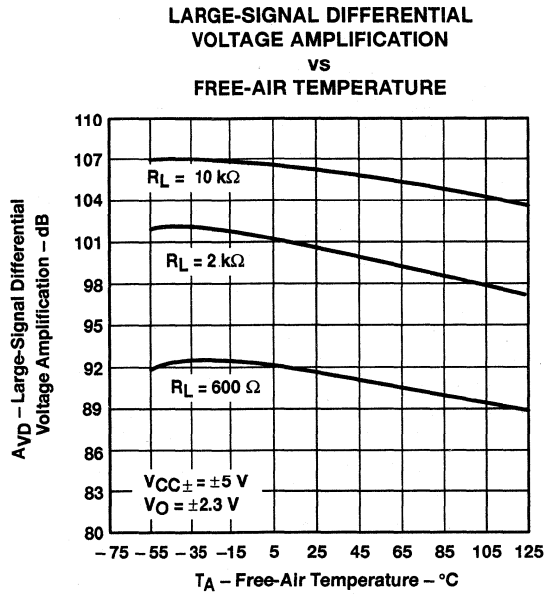


Figure 22

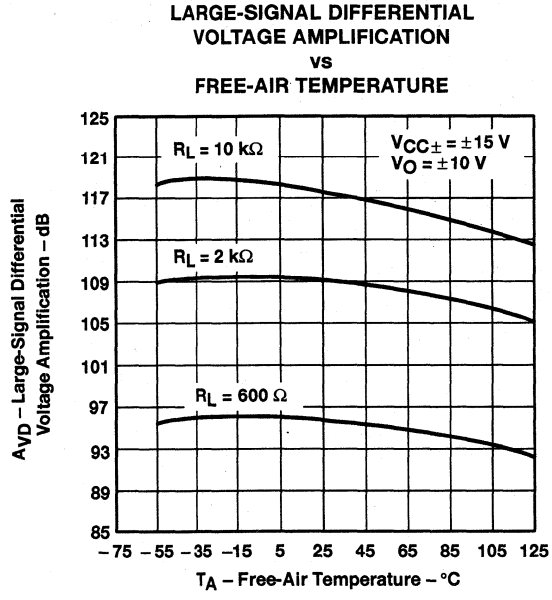


Figure 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

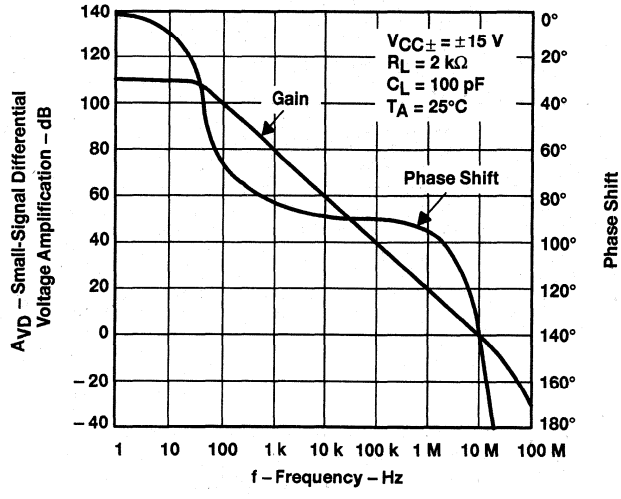


Figure 24

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

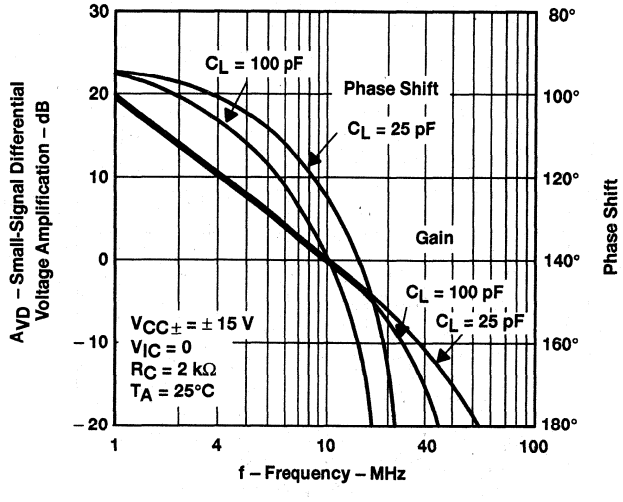


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

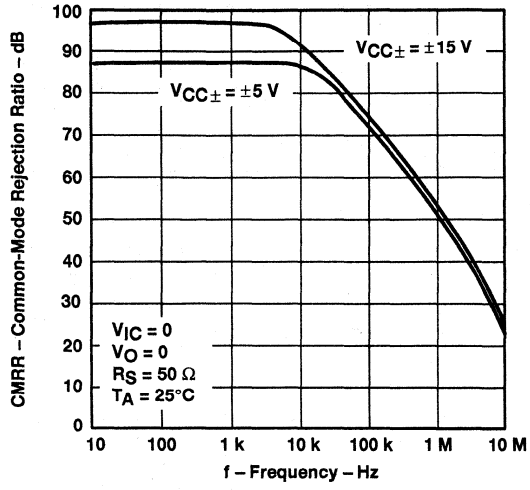


Figure 26

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

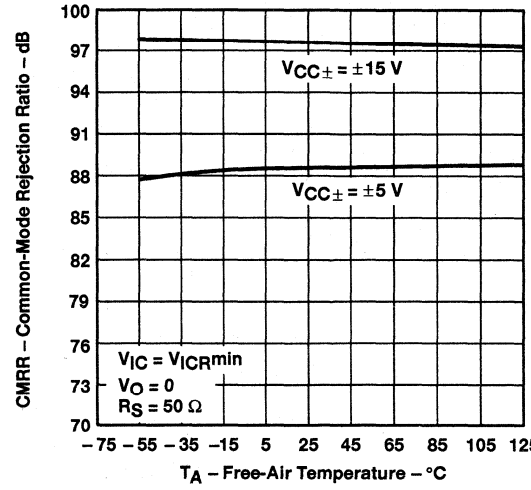


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

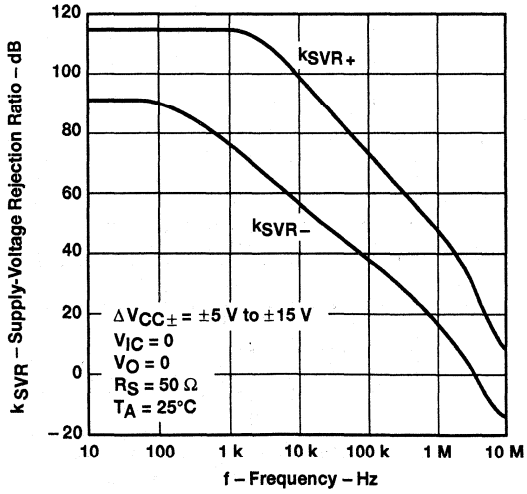


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

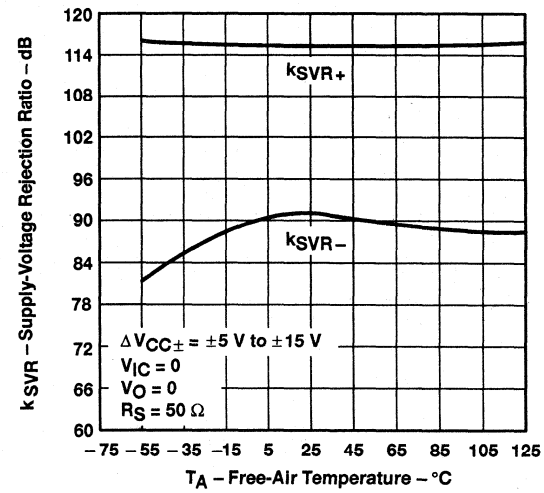


Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE

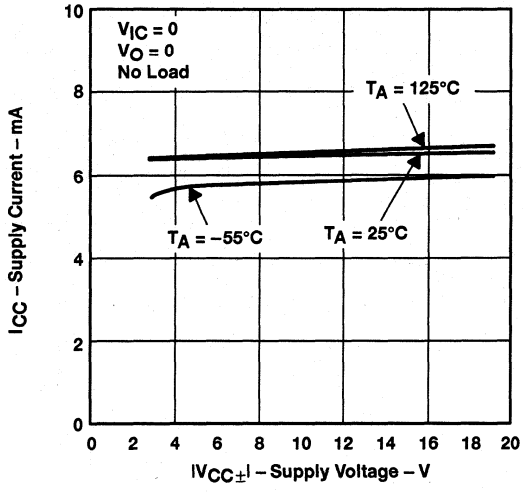


Figure 30

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

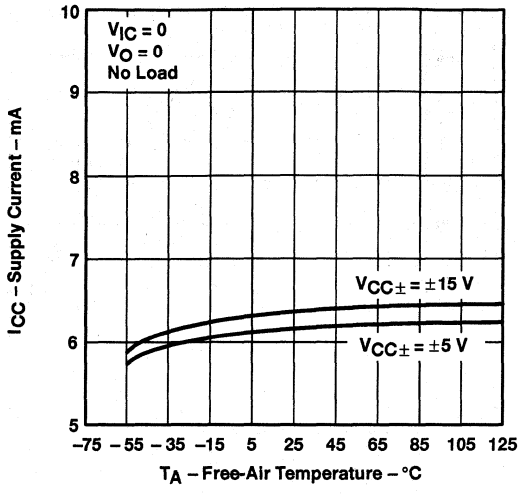


Figure 31

SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE

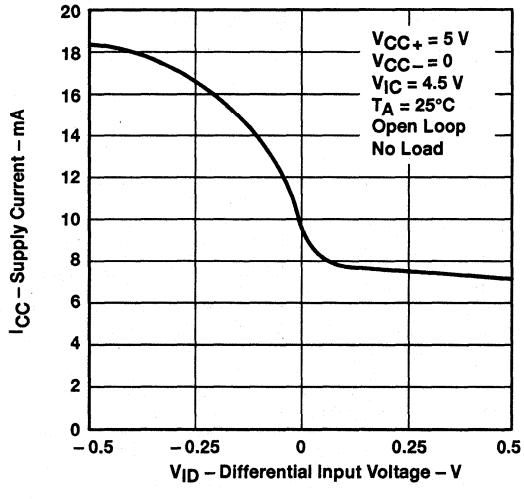


Figure 32

SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE

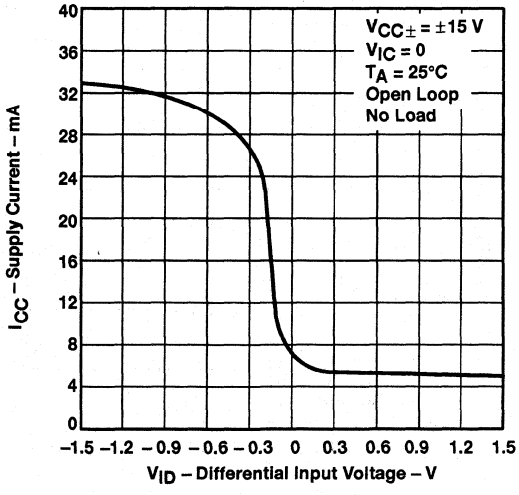


Figure 33

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

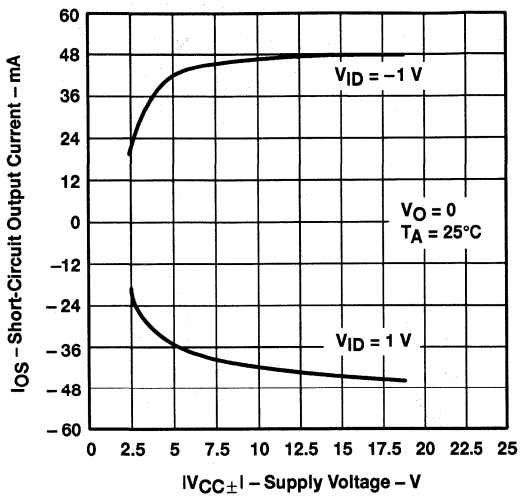


Figure 34

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

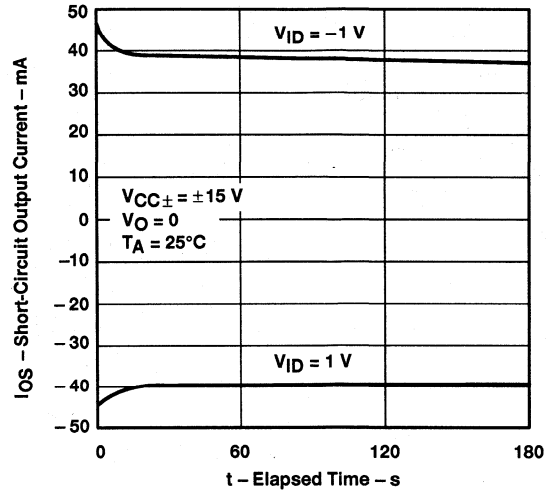


Figure 35

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

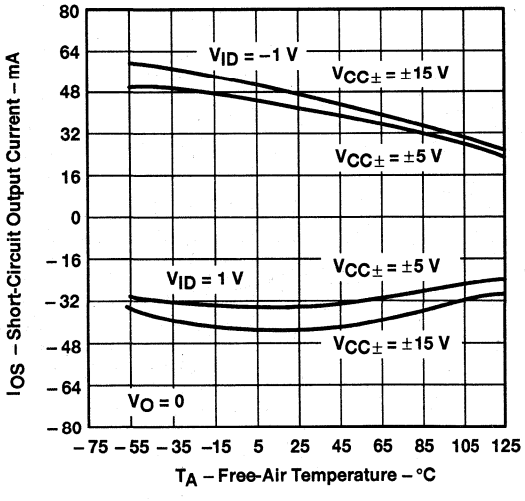


Figure 36

SLEW RATE vs FREE-AIR TEMPERATURE

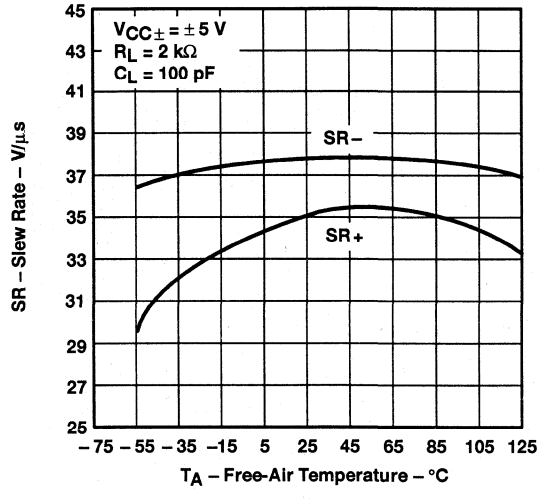


Figure 37

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs FREE-AIR TEMPERATURE

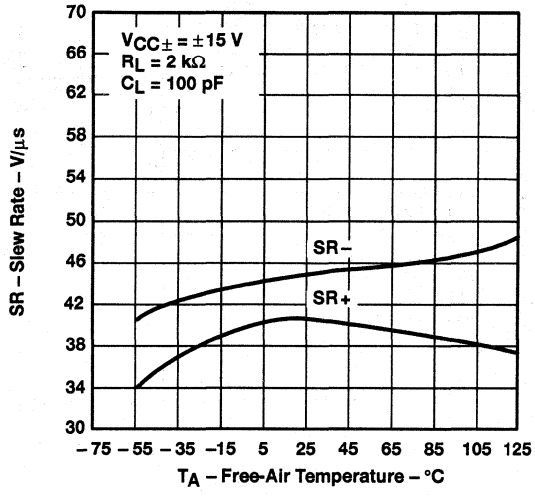


Figure 38

SLEW RATE vs LOAD RESISTANCE

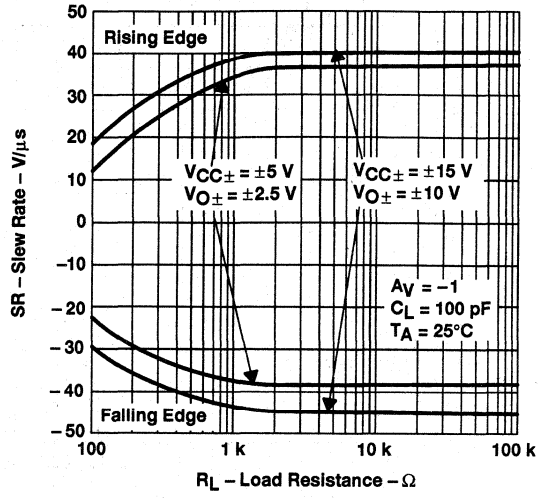


Figure 39

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

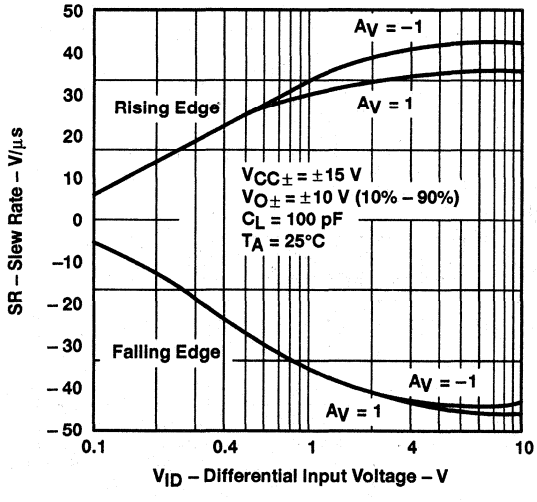


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

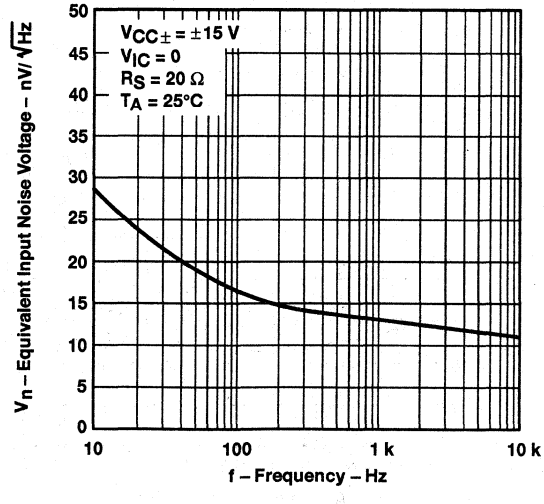


Figure 41

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT-REFERRED NOISE VOLTAGE
vs
NOISE BANDWIDTH

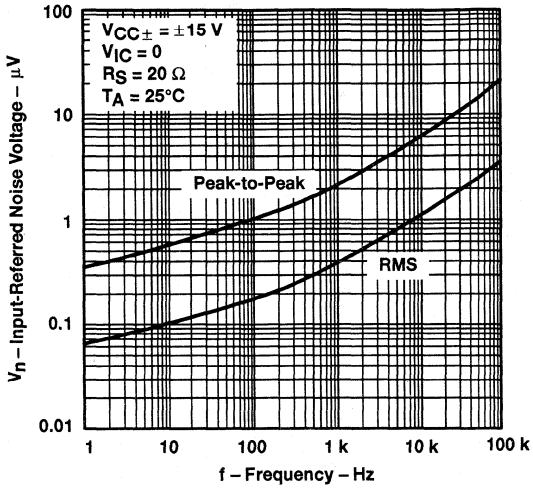


Figure 42

INPUT-REFERRED NOISE VOLTAGE
OVER A 10-SECOND TIME INTERVAL

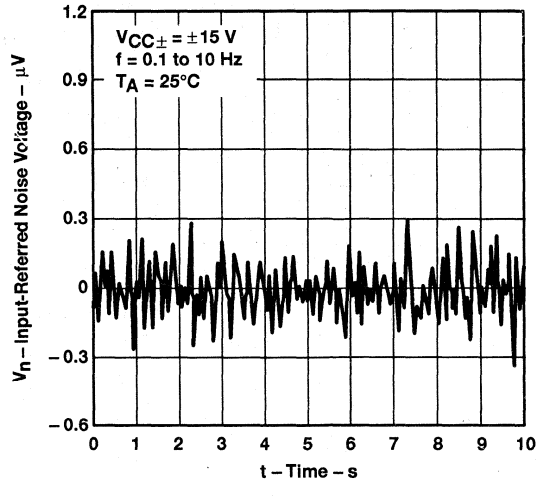


Figure 43

THIRD-OCTAVE SPECTRAL NOISE DENSITY
vs
FREQUENCY

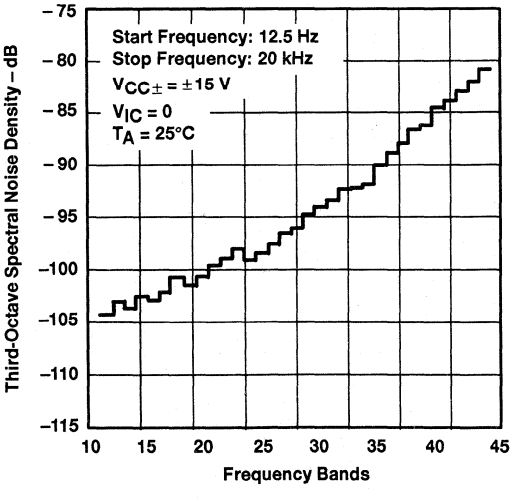


Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

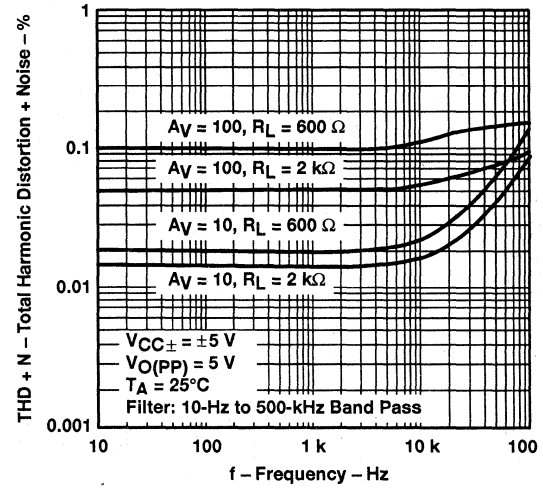


Figure 45

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

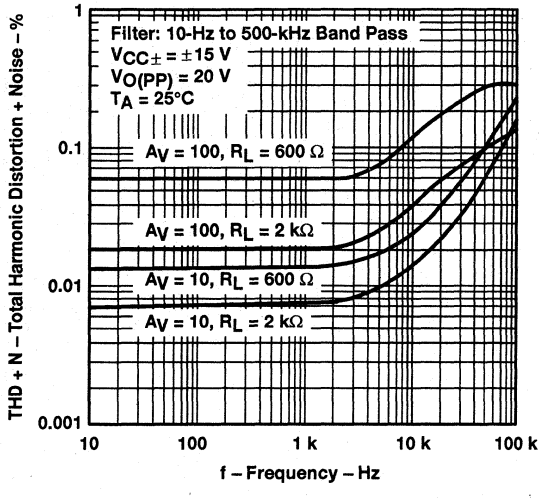


Figure 46

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

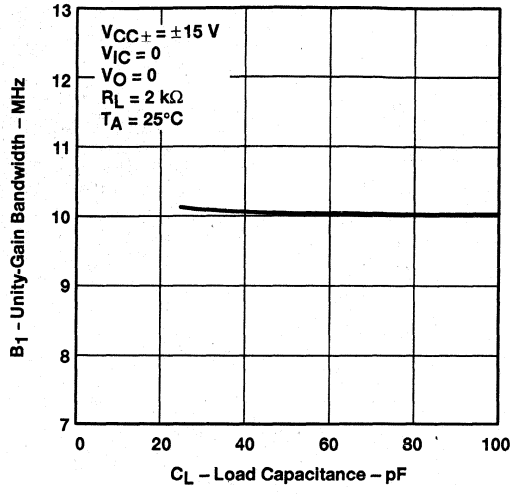


Figure 47

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

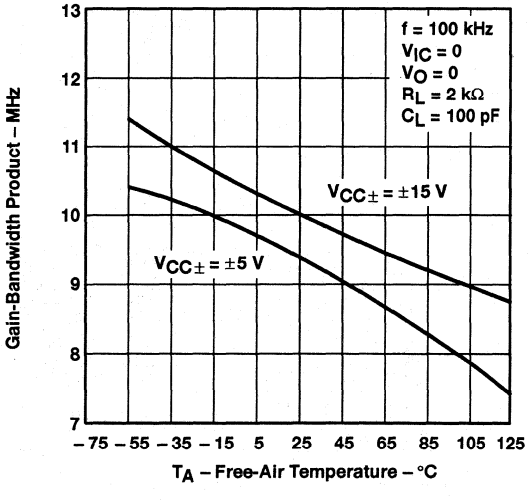


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

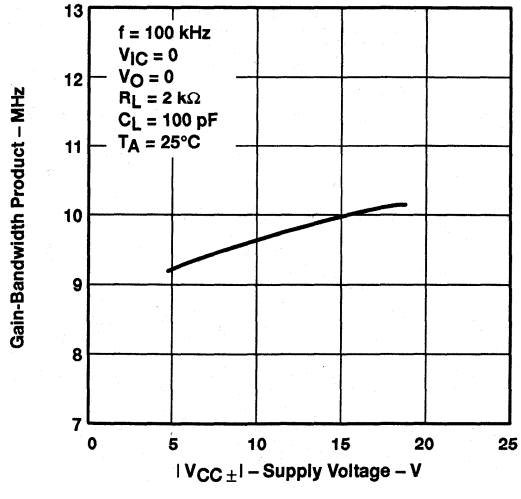


Figure 49

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

GAIN MARGIN vs LOAD CAPACITANCE

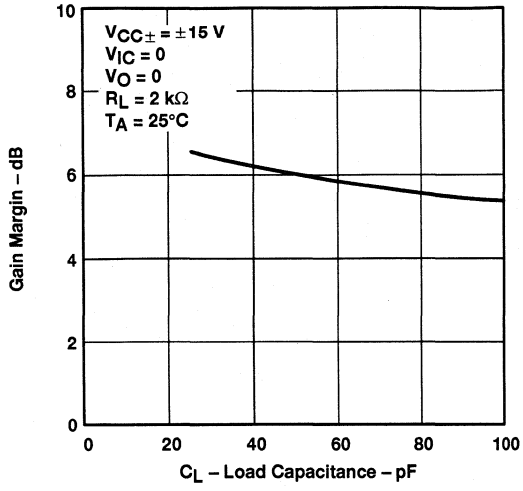


Figure 50

PHASE MARGIN vs FREE-AIR TEMPERATURE

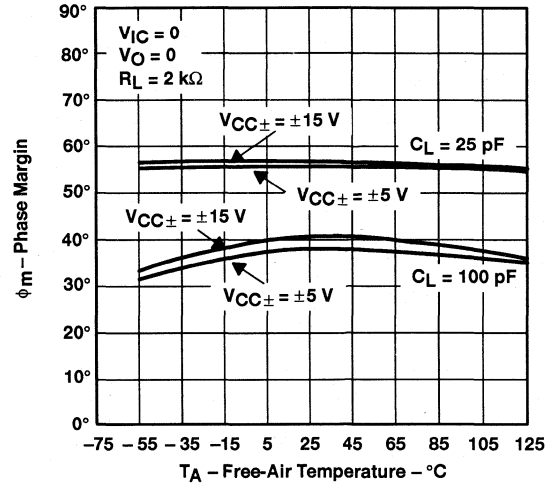


Figure 51

PHASE MARGIN vs SUPPLY VOLTAGE

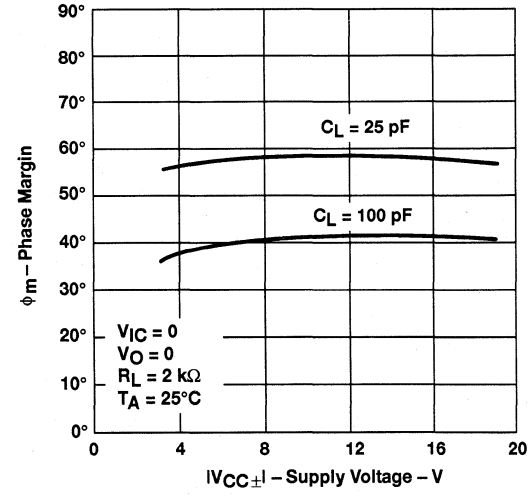


Figure 52

PHASE MARGIN vs LOAD CAPACITANCE

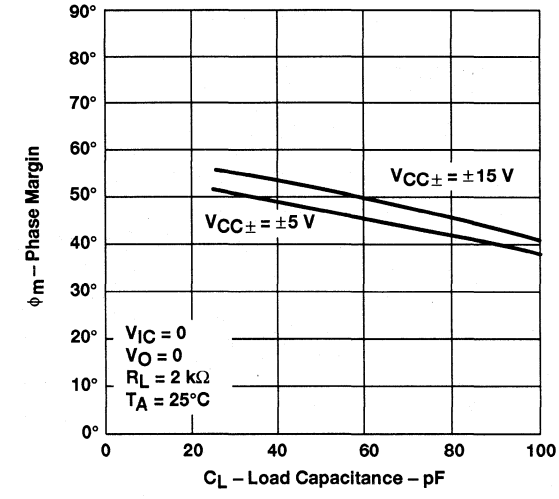


Figure 53

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

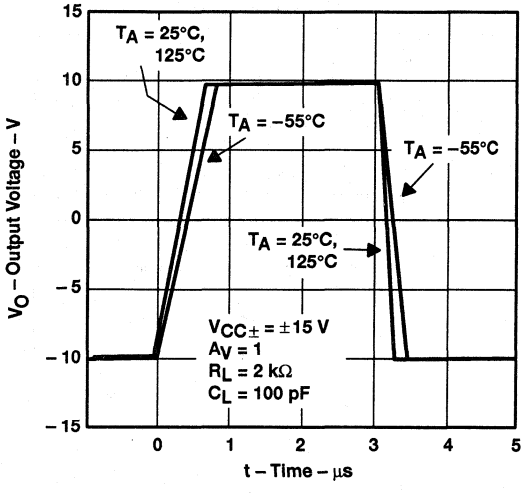


Figure 54

SMALL-SIGNAL PULSE RESPONSE

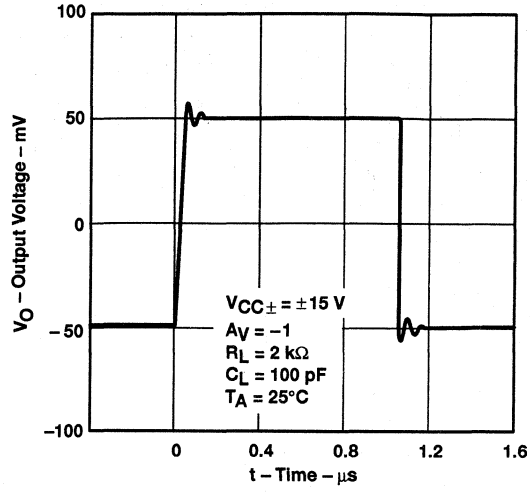


Figure 55

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

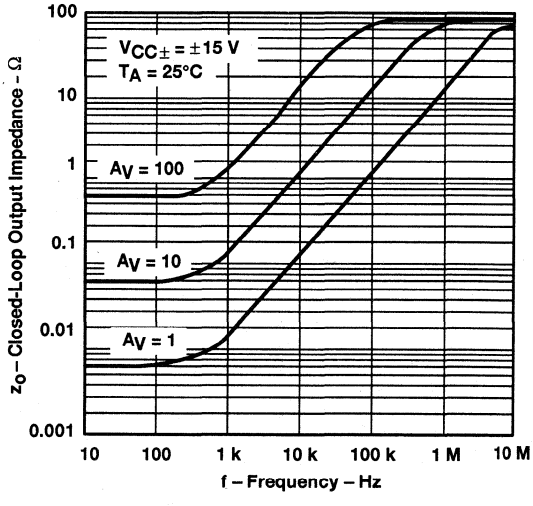


Figure 56

CROSSTALK ATTENUATION
vs
FREQUENCY

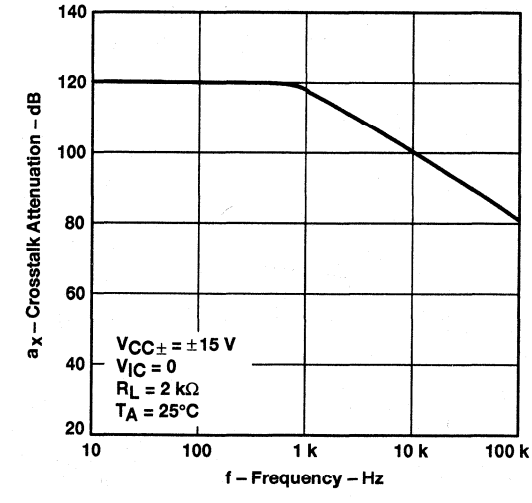


Figure 57

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

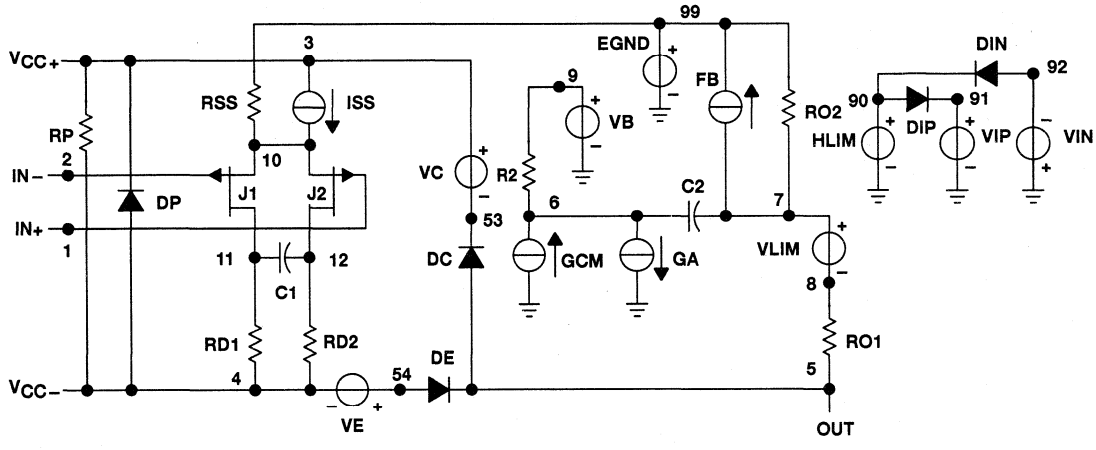
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 4) and subcircuit in Figure 58 were generated using the TLE2084 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G.R. Boyle, B.M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



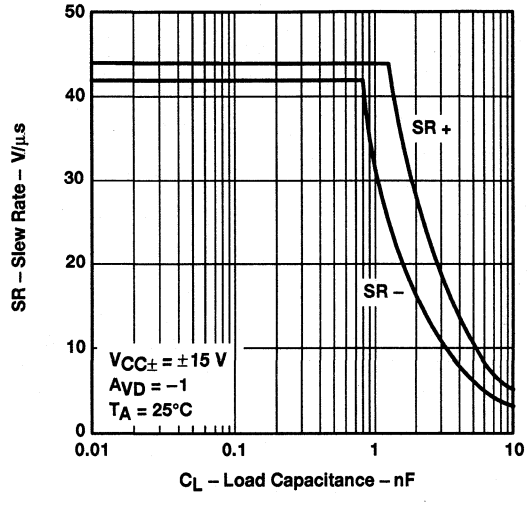

```
.SUBCKT TLE2084 1 2 3 4 5
C1      11      12      2.2E-12
C2      6       7       10.00E-12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,0) 0 .5
.5
FB      7       99      POLY (5) VB VC VE
VLP VLN 0
+ 5.607E6 –6E6 6E6 6E6 –6E6
GA      6       0       11 12 333.0E–6
GCM     0       6       10 99 7.43E–9
ISS     3       10      DC 400.0E–6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.0E3
RD1     4       11      3.003E3
RD2     4       12      3.003E3
RO1     8       5       80
RO2     7       99      80
RP      3       4       27.30E3
RSS     10      99      500.0E3
VB      9       0       DC 0
VC      3       53      DC 2.20
VE      54      4       DC 2.20
VLIM    7       8       DC 0
VLP     91      0       DC 45
VLN     0       92      DC 45
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=15.00E–12 BETA=554.5E–6
+ VTO=–.6)
.ENDS
```

Figure 58. Boyle Macromodel and Subcircuit

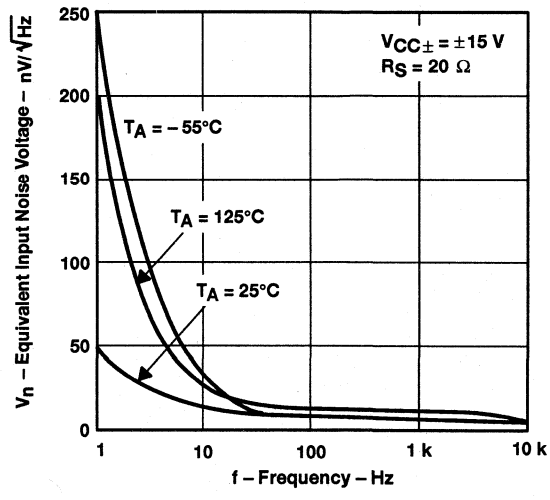
PSpice and *Parts* are trademarks of MicroSim Corporation.

- **Low Noise**
  10 Hz . . . 15 nV/√Hz
  1 kHz . . . 10.5 nV/√Hz
- **10000-pF Load Capability**
- **20-mA Min Short-Circuit Output Current**
- **27-V/μs Min Slew Rate**
- **High Gain-Bandwidth Product . . . 5.9 MHz**
- **Low V_{IO} . . . 500 μV Max at 25°C**
- **Single or Split Supply . . . 4 V to 44 V**
- **Fast Settling Time**
  340 ns to 0.1%
  400 ns to 0.01%
- **Saturation Recovery . . . 150 ns**
- **Large Output Swing**
  V_{CC-} +0.1 V to V_{CC+} – 1 V

SLEW RATE
vs
LOAD CAPACITANCE



EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



description

The TLE2141 and TLE2141A devices are high-performance, internally compensated operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2141A is a tighter offset voltage grade of the TLE2141. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	500 μV 900 μV	TLE2141ACD TLE2141CD	—	—	TLE2141ACP TLE2141CP	—
–40°C to 105°C	500 μV 900 μV	TLE2141AID TLE2141ID	—	—	TLE2141AIP TLE2141IP	TLE2141Y
–55°C to 125°C	500 μV 900 μV	TLE2141AMD TLE2141MD	TLE2141AMFK TLE2141MFK	TLE2141AMJG TLE2141MJB	TLE2141AMP TLE2141MP	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2141ACDR).

description (continued)

The design incorporates an input stage that simultaneously achieves low audio-band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2141 and TLE2141A are useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

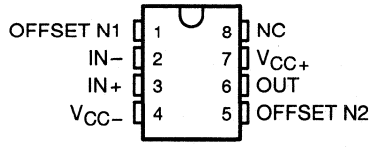
The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 500-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between $V_{CC-} - 0.3$ to $V_{CC+} - 1.8$ V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of $V_{CC-} - 0.1$ to $V_{CC+} - 1$ V under light current-loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

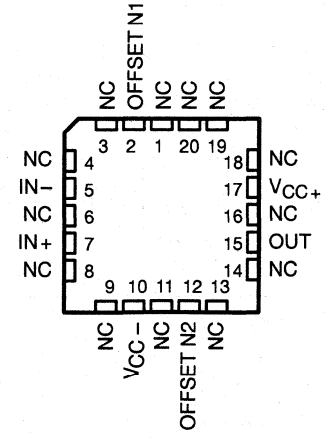
Both versions can also be used as comparators. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

Both the TLE2141 and TLE2141A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, I-suffix devices from –40°C to 105°C, and M-suffix devices over the full military temperature range of –55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

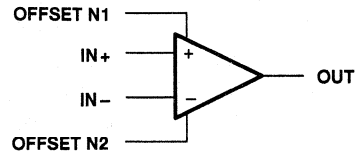


FK PACKAGE
(TOP VIEW)



NC – No internal connection

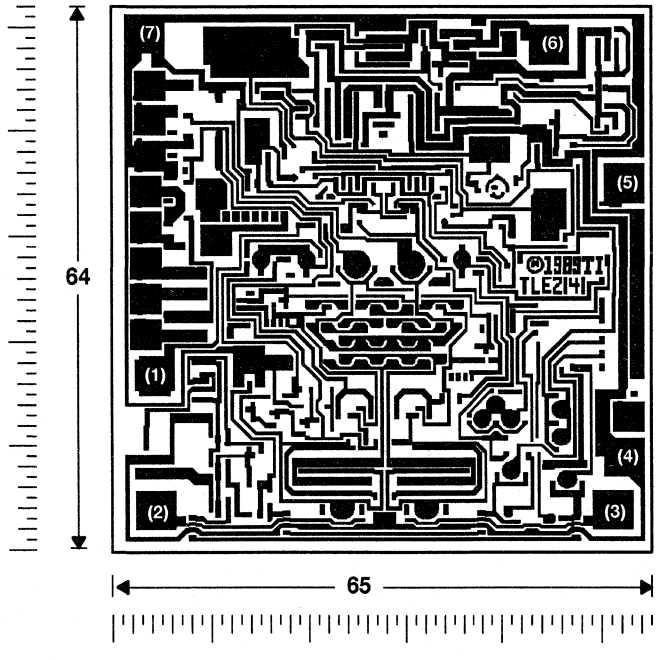
symbol

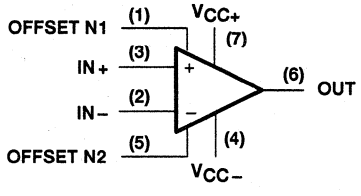


TLE2141Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2141. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

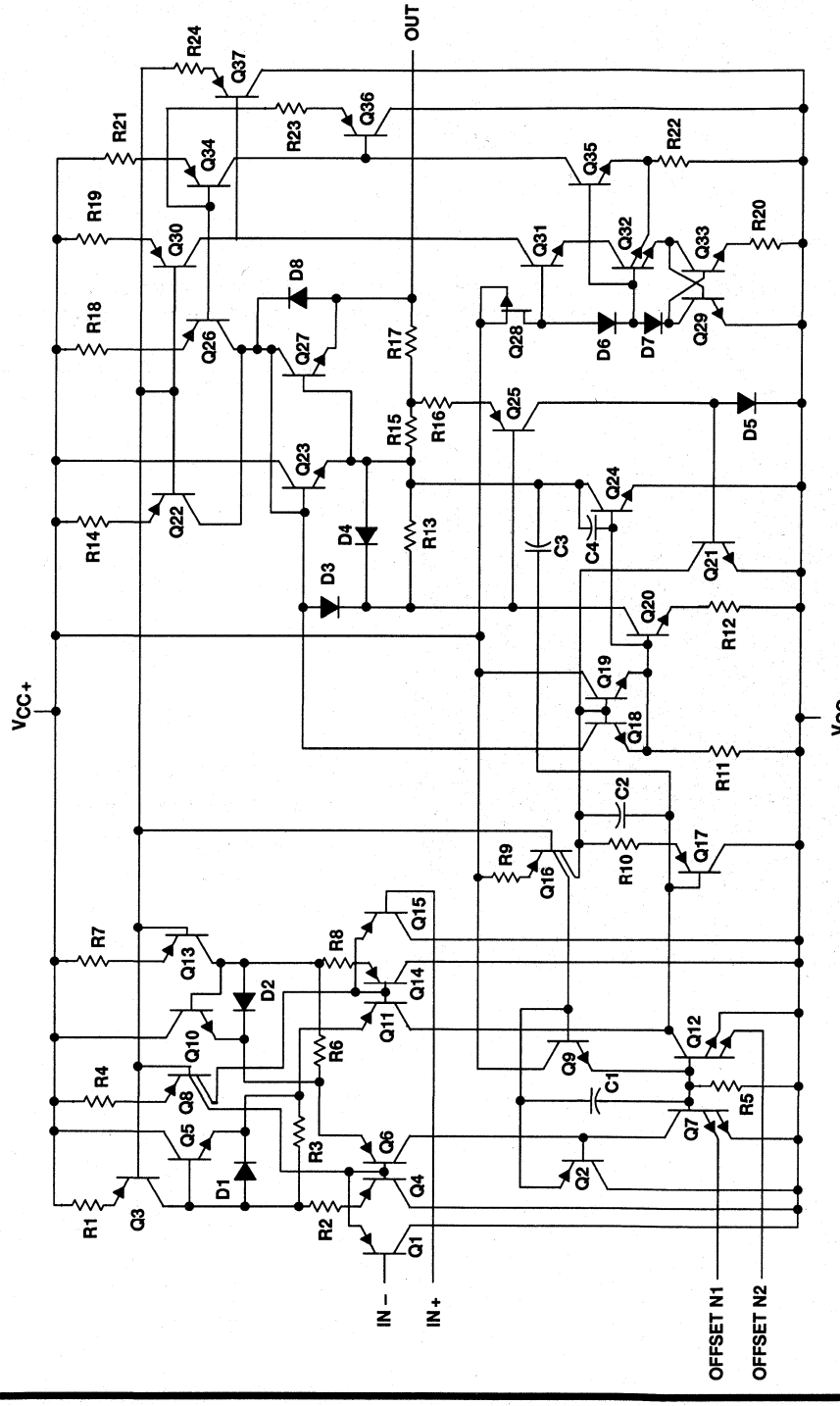
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic



COMPONENT COUNT (total device)	
Transistors	36
Epi-FET	1
Diodes	8
Resistors	24
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 22 V
Supply voltage, V_{CC-} ..... −22 V
Differential input voltage, V_{ID} (see Note 2) ..... ±44 V
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-} − 0.3 V
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±80 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 105°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if input is brought below V_{CC-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2	±22	±2	±22	±2	±22	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0	2.9	0	2.7	0	2.7	V
	$V_{CC\pm}$ = ±15 V	−15	12.9	−15	12.7	−15	12.7	
Operating free-air temperature, T_A		0	70	−40	105	−55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400		200	1000	μV
			Full range			1700			1300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.2	3.7		3.2	3.7		
			Full range	3.2			3.2			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.6		1.2	1.6	V
			Full range			1.7			1.7	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

† Full range is 0°C to 70°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS†		TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		57°			57°		

† R_L and C_L terminated to 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141C			TLE2141AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		200	900		175	500	µV
				Full range			1300			800	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			150			150	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	µA
				Full range			−1.6			−1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.9	−15.3 to 13.1		−15 to 12.9	−15.3 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −1.5 mA		25°C	13.7	14		13.7	14		
				Full range	13.6			13.6			
		I_O = −15 mA		25°C	13.1	13.7		13.1	13.7		
				Full range	13			13			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	−14.7	−14.9		−14.7	−14.9		V
				Full range	−14.6			−14.6			
		I_O = 1.5 mA		25°C	−14.5	−14.8		−14.5	−14.8		
				Full range	−14.4			−14.4			
		I_O = 15 mA		25°C	−13.4	−13.8		−13.4	−13.8		
				Full range	−13.3			−13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V		25°C	100	450		100	450		V/mV
				Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ		25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	

† Full range is 0°C to 70°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141I			TLE2141AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400		200	1000	μV
			Full range			1900			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.2			−2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.2	3.7		3.2	3.7		
		I_{OH} = −100 μA	Full range	3.8			3.8			
		I_{OH} = −1 mA		3.7			3.7			
		I_{OH} = −10 mA		3.3			3.3			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 μA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 μA	Full range			175			175	mV
		I_{OL} = 1 mA				225			225	
		I_{OL} = 10 mA				1.4			1.4	V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	10			10			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

† Full range is −40°C to 105°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS†		TLE2141I			TLE2141AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ,		45			45		V/μs
SR−	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = −1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		57°			57°		

† R_L and C_L terminated to 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141I			TLE2141AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	900		175	500	μV
				Full range			1500			1000	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.7			−1.7	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	100	450		100	450		V/mV
				Full range	40			40			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, No load		25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	

† Full range is −40°C to 105°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141I			TLE2141AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400		200	1000	μV
			Full range			2100			1700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.2	3.7		3.2	3.7		
		I_{OH} = −100 μA	Full range	3.75			3.75			
		I_{OH} = −1 mA		3.65			3.65			
		I_{OH} = −10 mA		3.25			3.25			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 μA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 μA	Full range			200			200	mV
		I_{OL} = 1 mA				250			225	
		I_{OL} = 10 mA				1.25			1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

† Full range is −55°C to 125°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS†		TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1	R_L = 2 kΩ,		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		57°			57°		

† R_L and C_L terminated to 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141M			TLE2141AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		200	900		175	500	µV
				Full range			1700			1200	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	µA
				Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 µA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 µA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	450		100	450		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V,	R_S = 50 Ω	25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, V_{IC} = 2.5 V	No load,	25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	

† Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 100 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2141Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω			200	1000	μV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	μA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		
		I_O = −15 mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		85	106		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−25	−50		mA
			V_{ID} = −1 V	20	31		
I_{CC}	Supply current	V_O = 0, No load			3.5	4.5	mA

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
V_{IO}	Input offset voltage		Distribution	1
I_{IO}	Input offset current		vs Free-air temperature	2
I_{IB}	Input bias current		vs Free-air temperature vs Common-mode input voltage	3 4
V_{OM+}	Maximum positive peak output voltage		vs Supply voltage vs Free-air temperature vs Output current vs Settling time	5 6 7 9
V_{OM-}	Maximum negative peak output voltage		vs Supply voltage vs Free-air temperature vs Output current vs Settling time	5 6 8 9
$V_{O(PP)}$	Maximum peak-to-peak output voltage		vs Frequency	10
V_{OH}	High-level output voltage		vs Output current	11
V_{OL}	Low-level output voltage		vs Output current	12
A_{VD}	Large-signal differential voltage amplification		vs Free-air temperature vs Frequency	13 14
z_o	Closed loop output impedance		vs Frequency	15
I_{OS}	Short-circuit output current		vs Free-air temperature	16
CMRR	Common-mode rejection ratio		vs Frequency vs Free-air temperature	17 18
k_{SVR}	Supply-voltage rejection ratio		vs Frequency vs Free-air temperature	19 20
I_{CC}	Supply current		vs Free-air temperature vs Supply voltage	21 22
V_N	Noise voltage		vs Frequency	23
V_N	Noise voltage		Over a 10-second period	24
I_n	Noise current		vs Frequency	25
THD + N	Total harmonic distortion plus noise		vs Frequency	26
SR	Slew rate		vs Free-air temperature vs Load capacitance	27 28
	Pulse response	Noninverting large signal	vs Time	29
		Inverting large signal	vs Time	30
		Small signal	vs Time	31
B_1	Unity-gain bandwidth		vs Load capacitance	32
	Gain margin		vs Load capacitance	33
ϕ_m	Phase margin		vs Load capacitance	34
	Phase shift		vs Frequency	14

TYPICAL CHARACTERISTICS†

TLE2141
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

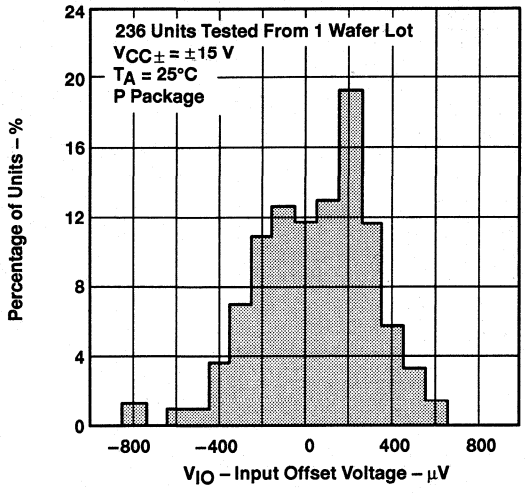


Figure 1

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

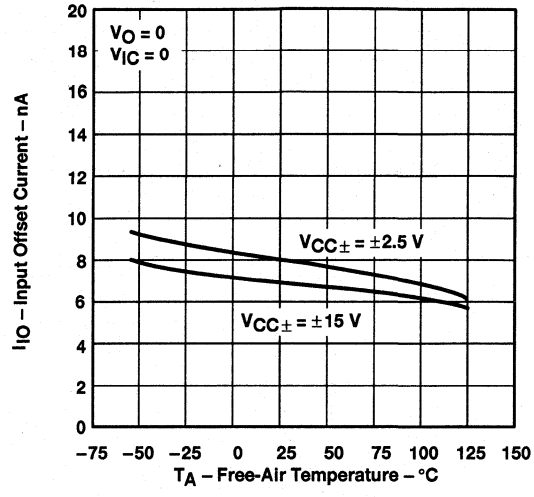


Figure 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

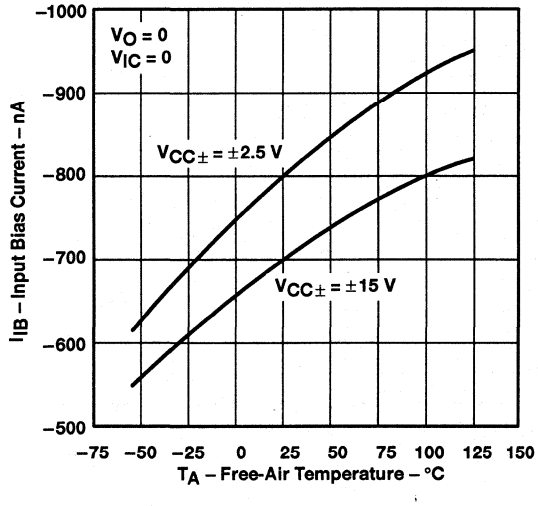


Figure 3

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

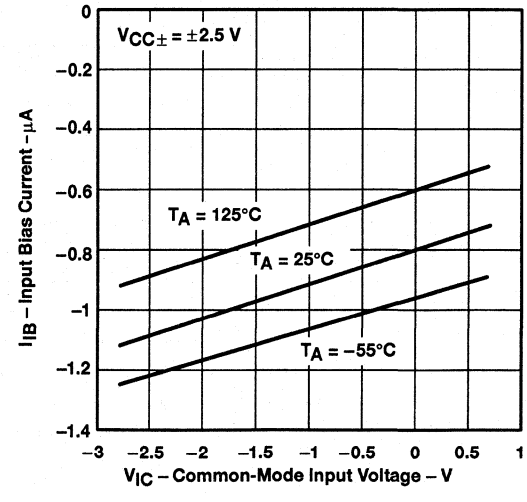


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

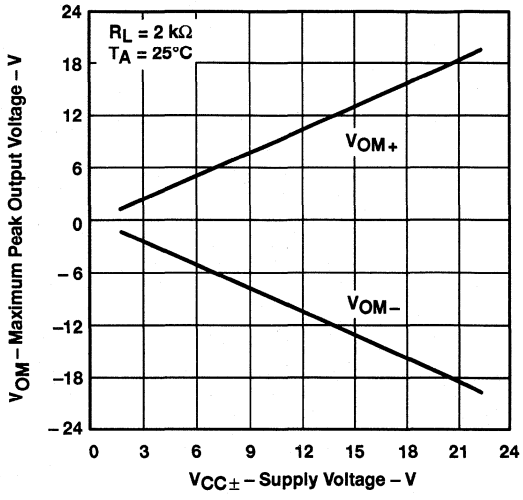


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

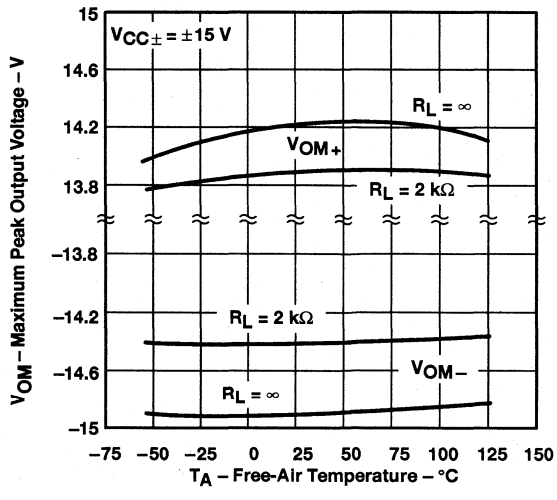


Figure 6

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

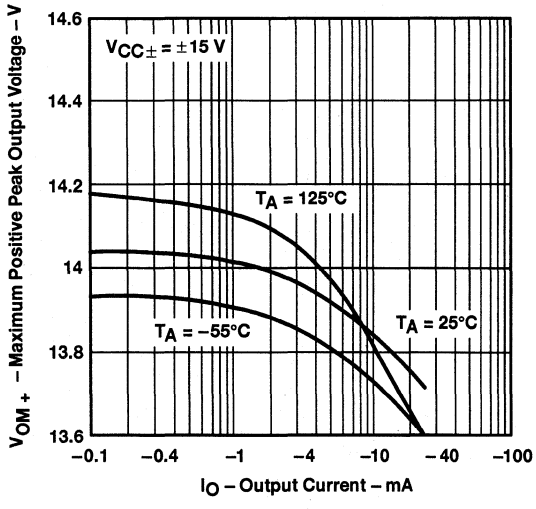


Figure 7

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

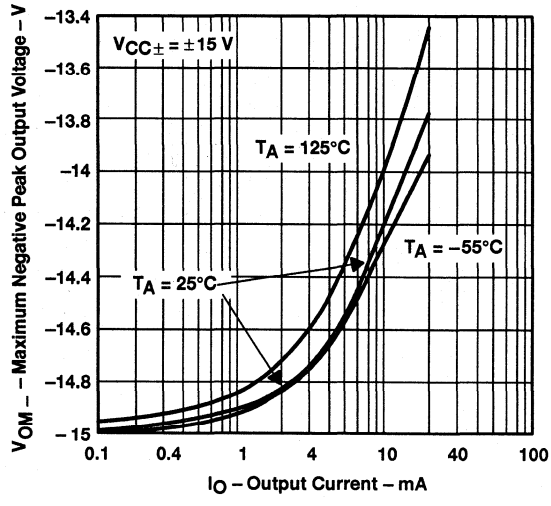


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SETTLING TIME

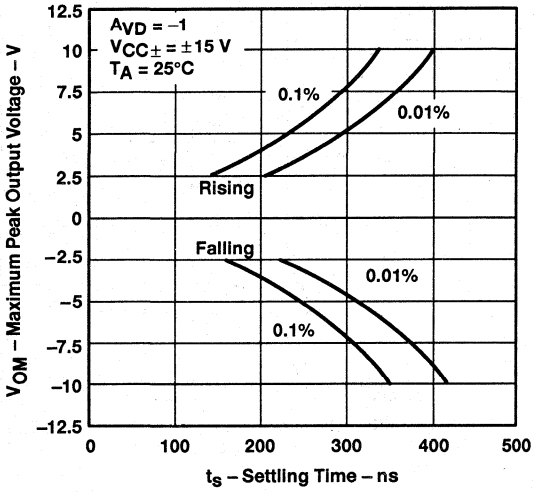


Figure 9

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

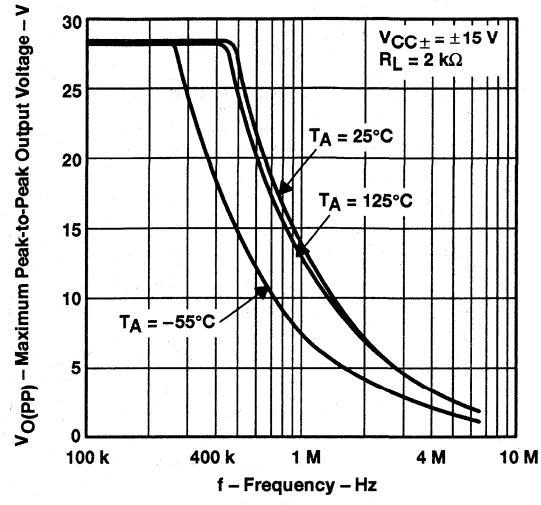


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

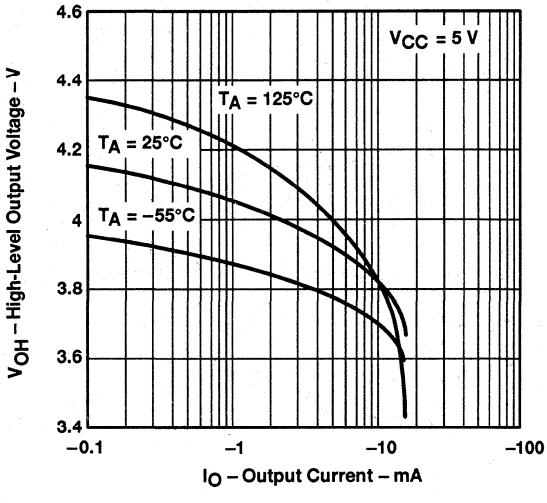


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

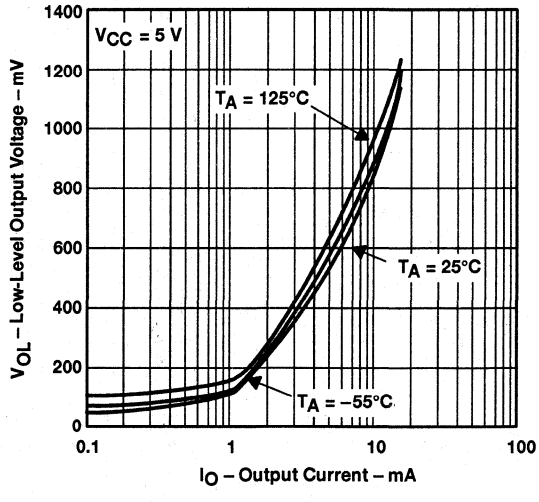


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

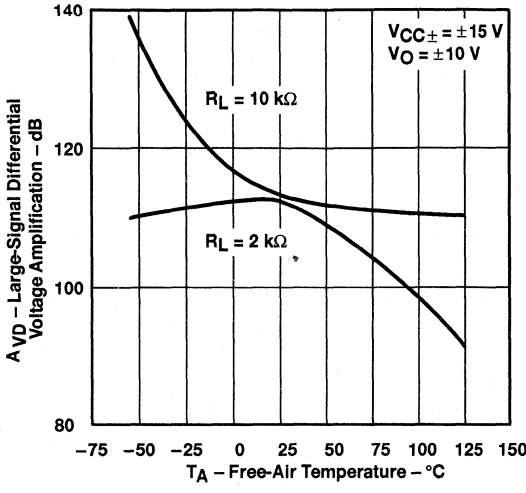


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

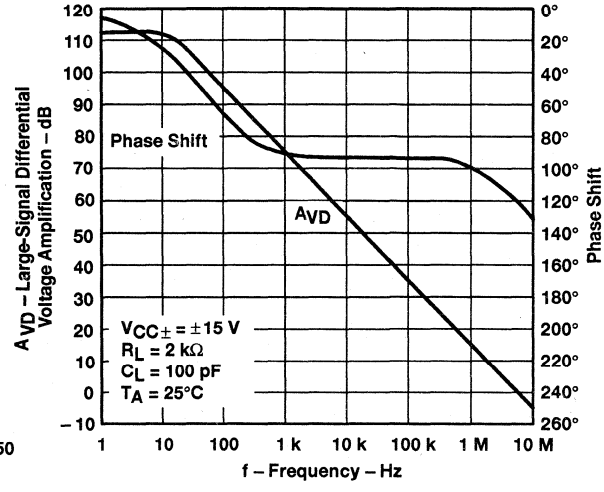


Figure 14

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

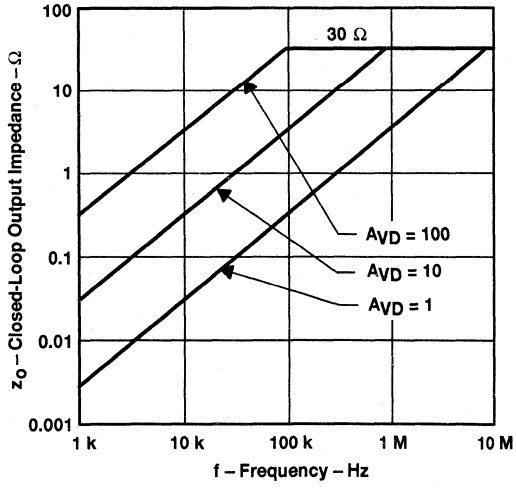


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

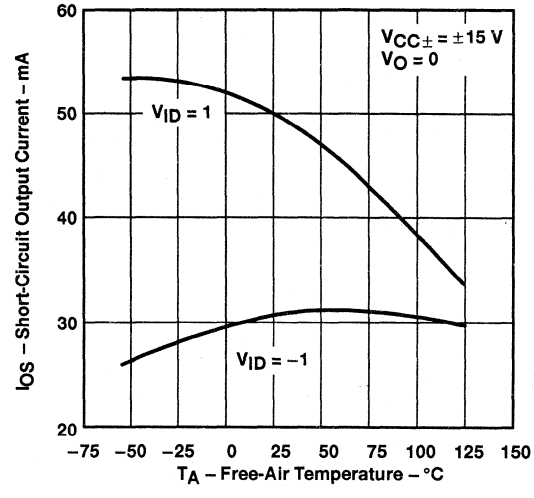


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

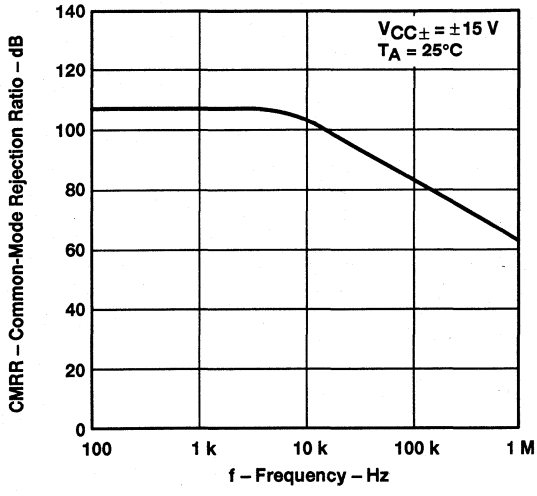


Figure 17

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

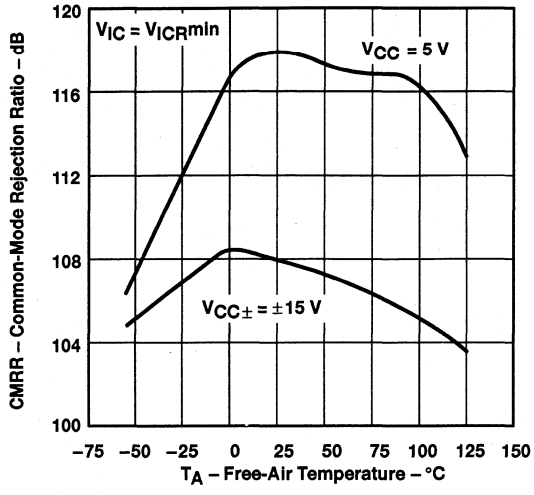


Figure 18

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

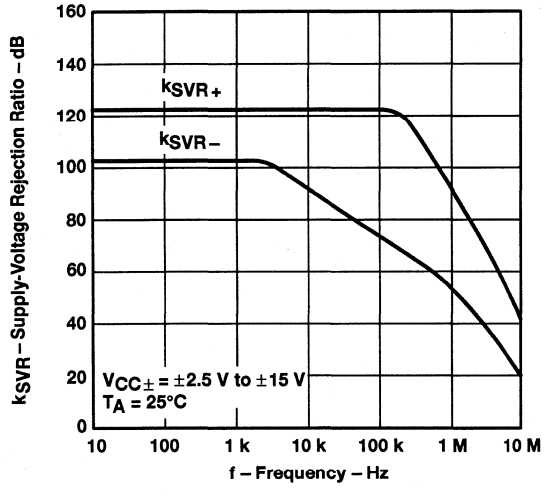


Figure 19

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

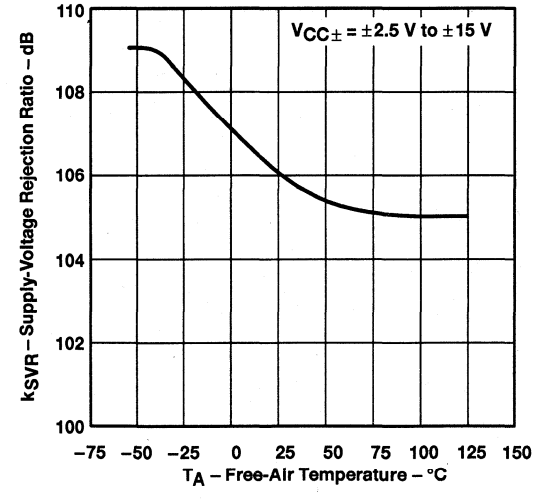


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

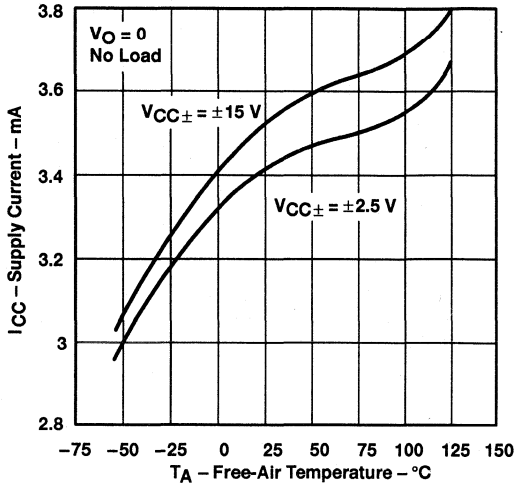


Figure 21

SUPPLY CURRENT vs SUPPLY VOLTAGE

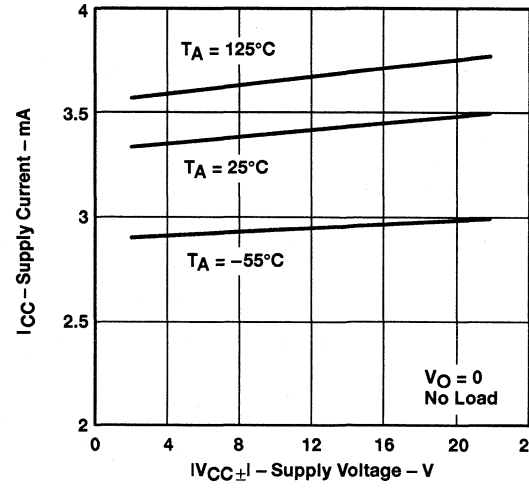


Figure 22

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

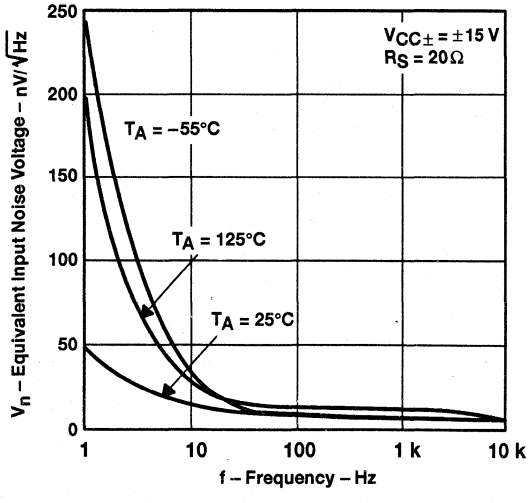


Figure 23

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

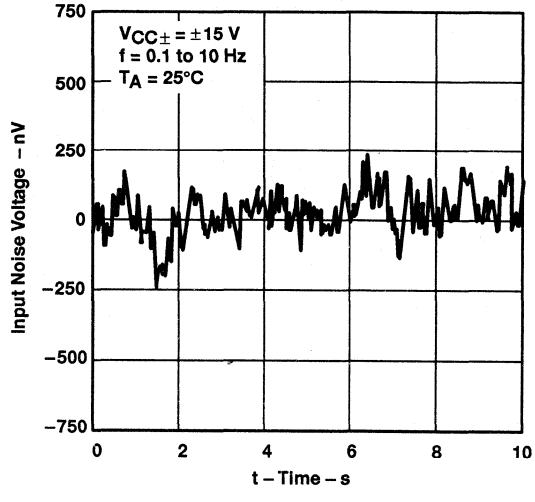


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NOISE CURRENT
vs
FREQUENCY

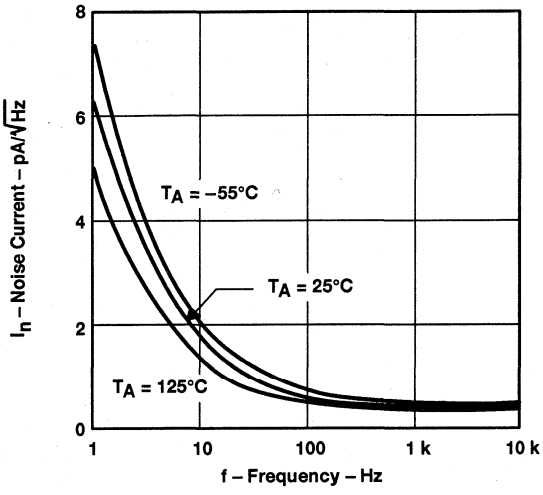


Figure 25

TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
FREQUENCY

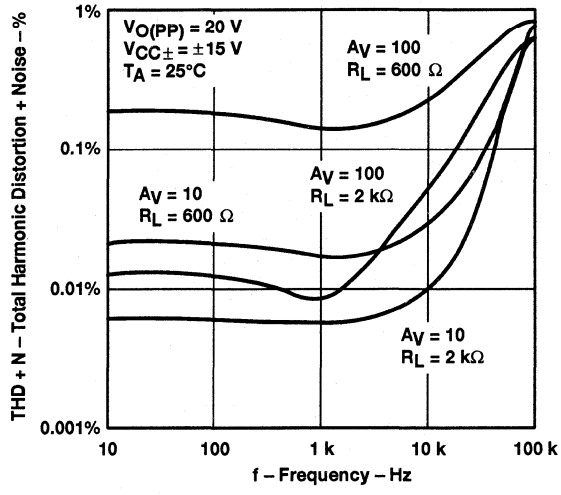


Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

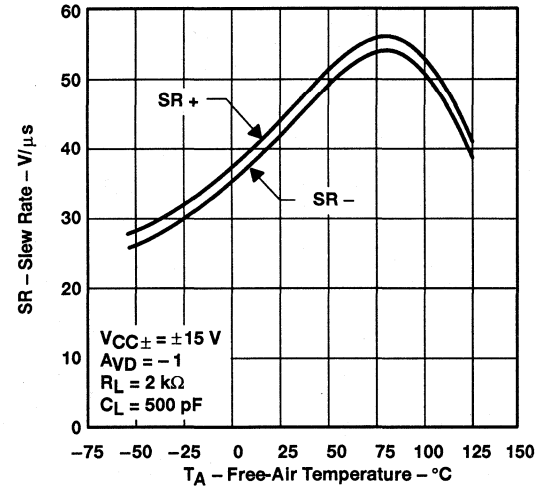


Figure 27

SLEW RATE
vs
LOAD CAPACITANCE

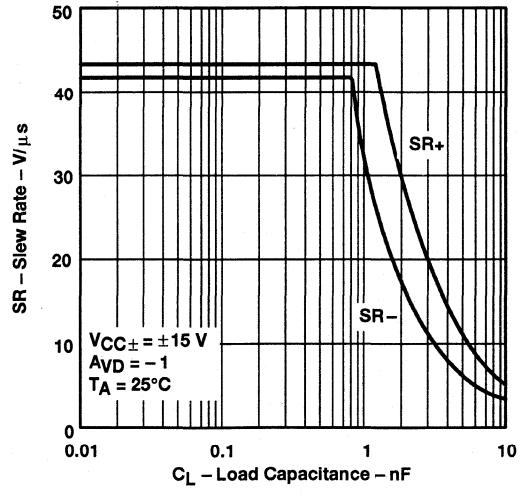


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NONINVERTING
LARGE-SIGNAL
PULSE RESPONSE

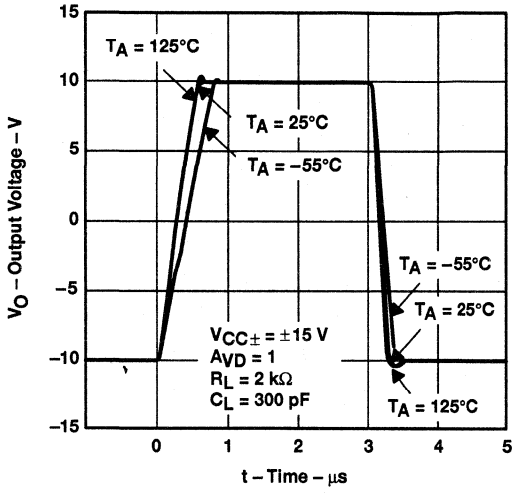


Figure 29

INVERTING
LARGE-SIGNAL
PULSE RESPONSE

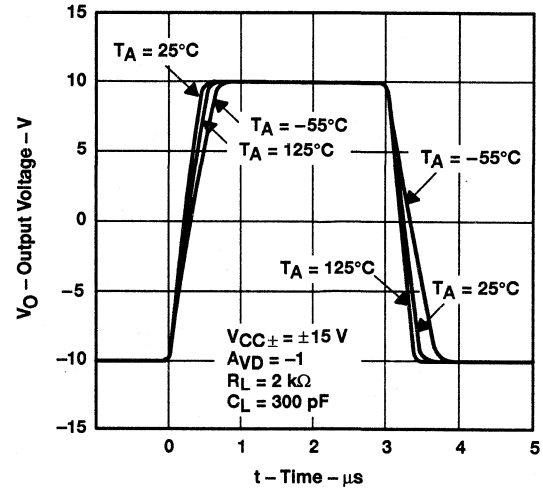


Figure 30

SMALL-SIGNAL
PULSE RESPONSE

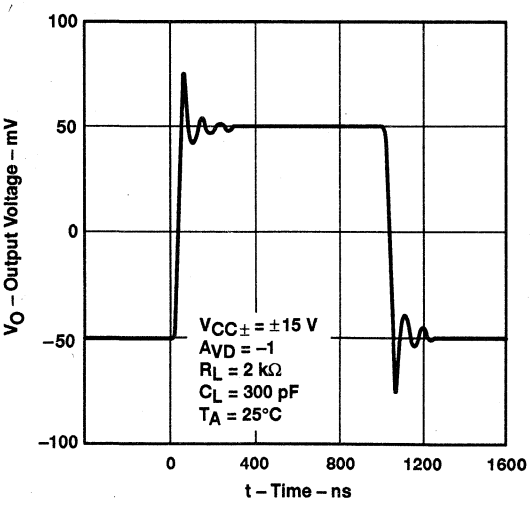


Figure 31

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

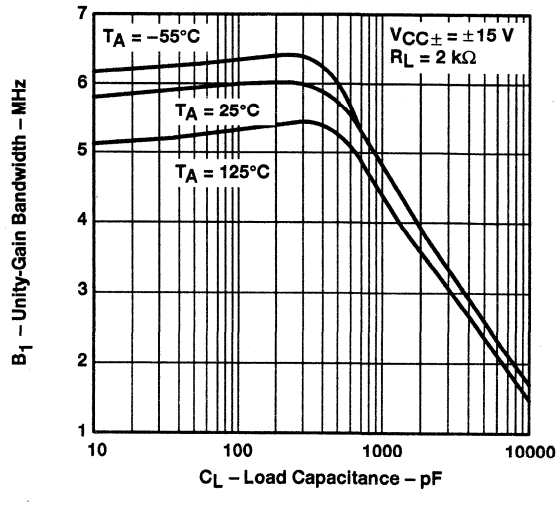


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

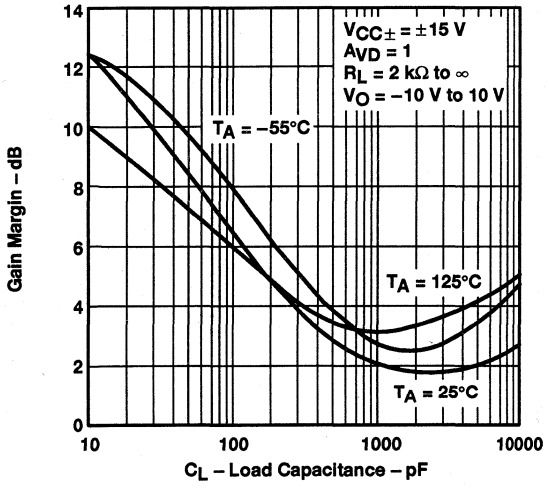


Figure 33

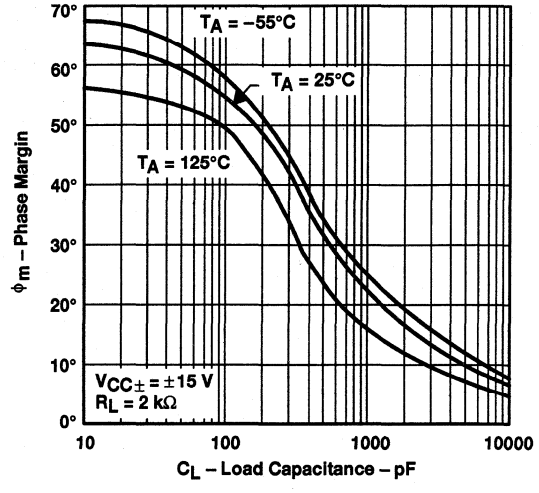


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input offset voltage nulling

The TLE2141 series offers external null pins that can be used to further reduce the input offset voltage. If this feature is desired, connect the circuit of Figure 35 as shown. If external nulling is not needed, the null pins may be left unconnected.

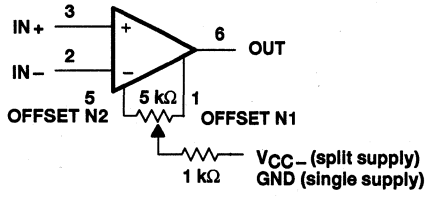
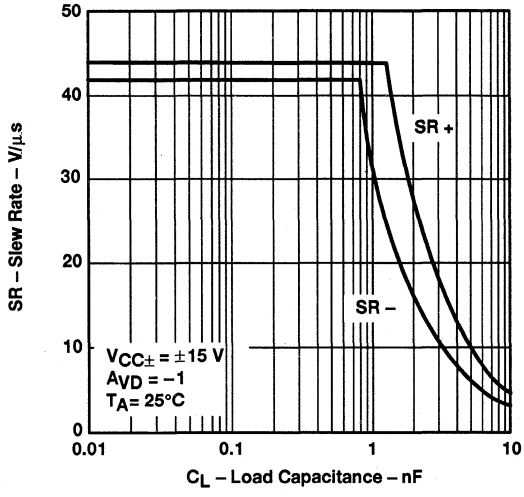


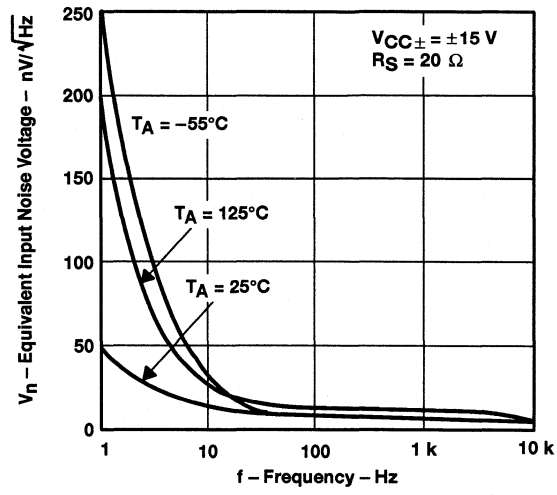
Figure 35. Input Offset Voltage Null Circuit

- **Low Noise**
  10 Hz . . . 15 nV/√Hz
  1 kHz . . . 10.5 nV/√Hz
- **10000-pF Load Capability**
- **20-mA Min Short-Circuit Output Current**
- **27-V/μs Min Slew Rate**
- **High Gain-Bandwidth Product . . . 5.9 MHz**
- **Low V_{IO} . . . 750 μV Max at 25°C**
- **Single or Split Supply**
- **Fast Settling Time**
  340 ns to 0.1%
  400 ns to 0.01%
- **Saturation Recovery . . . 150 ns**
- **Large Output Swing**
  V_{CC-} +0.1 V to V_{CC+} – 1 V

SLEW RATE vs LOAD CAPACITANCE



EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY



description

The TLE2142 and TLE2142A devices are high-performance internally-compensated operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2142A is a tighter offset voltage grade of the TLE2142. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

PACKAGED DEVICES						CHIP FORM (Y)
T_A	V_{IO}max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	
0°C to 70°C	750 μV	TLE2142ACD	—	—	TLE2142ACP	—
	1200 μV	TLE2142CD	—	—	TLE2142CP	
–40°C to 105°C	750 μV	TLE2142AID	—	—	TLC2142AIP	TLE2142Y
	1200 μV	TLE2142ID	—	—	TLC2142IP	
–55°C to 125°C	750 μV	TLE2142AMD	TLE2142AMFK	TLE2142AMJG	TLC2142AMP	—
	1200 μV	TLE2142MD	TLE2142MFK	TLE2142MJG	TLC2142MP	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2142ACDR).

description (continued)

The design incorporates a patent-pending input stage that simultaneously achieves low audio-band noise of 10.5 nV/$\sqrt{\text{Hz}}$, with a 6-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2142 and TLE2142A are useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

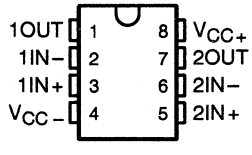
The special design also exhibits an improved insensitivity to inherit integrated circuit component mismatches as is evidenced by a 750-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between V_{CC-} −0.3 to V_{CC+} −1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of V_{CC-} +0.1 to V_{CC+} −1 V under light current-loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

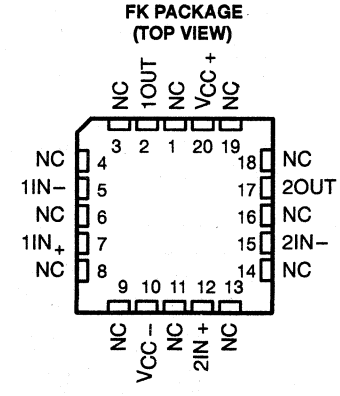
Both versions can also be used as comparators. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

Both the TLE2142 and TLE2142A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, I-suffix devices from −40°C to 105°C, and M-suffix devices over the full military temperature range of −55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

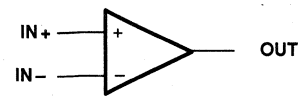


FK PACKAGE
(TOP VIEW)



NC – No internal connection

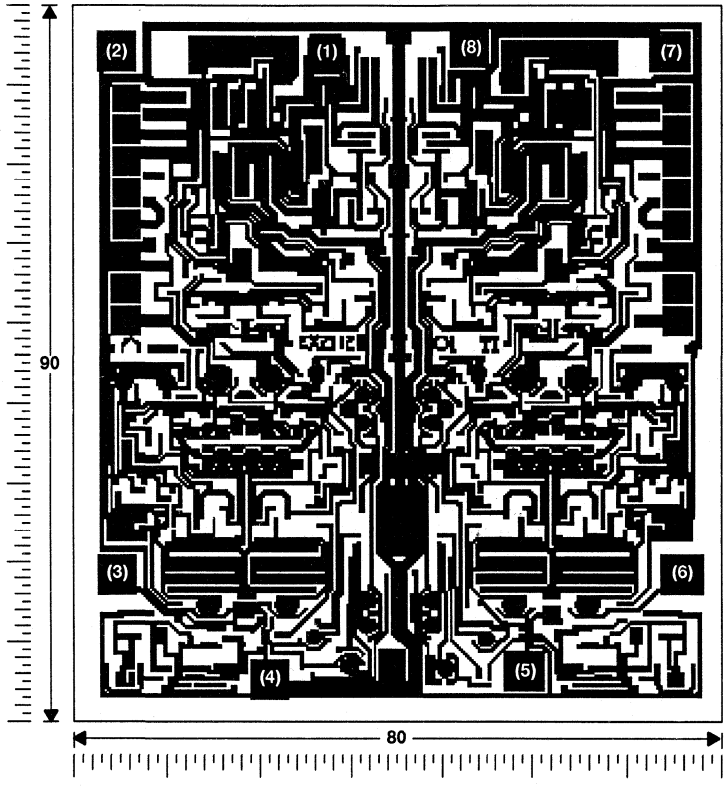
symbol (each amplifier)

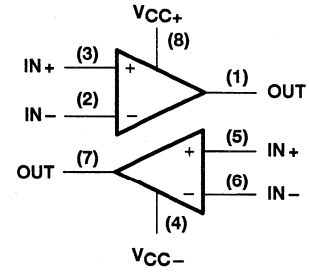


TLE2142Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2142. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

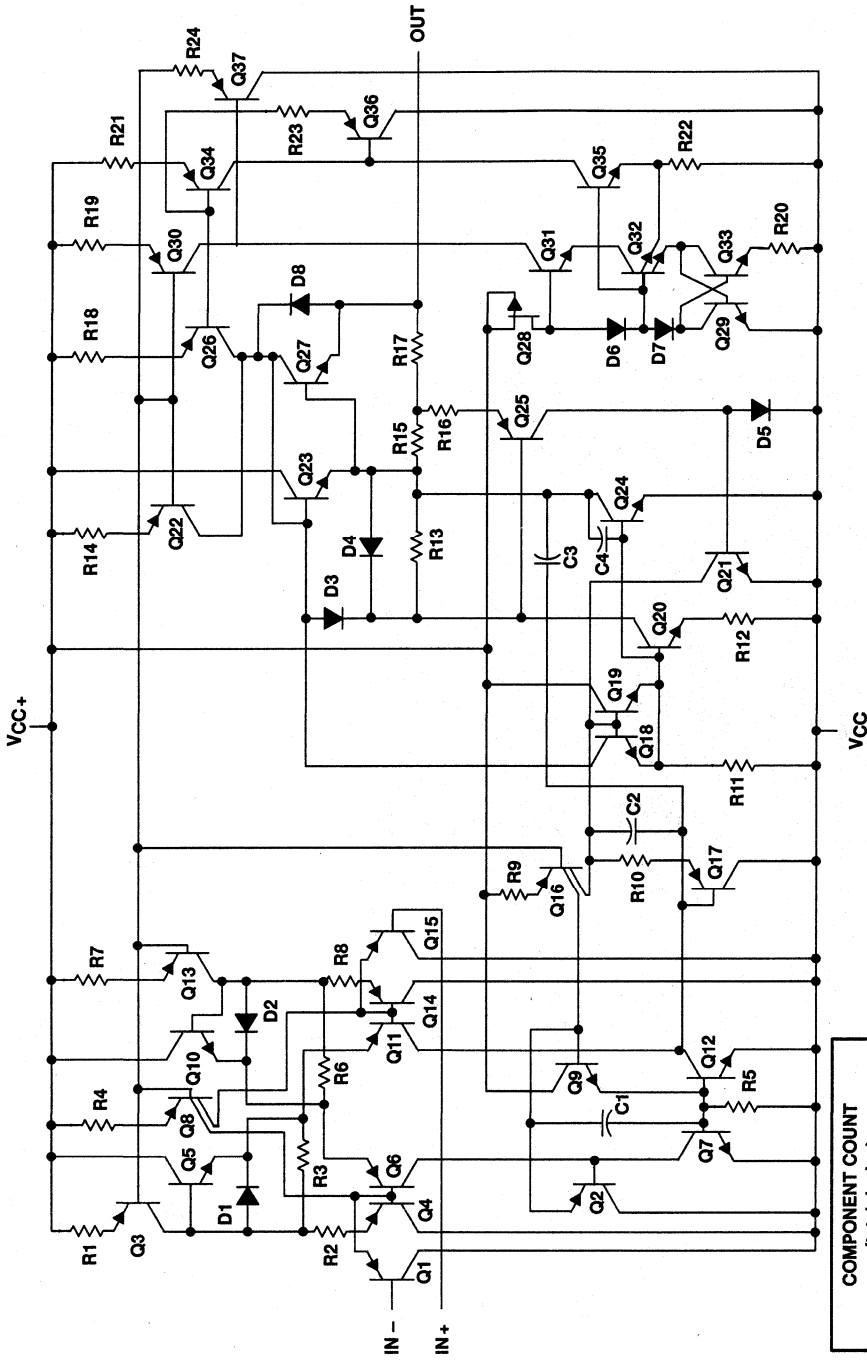
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN 4 IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (per amplifier)



COMPONENT COUNT (total device)	
Transistors	65
Epi-FET	1
Diodes	14
Resistors	43
Capacitors	8

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 22 V
Supply voltage, V_{CC-} ..... −22 V
Differential input voltage, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-} −0.3 V
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 105°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current will flow if input is brought below V_{CC-} −0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mV	5.8 mW/°C	464 mW	261 mW	145 mW
FK	1375 mV	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mV	8.4 mW/°C	672 mW	378 mW	210 mW
P	1000 mV	8.0 mW/°C	640 mW	360 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2	±22	±2	±22	±2	±22	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5$ V	0	2.9	0	2.7	0	2.7	V
	$V_{CC\pm} = \pm 15$ V	−15	12.9	−15	12.7	−15	12.7	
Operating free-air temperature, T_A		0	70	−40	105	−55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142C			TLE2142AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		200	1500	μV
			Full range			2200			1800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.4	3.7		3.4	3.7		
			Full range	3.4			3.4			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.4		1.2	1.4	V
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is 0°C to 70°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142C			TLE2142AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR−	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = −1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142C			TLE2142AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		290	1200		275	750	μV
				Full range			1600			1200	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			150			150	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.6			−1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.9	−15.3 to 13.1		−15 to 12.9	−15.3 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −1.5 mA		25°C	13.7	14		13.7	14		
				Full range	13.6			13.6			
		I_O = −15 mA		25°C	13.3	13.7		13.3	13.7		
				Full range	13.2			13.2			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
				Full range	−14.6			−14.6			
		I_O = 1.5 mA		25°C	−14.5	−14.8		−14.5	−14.8		
				Full range	−14.4			−14.4			
		I_O = 15 mA		25°C	−13.4	−13.8		−13.4	−13.8		
				Full range	−13.3			−13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V		25°C	100	450		100	450		V/mV
				Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ		25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		6.9	9		6.9	9	mA
				Full range			9.4			9.4	

† Full range is 0°C to 70°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142C			TLE2142AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		220	1500	µV
			Full range			2400			2000	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	µA
			Full range			−2.2			−2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 µA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 µA	Full range	3.8			3.8			
		I_{OH} = 1 mA		3.7			3.7			
		I_{OH} = 10 mA		3.5			3.5			
V_{OL}	Low-level output voltage	I_{OL} = 150 µA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 µA	Full range			175			175	mV
		I_{OL} = 1 mA				225			225	
		I_{OL} = 10 mA				1.2			1.2	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	10			10			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is – 40°C to 105°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142I			TLE2142I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		290	1200		275	750	μV
				Full range			1800			1400	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.7			−1.7	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.3	13.7		13.3	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.3			13.3			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	100	450		100	450		V/mV
				Full range	40			40			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C	85	108		85	108		dB
		R_S = 50 Ω		Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		6.9	9		6.9	9	mA
				Full range			9.4			9.4	

† Full range is −40°C to 105°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ,	30	45		30	45		V/μs
SR−	Negative slew rate			30	42		30	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f =100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		200	1500	μV
			Full range			2600			2200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.75			3.75			
		I_{OH} = 1 mA		3.65			3.65			
		I_{OH} = 10 mA		3.45			3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 μA	Full range			200			200	mV
		I_{OL} = 1 mA				250			250	
		I_{OL} = 10 mA				1.25			1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is – 55°C to 125°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR−	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = −1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142M			TLE2142AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		290	1200		275	750	μV
				Full range			2000			1600	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.3	13.7		13.3	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.3			13.3			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	450		100	450		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V,	R_S = 50 Ω	25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, V_{IC} = 2.5 V	No load,	25°C		6.9	9		6.9	9	mA
				Full range			9.4			9.4	

† Full range is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	R_L = 2 kΩ, C_L = 100 pF	A_{VD} = −1,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142Y MIN	TLE2142Y TYP	TLE2142Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω			150	875	μV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	μA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		
		I_O = −15 mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		85	106		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−25	−50		mA
			V_{ID} = −1 V	20	31		
I_{CC}	Supply current	V_O = 0, No load			6.9	9	mA

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS†

TLE2142
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

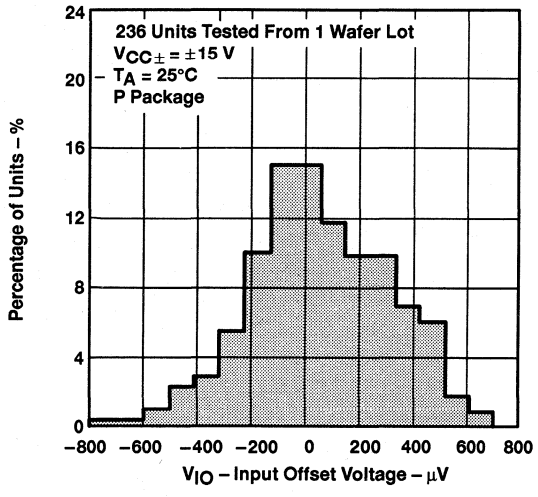


Figure 1

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

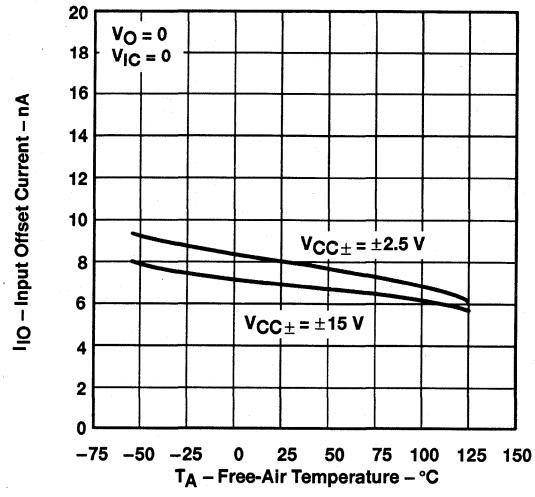


Figure 2

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

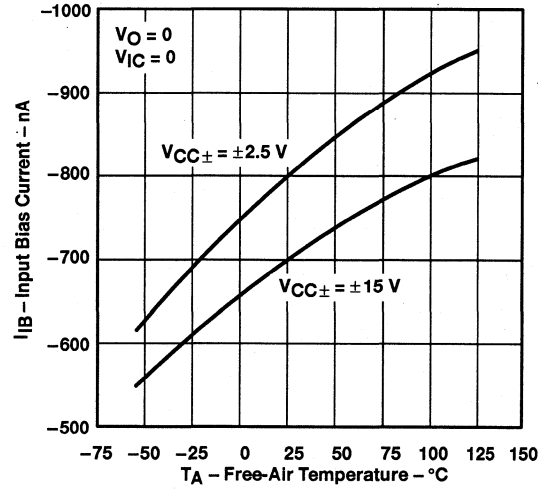


Figure 3

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

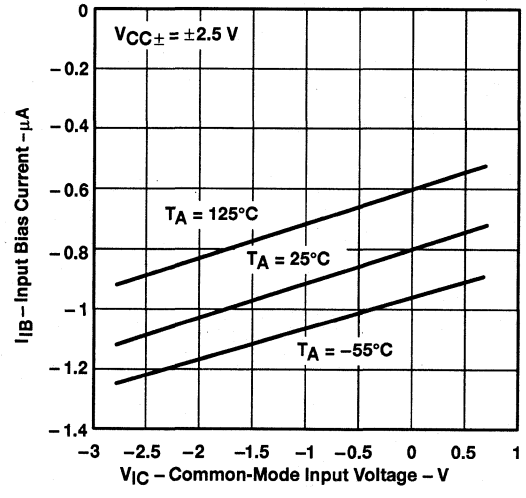


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

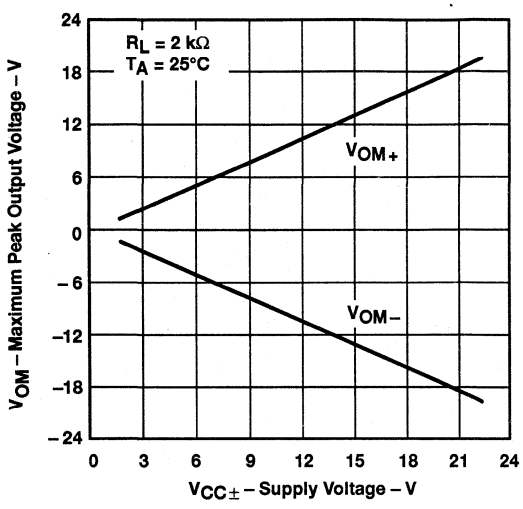


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

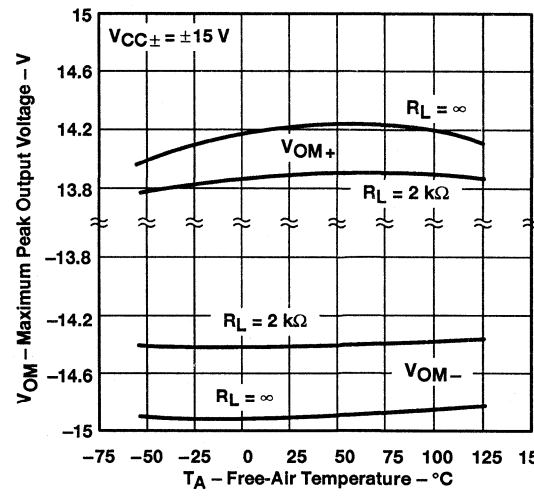


Figure 6

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

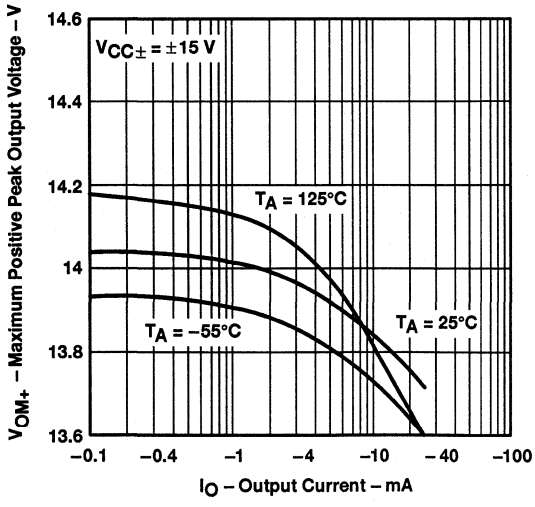


Figure 7

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

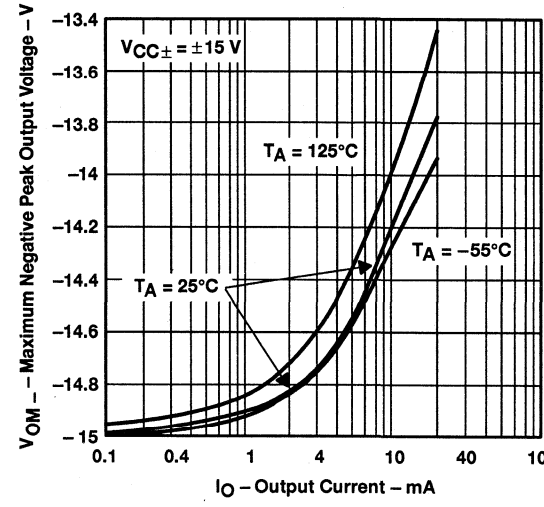


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SETTLING TIME

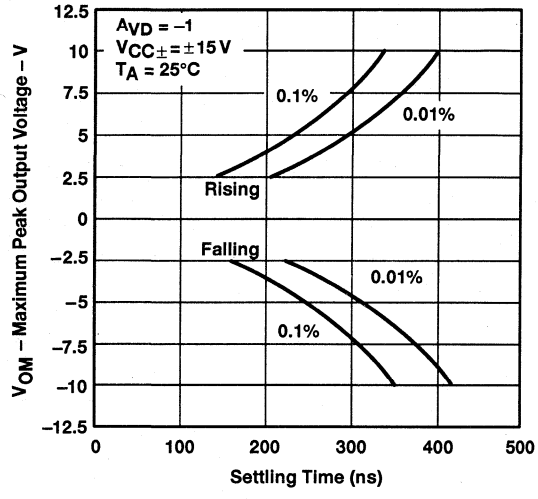


Figure 9

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

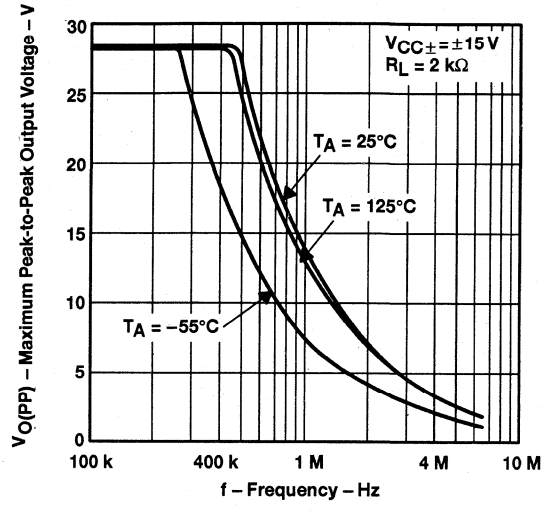


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

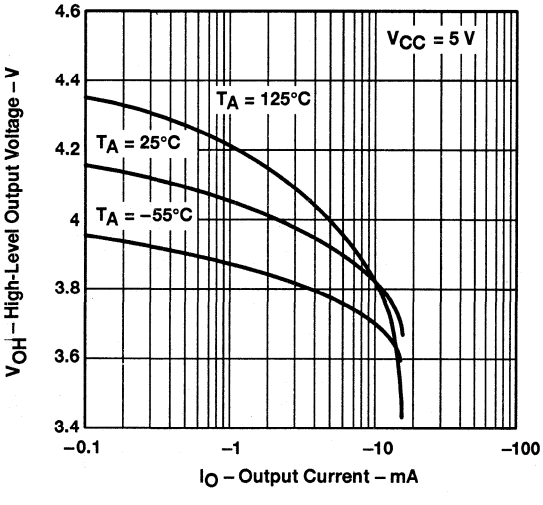


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

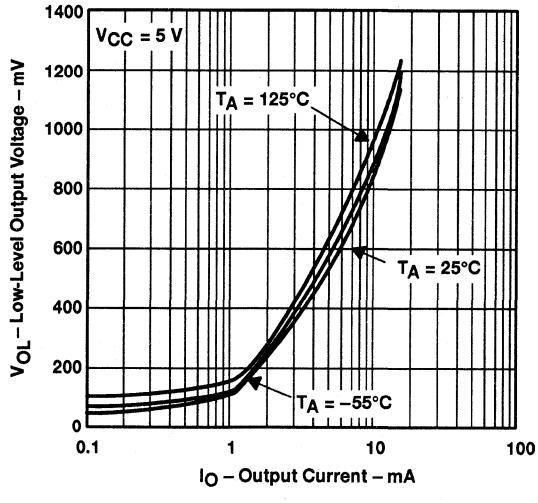


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

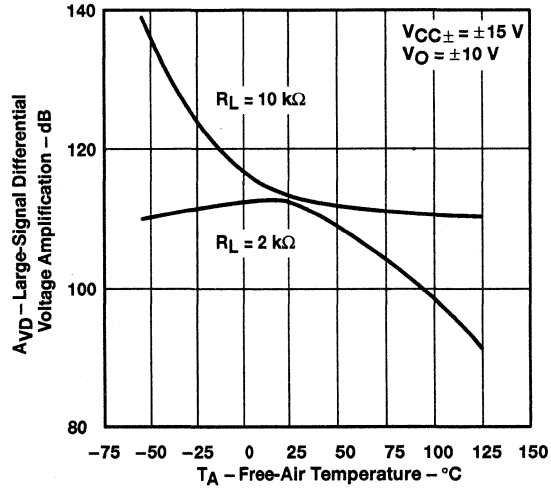


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

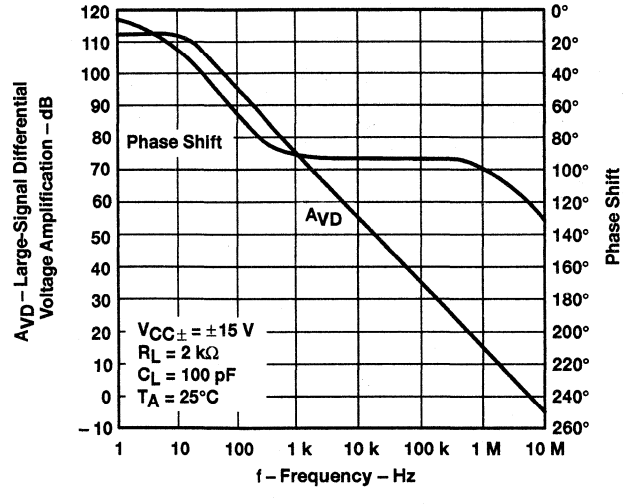


Figure 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

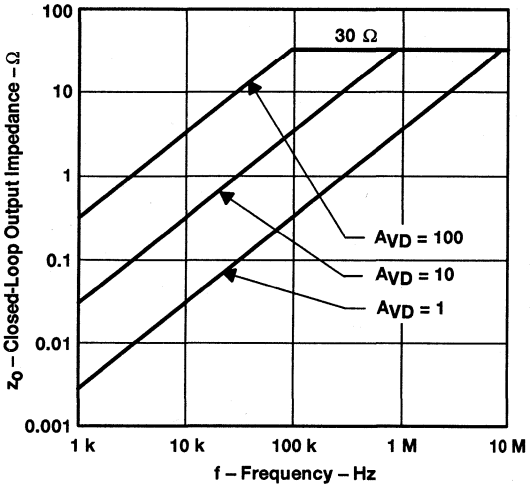


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

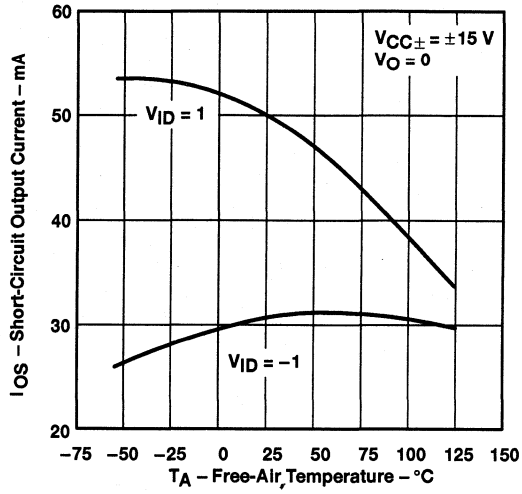


Figure 16

COMMON-MODE REJECTION RATIO vs FREQUENCY

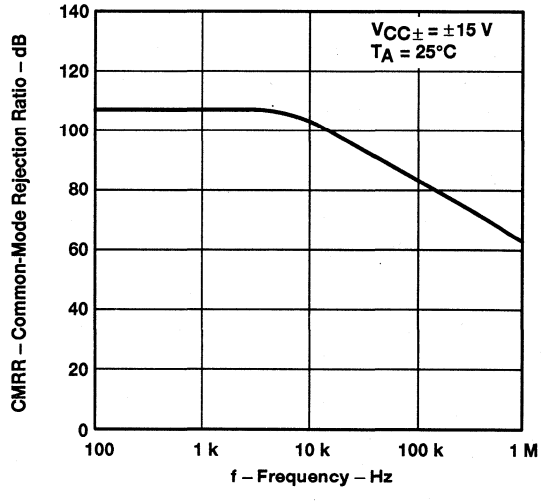


Figure 17

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

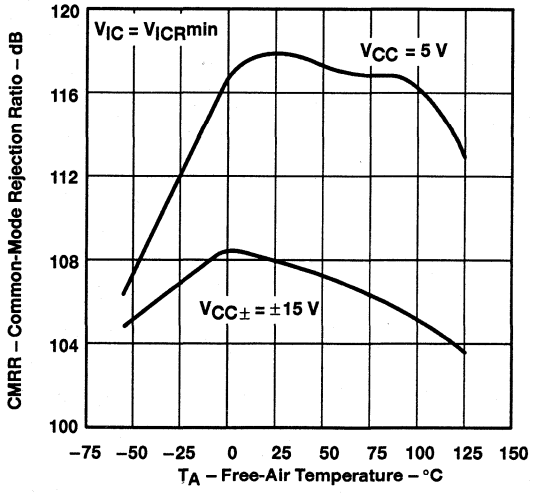


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

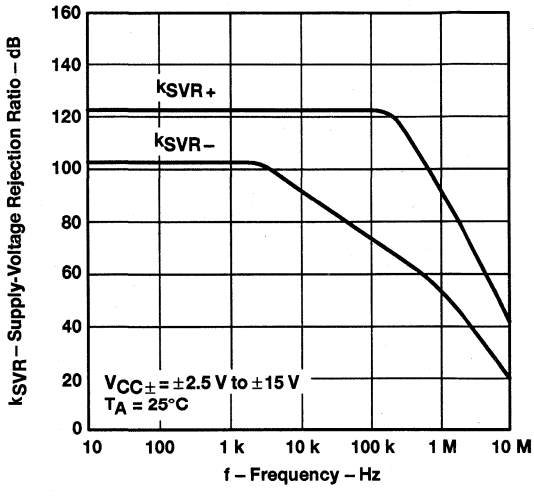


Figure 19

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

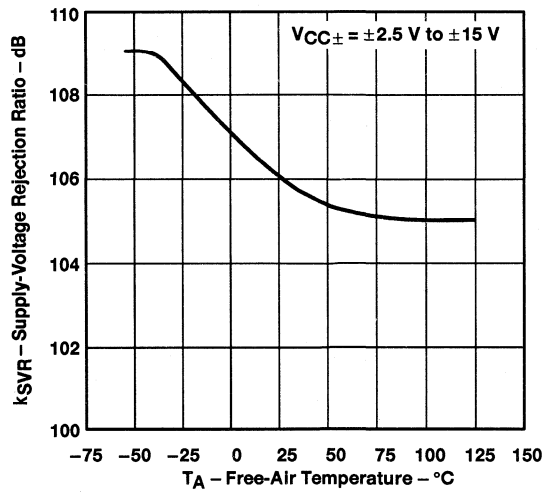


Figure 20

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

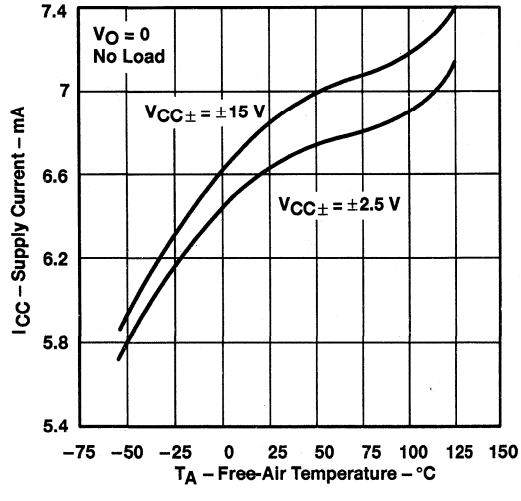


Figure 21

SUPPLY CURRENT vs SUPPLY VOLTAGE

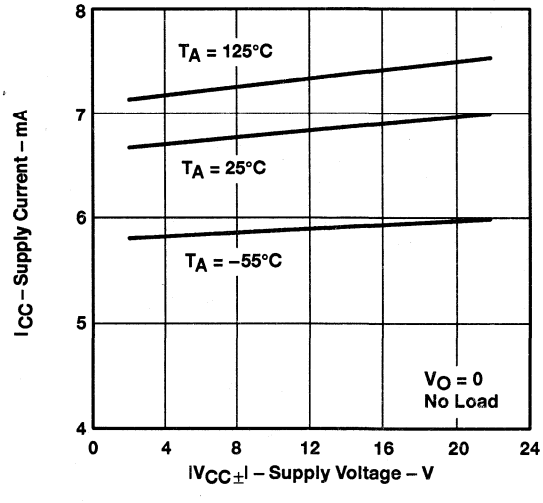


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

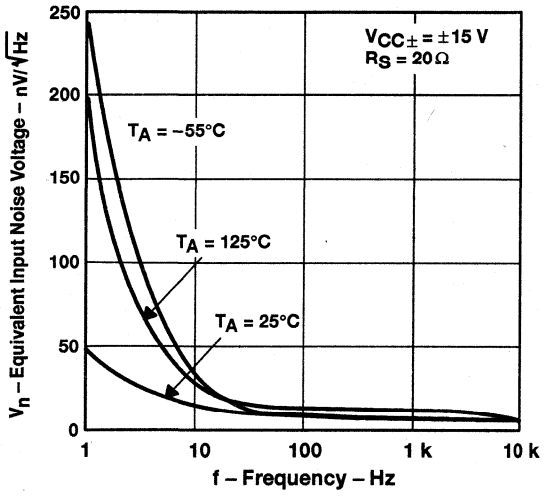


Figure 23

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

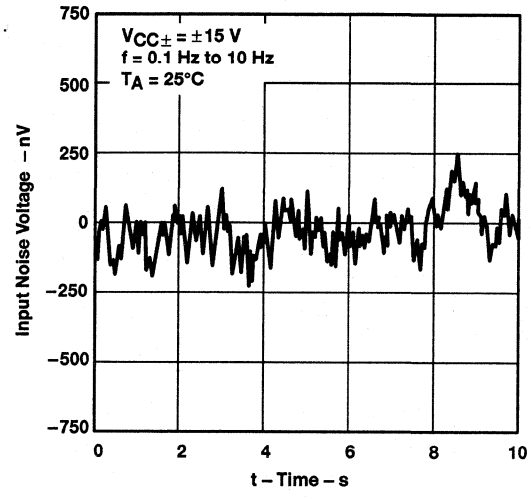


Figure 24

EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

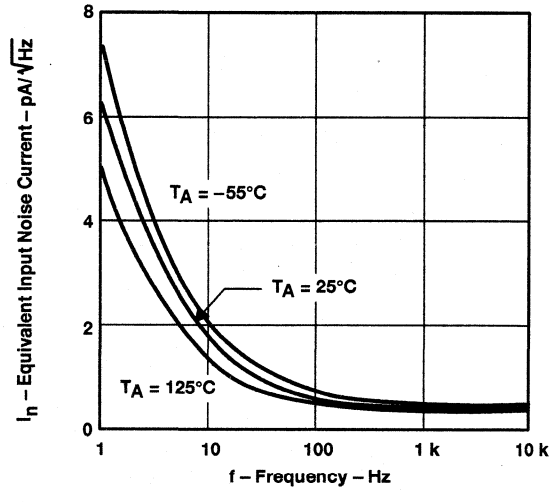


Figure 25

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

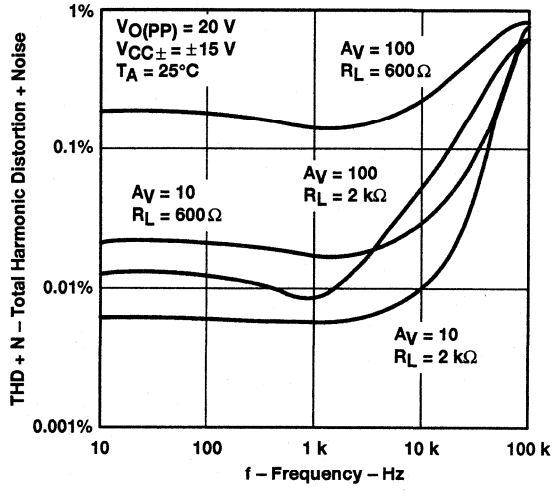


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs FREE-AIR TEMPERATURE

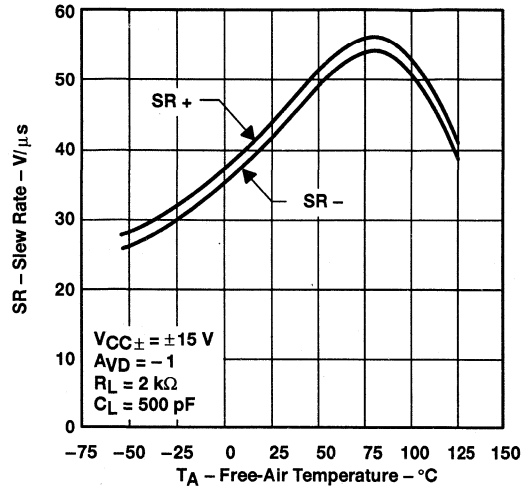


Figure 27

SLEW RATE vs LOAD CAPACITANCE

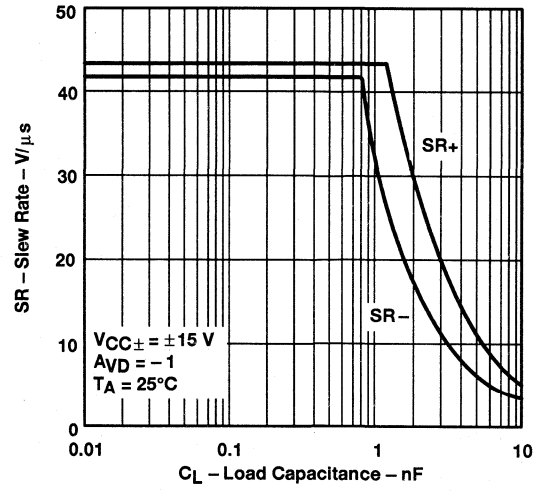


Figure 28

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

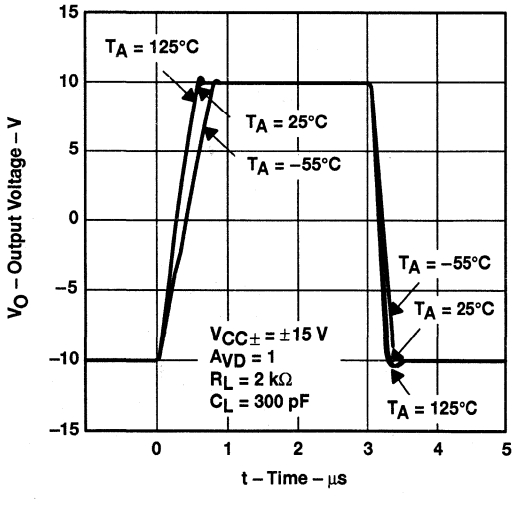


Figure 29

INVERTING LARGE-SIGNAL PULSE RESPONSE

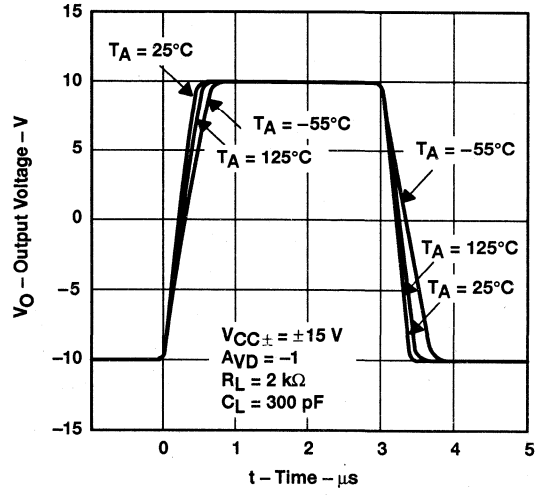


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL PULSE RESPONSE

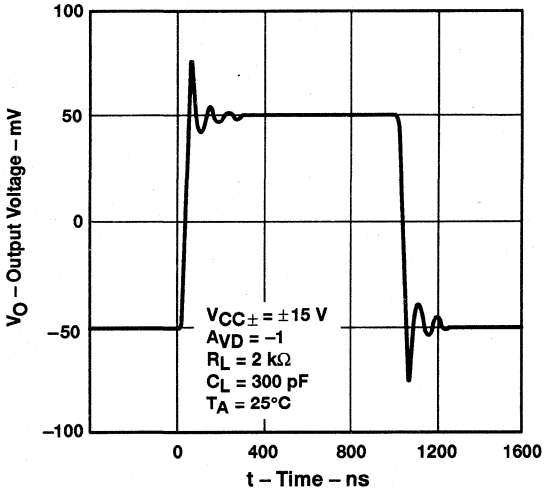


Figure 31

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

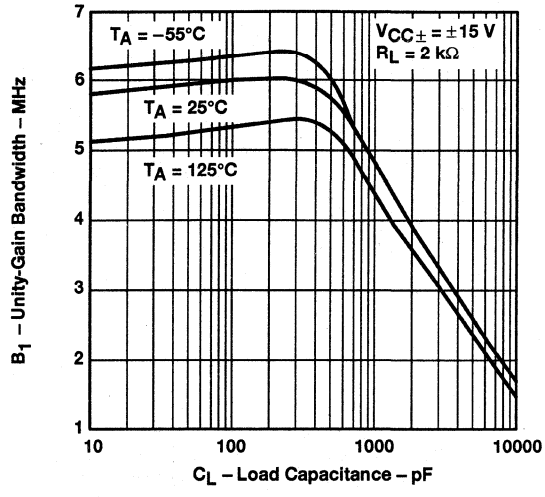


Figure 32

GAIN MARGIN vs LOAD CAPACITANCE

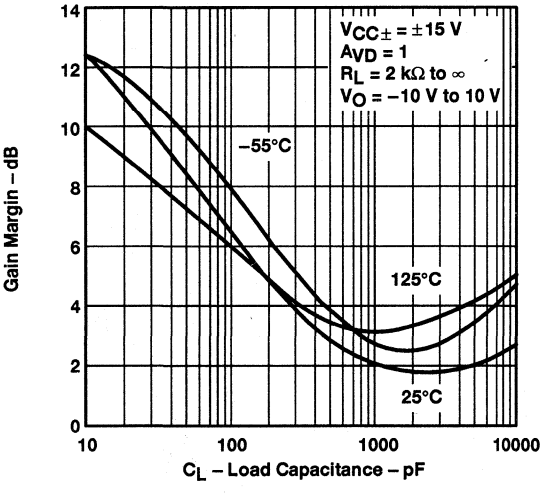


Figure 33

PHASE MARGIN vs LOAD CAPACITANCE

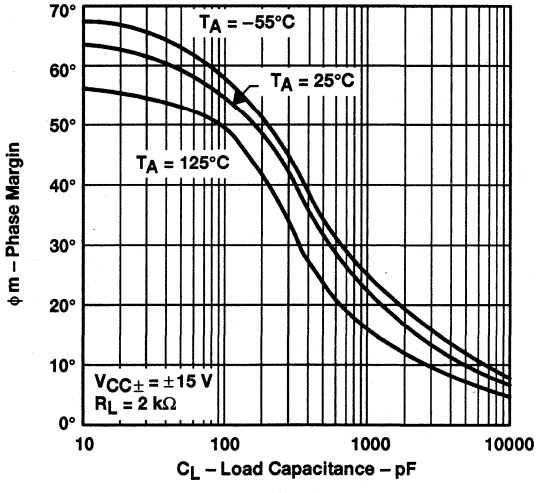
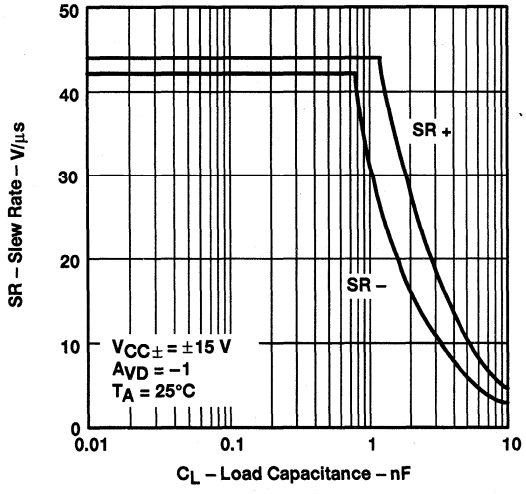


Figure 34

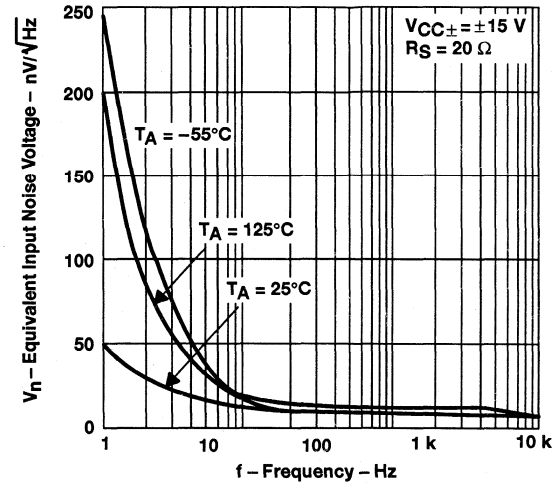
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

- **Low Noise**
  10 Hz . . . 15 nV/√Hz
  1 kHz . . . 10.5 nV/√Hz
- **10000-pF Load Capability**
- **20-mA Min Short-Circuit Output Current**
- **27-V/μs Min Slew Rate**
- **High Gain-Bandwidth Product . . . 5.9 MHz**
- **Low V_{IO} . . . 1.5 mV Max at 25°C**
- **Single or Split Supply**
- **Fast Settling Time**
  340 ns to 0.1%
  400 ns to 0.01%
- **Saturation Recovery . . . 150 ns**
- **Large Output Swing**
  V_{CC-} +0.1 V to V_{CC+} – 1 V

SLEW RATE vs LOAD CAPACITANCE



EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY



description

The TLE2144 and TLE2144A devices are high-performance, internally compensated operational amplifiers built using the Texas Instruments complementary bipolar Excalibur process. The TLE2144A is a tighter offset voltage grade of the TLE2144. Both are pin-compatible upgrades to standard industry products.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM (Y)
		SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	1.5 mV	—	—	—	TLE2144ACN	—
	2.4 mV	TLE2144CDW	—	—	TLE2144CN	
–40°C to 105°C	1.5 mV	—	—	—	TLE2144AIN	TLE2144Y
	2.4 mV	TLE2144IDW	—	—	TLE2144IN	
–55°C to 125°C	1.5 mV	—	TLE2144AMFK	TLE2144AMJ	TLE2144AMN	—
	2.5 mV	TLE2144MDW	TLE2144MFK	TLE2144MJ	TLE2144MN	

The DW packages are available taped and reeled. Add R suffix to device type (e.g., TLE2144CDWR). Chips are tested at T_A = 25°C.

description (continued)

The design incorporates a patent-pending input stage that simultaneously achieves low audio-band noise of 10.5 nV/$\sqrt{\text{Hz}}$ with a 6-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2144 and TLE2144A are useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

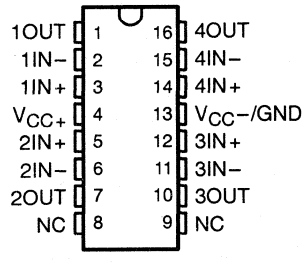
The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 1.5-mV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between V_{CC-} −0.3 to V_{CC+} −1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of V_{CC-} +0.1 to V_{CC+} −1 V under light current loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

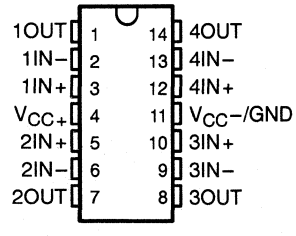
Both versions can also be used as comparators. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

Both the TLE2144 and TLE2144A are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, I-suffix devices from −40°C to 105°C, and M-suffix devices over the full military temperature range of −55°C to 125°C.

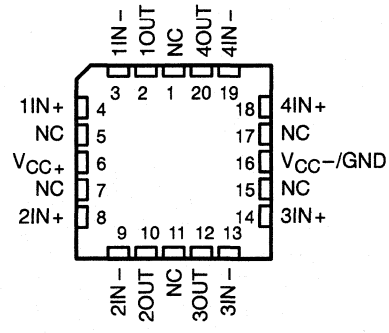
DW PACKAGE
(TOP VIEW)



J OR N PACKAGE
(TOP VIEW)

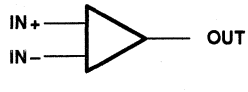


FK PACKAGE
(TOP VIEW)



NC – No internal connection

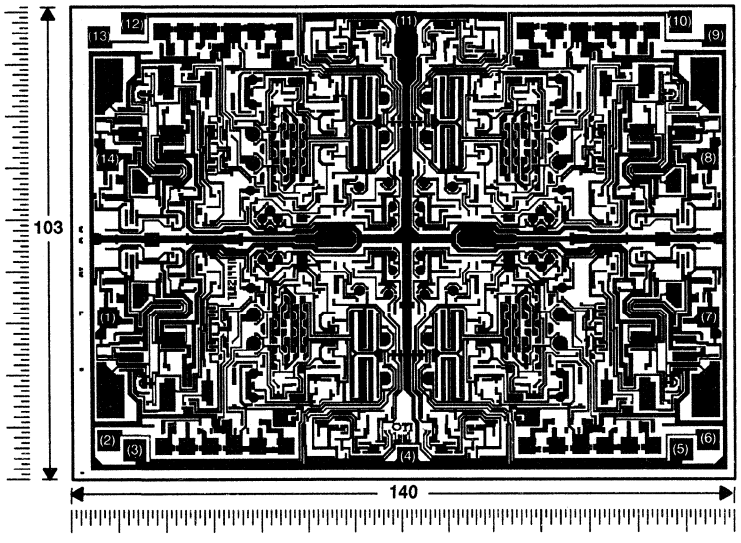
symbol (each amplifier)

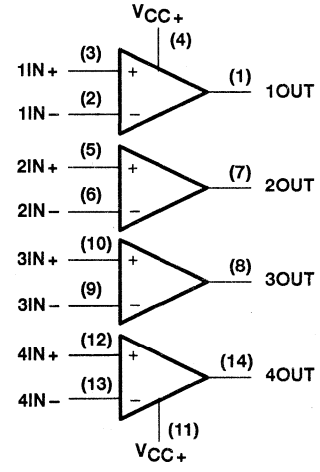


TLE2144Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2144. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

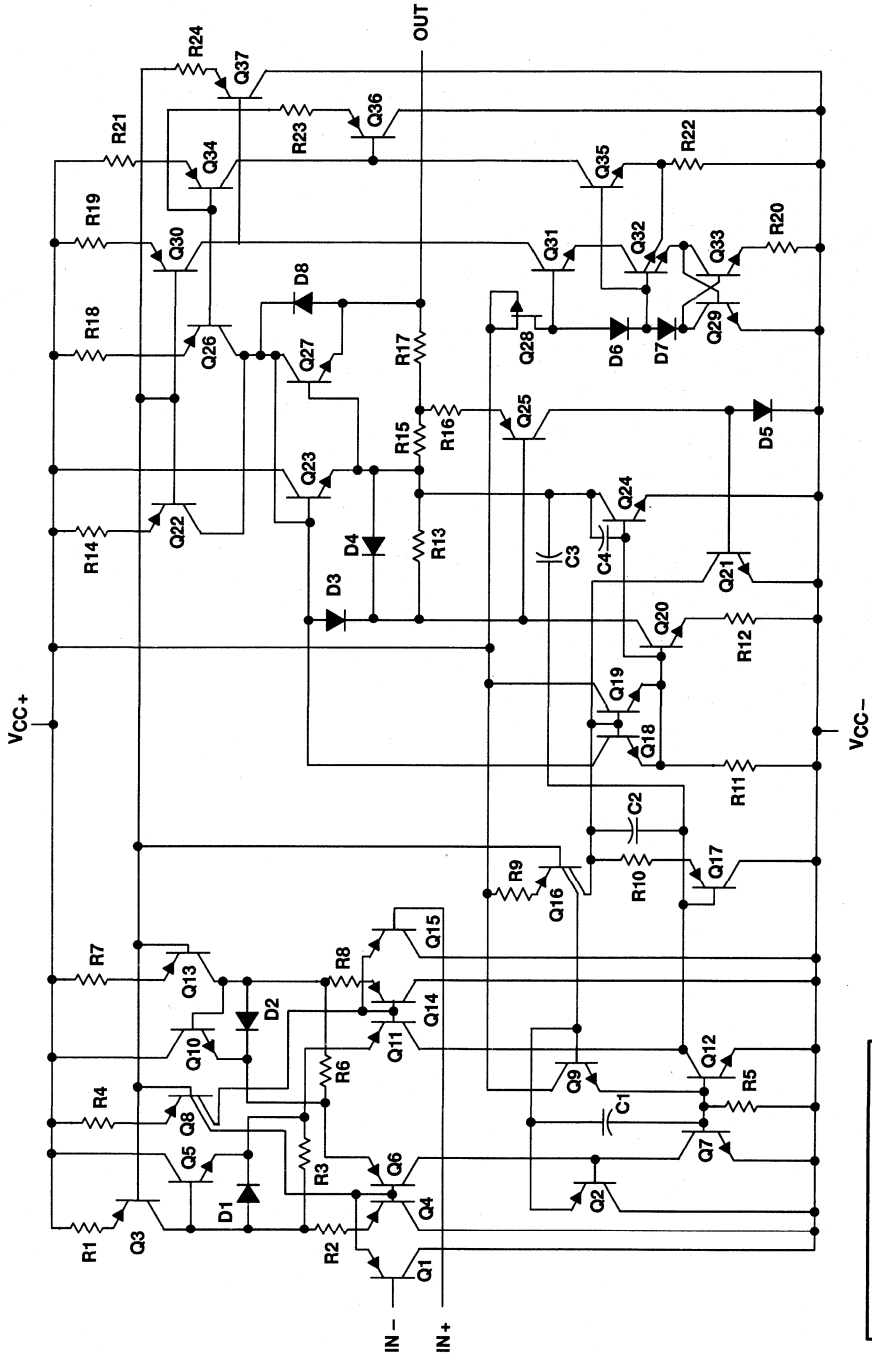
BONDING PADS:
4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (per amplifier)



COMPONENT COUNT (total device)	
Transistors	130
Epi-FET	2
Diodes	28
Resistors	86
Capacitors	16

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 22 V
Supply voltage, V_{CC-} ..... −22 V
Differential input voltage range, V_{ID} (see Note 2) ..... V_{CC+} to V_{CC-}
Input voltage range, V_I (any input) ..... V_{CC+} to V_{CC-} −0.3 V
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 105°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if input is brought below $V_{CC-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	369 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	414 mW	230 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2	±22	±2	±22	±2	±22	V
Common-mode input voltage, V_{IC}	$V_{CC} = 5$ V	0	2.9	0	2.7	0	2.7	V
	$V_{CC\pm} = \pm 15$ V	−15	12.9	−15	12.7	−15	12.7	
Operating free-air temperature, T_A		0	70	−40	105	−55	125	°C

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		0.5	3.8		0.5	3	mV
			Full range			4.4			3.6	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.4	3.7		3.4	3.7		
			Full range	3.4			3.4			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.6		1.2	1.6	V
			Full range			1.7			1.7	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	95		50	95		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.5			18.5	

† Full range is 0°C to 70°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR−	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = −1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2144C			TLE2144AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		0.6	2.4		0.5	1.5	mV
				Full range			3.2			2.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			150			150	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	µA
				Full range			−1.6			−1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.9	−15.3 to 13.1		−15 to 12.9	−15 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −1.5 mA		25°C	13.7	14		13.7	14		
				Full range	13.6			13.6			
		I_O = −15 mA		25°C	13.1	13.7		13.1	13.7		
				Full range	13			13			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	−14.7	−14.9		−14.7	−14.9		V
				Full range	−14.6			−14.6			
		I_O = 1.5 mA		25°C	−14.5	−14.8		−14.5	−14.8		
				Full range	−14.4			−14.4			
		I_O = 15 mA		25°C	−13.4	−13.8		−13.4	−13.8		
				Full range	−13.3			−13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V		25°C	100	170		100	170		V/mV
				Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ		25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		13.8	18		13.8	18	mA
				Full range			18.8			18.8	

† Full range is 0°C to 70°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		0.5	3.8		0.5	3	mV
			Full range			4.8			4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	µA
			Full range			−2.2			−2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 µA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 µA	Full range	3.8			3.8			
		I_{OH} = 1 mA		3.7			3.7			
		I_{OH} = 10 mA		3.5			3.5			
V_{OL}	Low-level output voltage	I_{OL} = 150 µA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 µA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 µA	Full range			175			175	mV
		I_{OL} = 1 mA				225			225	
		I_{OL} = 10 mA				1.4			1.4	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, V_O = 1 V to −1.5 V, R_L = 2 kΩ	25°C	50	95		50	95		V/mV
			Full range	10			10			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.4			18.4	

† Full range is −40°C to 105°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR−	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = −1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 10 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2144I			TLE2144AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		0.6	2.4		0.5	1.5	mV
				Full range			3.2			2.8	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	µA
				Full range			−1.7			−1.7	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 µA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 µA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	170		100	170		V/mV
				Full range	40			40			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		13.8	18		13.8	18	mA
				Full range			18.8			18.8	

† Full range is −40°C to 105°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		0.5	3.8		0.5	3	mV
			Full range			5.2			4.4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.75			3.75			
		I_{OH} = 1 mA		3.65			3.65			
		I_{OH} = 10 mA		3.45			3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 μA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 μA	Full range			200			200	mV
		I_{OL} = 1 mA				250			250	
		I_{OL} = 10 mA				1.45			1.45	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	95		50	95		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.4			18.4	

† Full range is −55°C to 125°C.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = −1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR−	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = −1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1	R_L = 2 kΩ†,		660			660		kHz
ϕ_m	Phase margin	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2144M			TLE2144AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		0.6	2.4		0.5	1.5	mV
				Full range			4			3.2	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	170		100	170		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, V_{IC} = 2.5 V	No load,	25°C		13.8	18		13.8	18	mA
				Full range			18.8			18.8	

† Full range is −55°C to 125°C

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	R_L = 2 kΩ, C_L = 100 pF	A_{VD} = −1,	27	45		27	45		V/μs
SR−	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = −1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		.4			.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 10 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2144Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω, V_O = 0			0.3	1.8	mV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	µA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		
		I_O = −15 mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V,	R_S = 50 Ω	85	106		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−25	−50		mA
			V_{ID} = −1 V	20	31		
I_{CC}	Supply current	V_O = 0,	No load		13.8	18	mA

TYPICAL CHARACTERISTICS

Table of Graphs

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TYPICAL CHARACTERISTICS†

**TLE2144
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

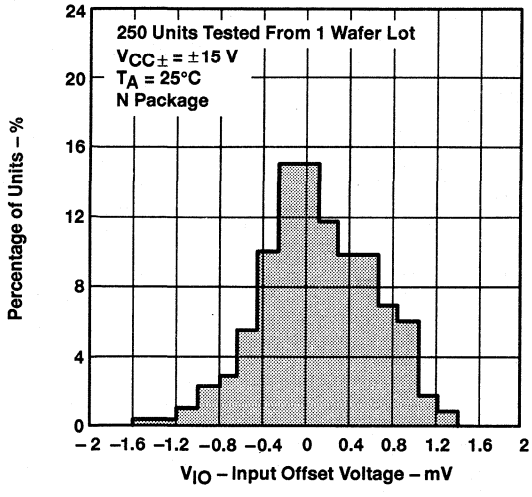


Figure 1

**INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

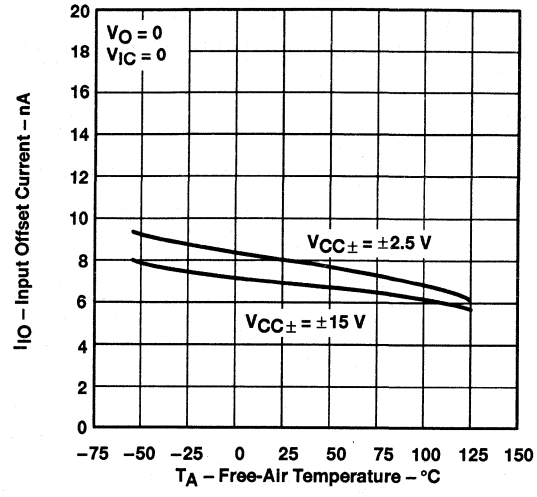


Figure 2

**INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE**

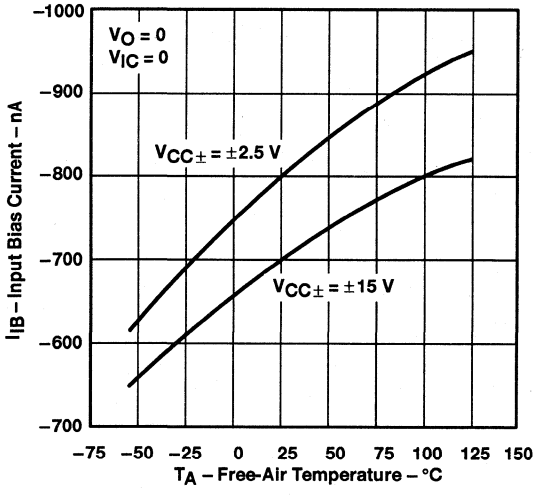


Figure 3

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

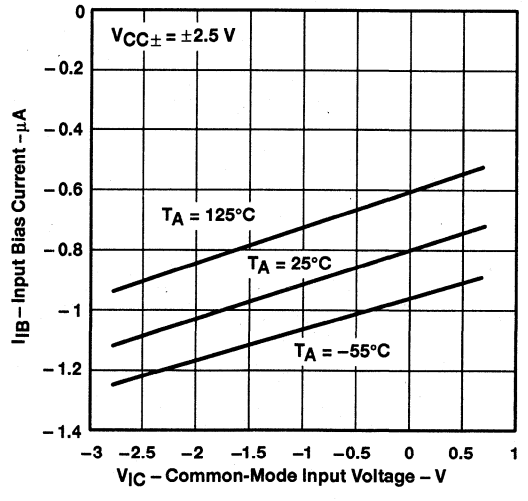


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

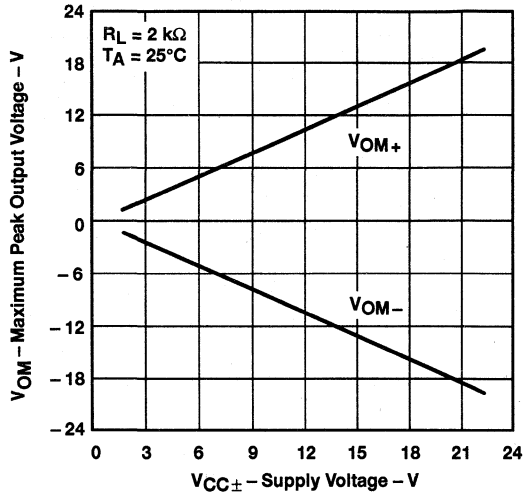


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

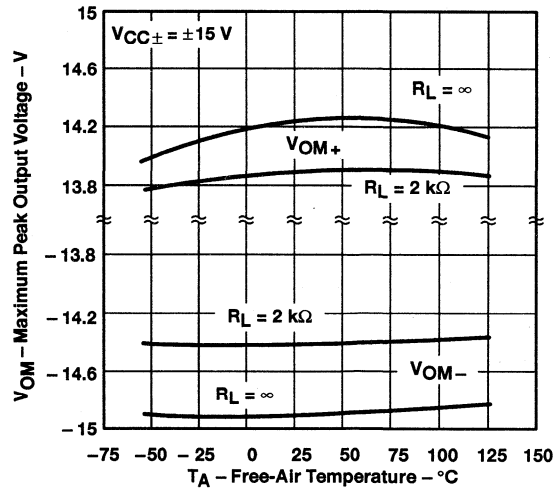


Figure 6

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

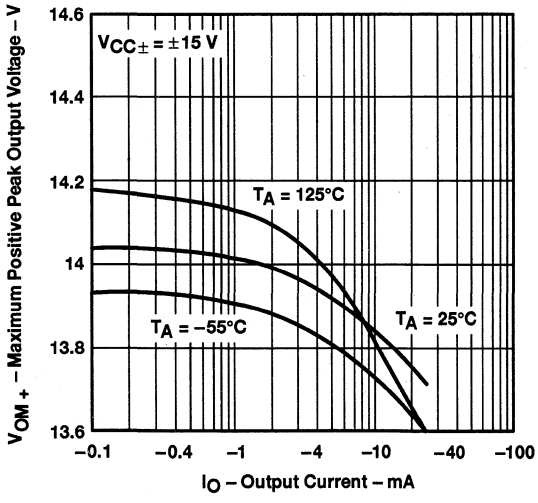


Figure 7

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

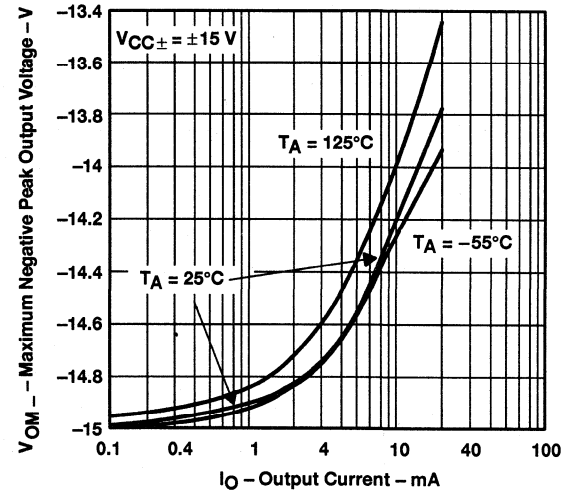


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SETTLING TIME

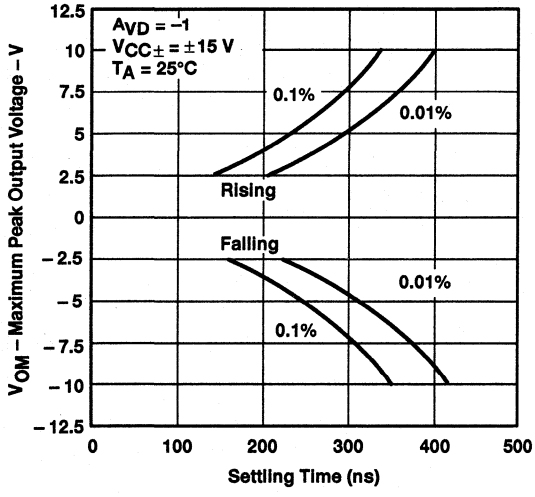


Figure 9

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

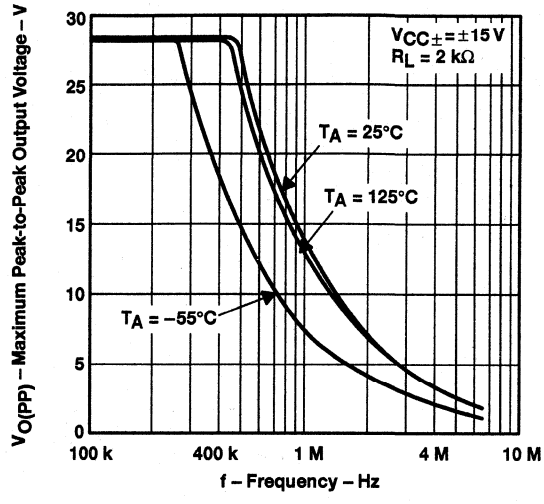


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

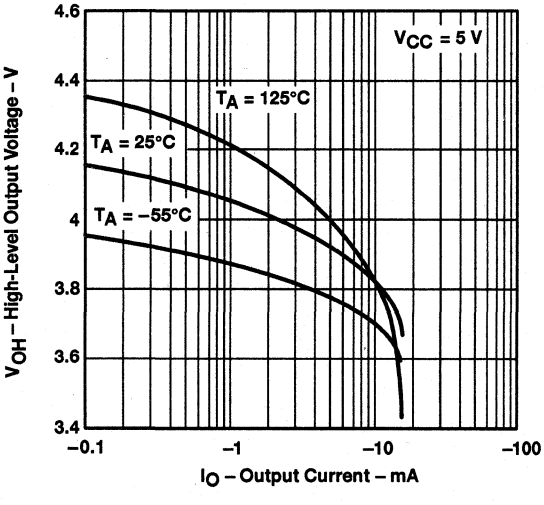


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

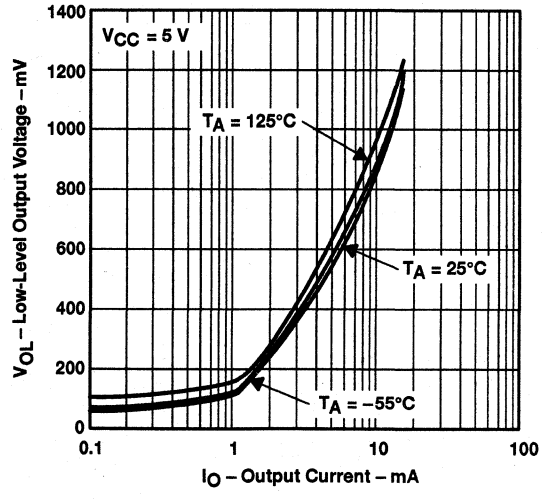


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

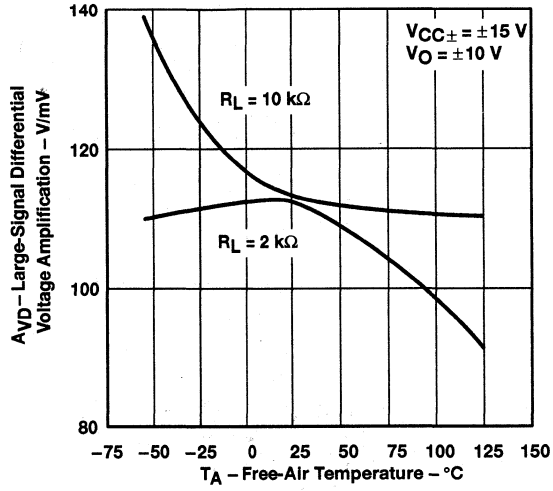


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

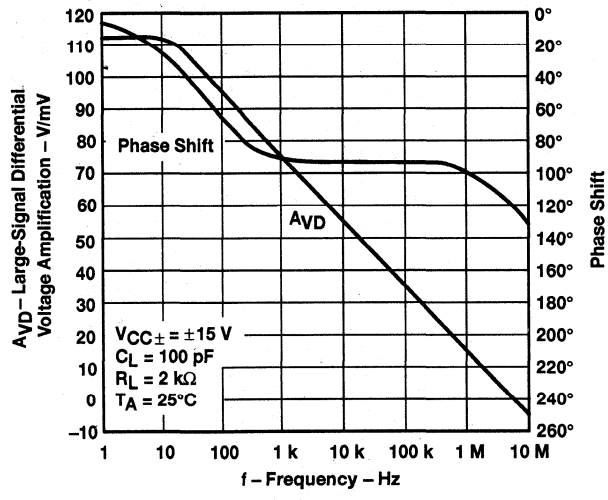


Figure 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

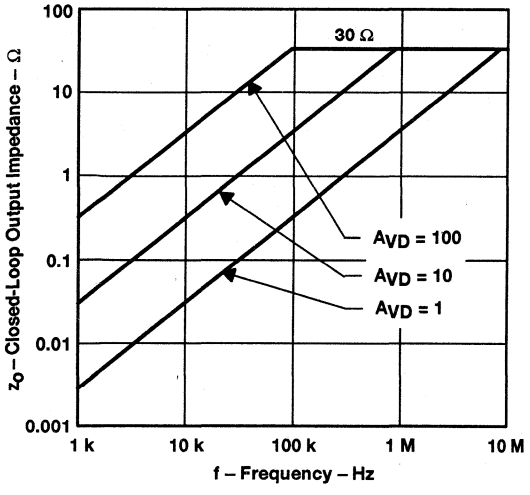


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

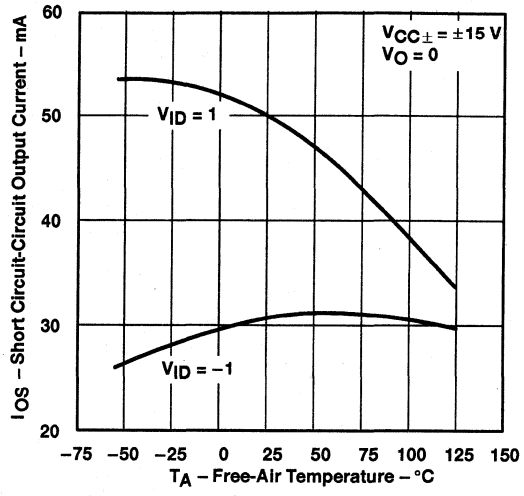


Figure 16

COMMON-MODE REJECTION RATIO vs FREQUENCY

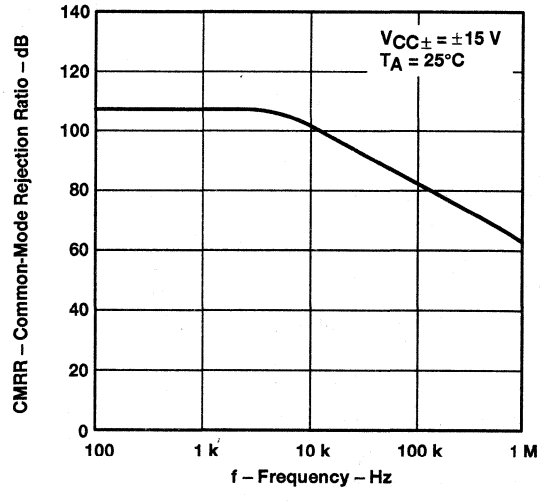


Figure 17

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

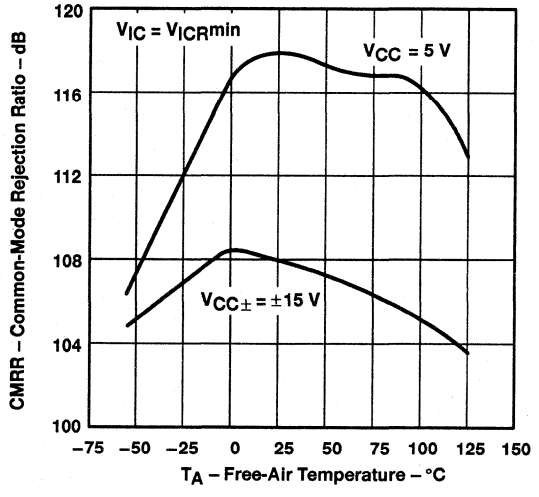


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

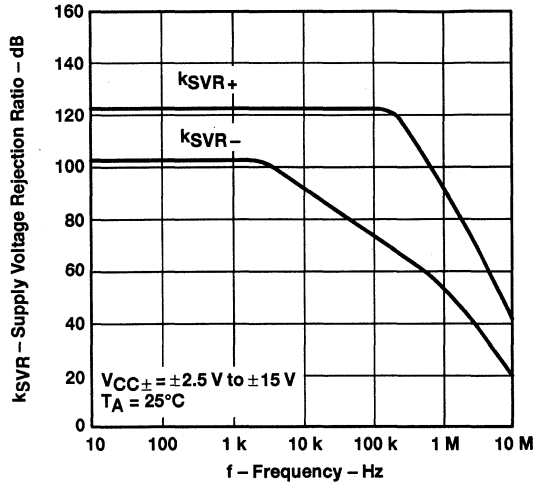


Figure 19

SUPPLY VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

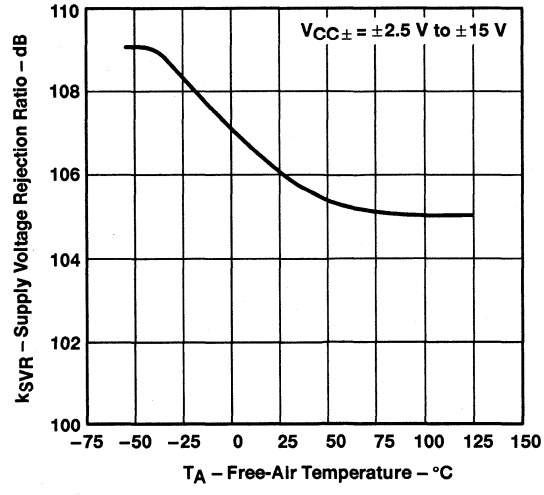


Figure 20

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

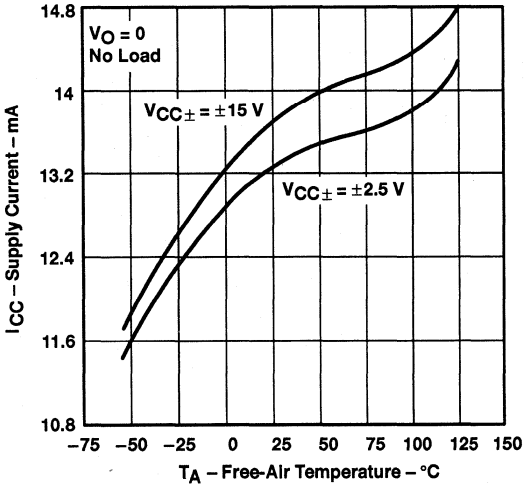


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

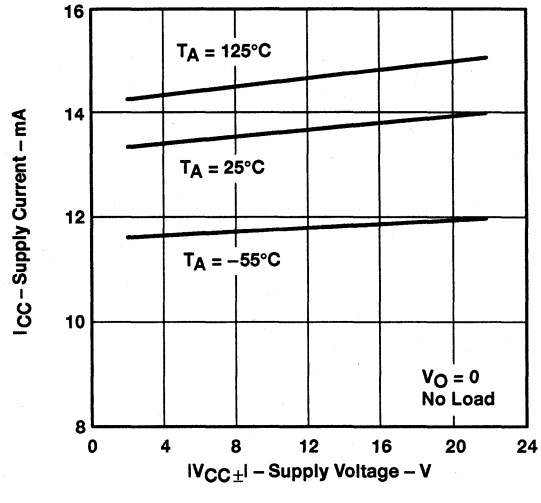


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

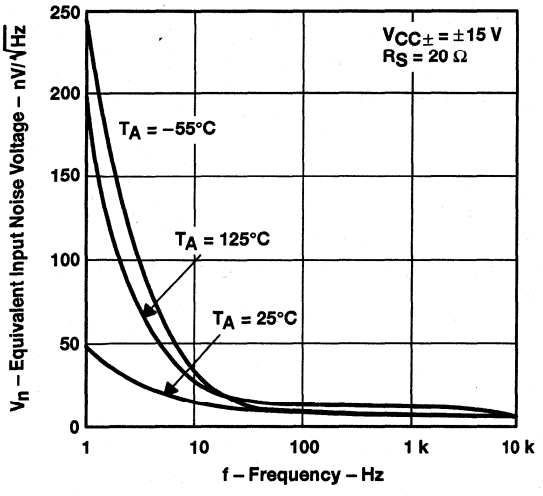


Figure 23

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

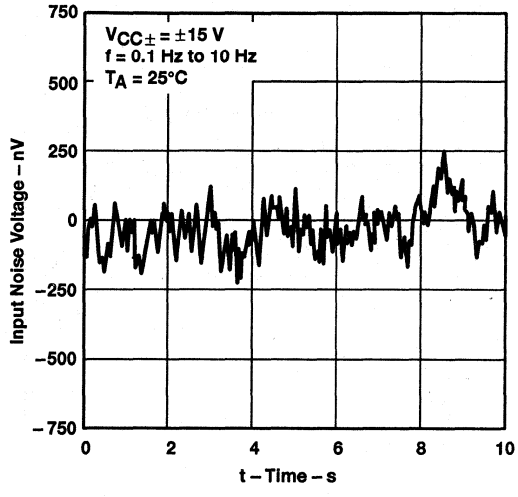


Figure 24

NOISE CURRENT vs FREQUENCY

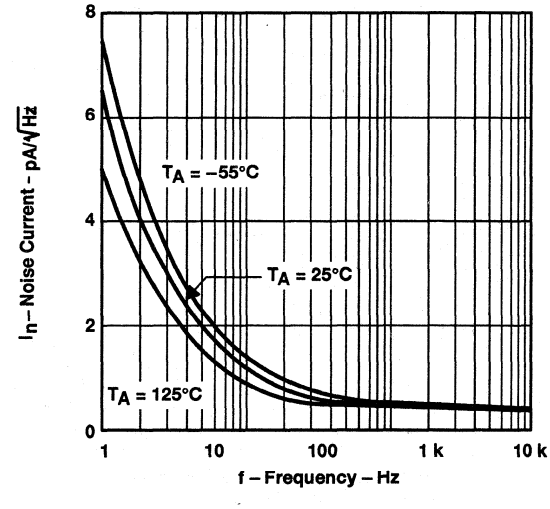


Figure 25

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

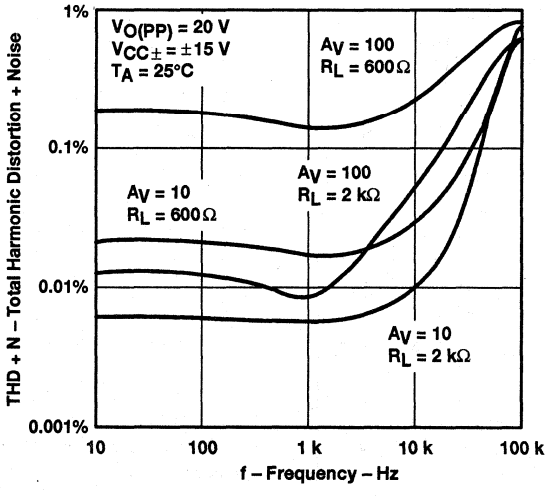


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE vs FREE-AIR TEMPERATURE

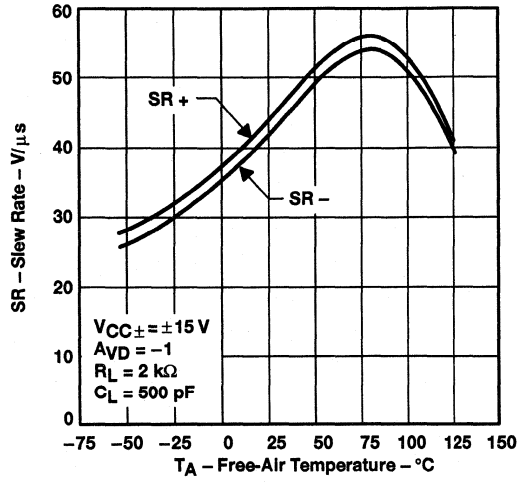


Figure 27

SLEW RATE vs LOAD CAPACITANCE

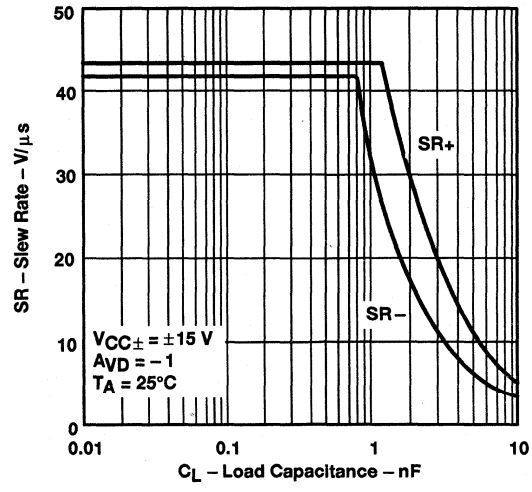


Figure 28

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

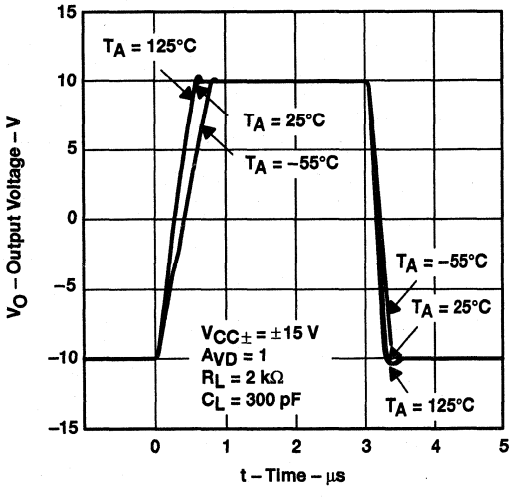


Figure 29

INVERTING LARGE-SIGNAL PULSE RESPONSE

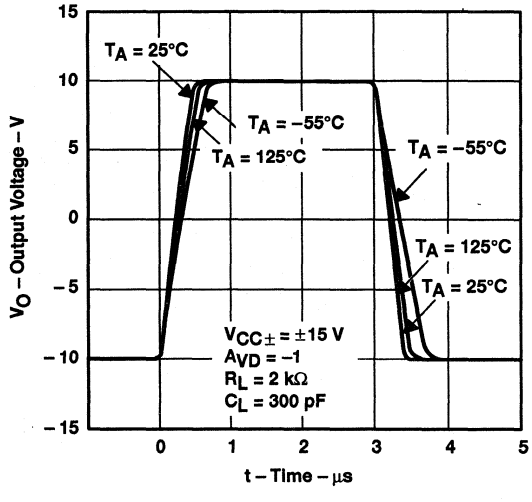


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SMALL-SIGNAL
PULSE RESPONSE

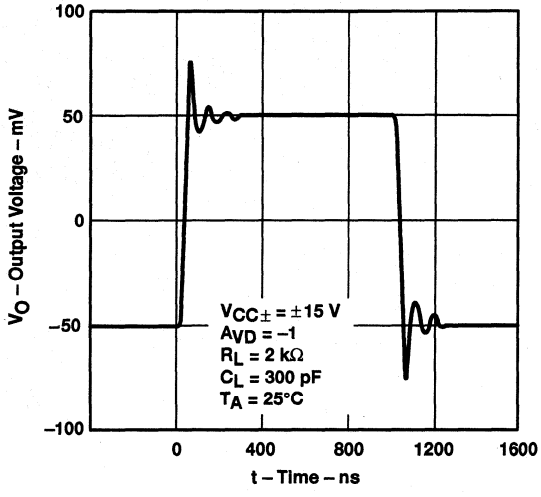


Figure 31

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

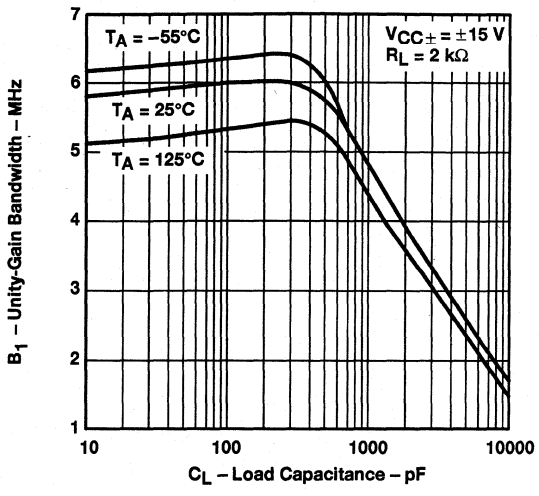


Figure 32

GAIN MARGIN
vs
LOAD CAPACITANCE

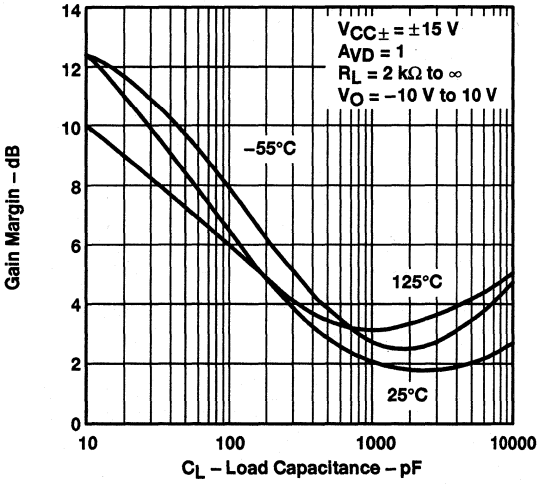


Figure 33

PHASE MARGIN
vs
LOAD CAPACITANCE

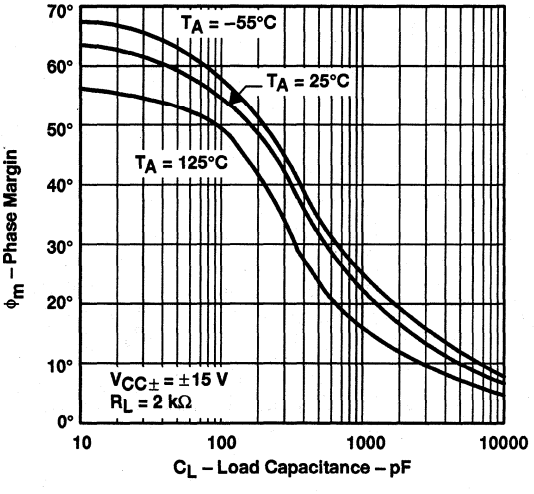


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

- **Excellent Output Drive Capability**
  V_O = ± 2.5 V Min at R_L = 100 Ω,
  $V_{CC±}$ = ± 5 V
  V_O = ± 12.5 V Min at R_L = 600 Ω,
  $V_{CC±}$ = ± 15 V
- **Low Supply Current . . . 280 μA Typ**
- **Decompensated for High Slew Rate and Gain-Bandwidth Product**
  A_{VD} = 0.5 Min
  Slew Rate = 10 V/μs Typ
  Gain-Bandwidth Product = 6.5 MHz Typ
- **Macromodel Included**
- **Wide Operating Supply Voltage Range**
  $V_{CC±}$ = ± 3.5 V to ± 20 V
- **High Open-Loop Gain . . . 280 V/mV Typ**
- **Low Offset Voltage . . . 500 μV Max**
- **Low Offset Voltage Drift With Time**
  0.04 μV/Month Typ
- **Low Input Bias Current . . . 5 pA Typ**

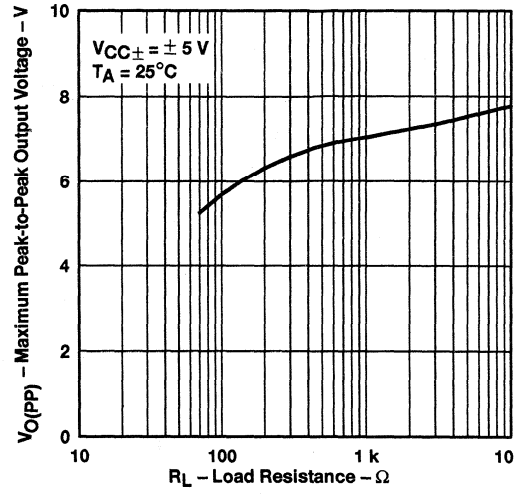
description

The TLE2161, TLE2161A, and TLE2161B are JFET-input, low-power, precision operational amplifiers manufactured using the Texas Instruments Excalibur process. Decompensated for stability with a minimum closed-loop gain of 5, these devices combine outstanding output drive capability with low power consumption, excellent dc precision, and high gain-bandwidth product.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a device that remains precise even with changes in temperature and over years of use.

A variety of available options includes small-outline packages and chip-carrier versions for high-density system applications.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE



AVAILABLE OPTIONS

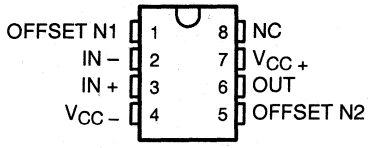
T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV	—	—	—	TLE2161BCP
	1.5 mV	TLE2161ACD			TLE2161ACP
	3 mV	TLE2161CD	—	—	TLE2161CP
−40°C to 85°C	500 μV	—	—	—	TLE2161BIP
	1.5 mV	TLE2161AID			TLE2161AIP
	3 mV	TLE2161ID	—	—	TLE2161IP
−55°C to 125°C	500 μV	—	—	TLE2161BMJG	TLE2161BMP
	1.5 mV	TLE2161AMD	TLE2161AMFK	TLE2161AMJG	TLE2161AMP
	3 mV	TLE2161MD	TLE2161MFK	TLE2161MJG	TLE2161MP

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2161ACDR).

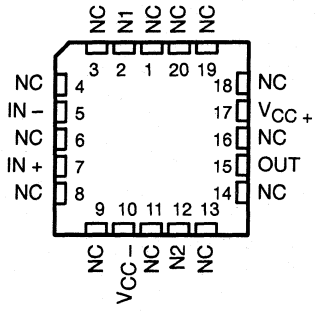
description (continued)

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

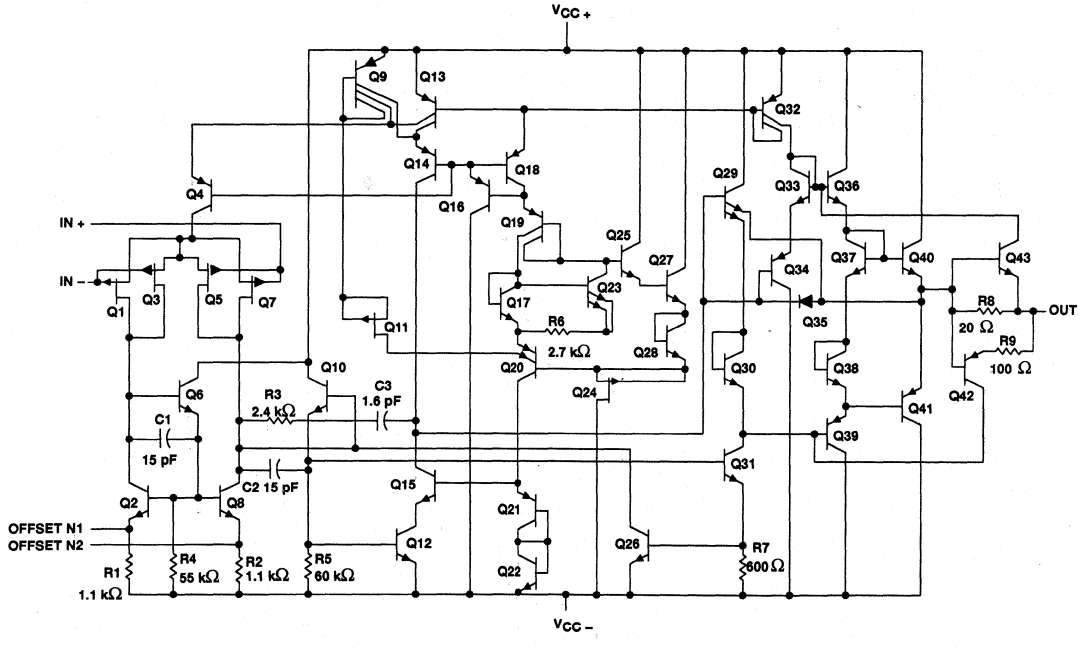


FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} ..... −19 V
Differential input voltage, V_{ID} (see Note 2) ..... ±38 V
Input voltage range, V_I (any input) ..... $V_{CC\pm}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±80 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and /or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		+3.5	+20	+3.5	+20	+3.5	+20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	−1.6	4	−1.6	4	−1.6	4	V
	$V_{CC\pm} = \pm 15$ V	−11	13	−11	13	−11	13	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161C, TLE2161AC TLE2161BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161C	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			4	
		TLE2161AC		25°C		0.6	2.6	
				Full range			3.5	
		TLE2161BC		25°C		0.5	1.9	
				Full range			2.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.3			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		V_O = 0, No load	25°C		280	325	μA
				Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		29		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A†	TLE2161C, TLE2161AC TLE2161BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	A_{VD} = 5,	R_L = 10 kΩ,	C_L = 100 pF	25°C	7	10		V/μs
					Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω,	f = 10 Hz		25°C		59	100	nV/√Hz
		R_S = 20 Ω,	f = 1 kHz				43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	A_{VD} = 5,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz,	R_L = 10 kΩ,	C_L = 100 pF	25°C		5.8		MHz
		f = 100 kHz,	R_L = 100 kΩ,	C_L = 100 pF			4.3		
t_s	Settling time	ε = 0.1%			25°C		5		μs
		ε = 0.01%					10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5,	R_L = 10 kΩ		25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5,	R_L = 10 kΩ,	C_L = 100 pF	25°C		70°		
		A_{VD} = 5,	R_L = 100 Ω,	C_L = 100 pF			84°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161C, TLE2161AC TLE2161BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161C	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			3.9	
		TLE2161AC		25°C		0.5	1.5	
				Full range			2.5	
		TLE2161BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to − 8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		VCC± = ±5 V to ±15 V, RS = 50 Ω	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		V_O = 0, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		34		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A†	TLE2161C, TLE2161AC TLE2161BC			UNIT
						MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	A_{VD} = 5,	R_L = 10 kΩ,	C_L = 100 pF	25°C	7	10		V/μs
					Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω,	f = 10 Hz		25°C		70	100	nV/√Hz
		R_S = 20 Ω,	f = 1 kHz				40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	A_{VD} = 5,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz,	R_L = 10 kΩ,	C_L = 100 pF	25°C		6.4		MHz
		f = 100 kHz,	R_L = 600 Ω,	C_L = 100 pF			5.6		
t_s	Settling time	ε = 0.1%			25°C		5		μs
		ε = 0.01%					10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5,	R_L = 10 kΩ		25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5,	R_L = 10 kΩ,	C_L = 100 pF	25°C		72°		
		A_{VD} = 5,	R_L = 600 Ω,	C_L = 100 pF			78°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161I, TLE2161AI TLE2161BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161I	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			4.4	
		TLE2161AI		25°C		0.6	2.6	
				Full range			3.9	
		TLE2161BI		25°C		0.5	1.9	
				Full range			2.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			
V_{OM+}	Maximum positive peak output voltage		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.1			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.1			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		280	325	μA
				Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		29		μA

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A= 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A†	TLE2161I, TLE2161AI TLE2161BI			UNIT
						MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	A_{VD} = 5,	R_L = 10 kΩ,	C_L = 100 pF	25°C	7	10		V/μs
					Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω,	f = 10 Hz		25°C		59	100	nV/√Hz
		R_S = 20 Ω,	f = 1 kHz				43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	A_{VD} = 5,	f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz,	R_L = 10 kΩ,	C_L = 100 pF	25°C		5.8		MHz
		f = 100 kHz,	R_L = 100 Ω,	C_L = 100 pF			4.3		
t_s	Settling time	ε = 0.1%			25°C		5		μs
		ε = 0.01%					10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5,	R_L = 10 kΩ		25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5,	R_L = 10 kΩ,	C_L = 100 pF	25°C		70°		
		A_{VD} = 5,	R_L = 100 Ω,	C_L = 100 pF			84°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161I, TLE2161AI TLE2161BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161I	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			4.3	
		TLE2161AI		25°C		0.5	1.5	
				Full range			2.9	
		TLE2161BI		25°C		0.3	0.5	
				Full range			1.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to − 8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		34		μA

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A= 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161I, TLE2161AI TLE2161IB			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		70	100	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 5, R_L = 10 kΩ, f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		6.4		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF			5.6		
t_s	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF			78°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161M, TLE2161AM, TLE2161BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161M	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			6	
		TLE2161AM		25°C		0.6	2.6	
				Full range			4.6	
		TLE2161BM		25°C		0.5	1.9	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
		FK and JG packages	R_L = 600 Ω	25°C	2.5	3.6		V
				Full range	2			
		D and P packages	R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3			
		FK and JG packages	R_L = 600 Ω	25°C	−2.5	−3.5		
				Full range	−2			
		D and P packages	R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to −2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			
		D and P packages	V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ± 5 V (unless otherwise noted continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161M TLE2161AM TLE2161BM			UNIT
				MIN	TYP	MAX	
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	V_O = 0, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range	V_O = 0, No load	Full range		39		μA

† Full range is – 55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ± 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2161M TLE2161AM TLE2161BM			UNIT
			MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF		10		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz		59		nV/√Hz
		R_S = 20 Ω, f = 1 kHz		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 5, f = 10 kHz, $V_{O(PP)}$ = 2 V, R_L = 10 kΩ		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF		5.8		MHz
		f = 100 kHz, R_L = 600 kΩ, C_L = 100 pF		4.3		
t_s	Settling time	ε = 0.1%		5		μs
		ε = 0.01%		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ		420		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF		70°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF		84°		

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161M, TLE2161AM, TLE2161BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161M	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			6	
		TLE2161AM		25°C		0.5	1.5	
				Full range			3.6	
		TLE2161BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−12.5			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	7			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		46		μA

† Full range is – 55°C to 125°C.

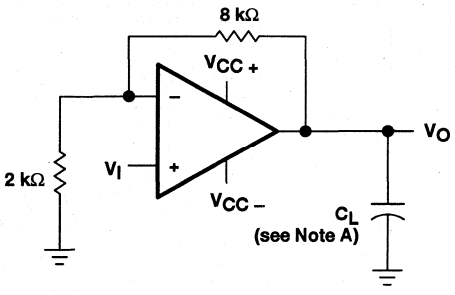
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161M, TLE2161AM, TLE2161BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		70		nV/√Hz
		R_S = 20 Ω, f = 1 kHz			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 Hz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 5, R_L = 10 kΩ, f = 10 kHz,	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		6.4		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF			5.6		
t_s	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF			78°		

† Full range is – 55°C to 125°C.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

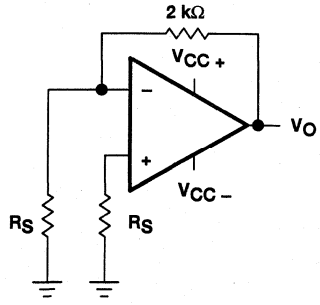
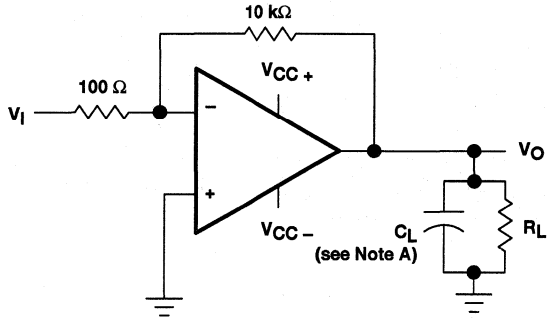


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Gain-Bandwidth Product and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

Input bias and offset current

At the picoampere bias-current level typical of the TLE2161, TLE2161A, and TLE2161B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

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I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5 6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{ICR}	Common-mode input voltage range limits	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage	vs Output current vs Supply voltage	8, 9 10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	16 17
I_{OS}	Short-circuit output current	vs Time vs Free-air temperature	18 19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	22 23
	Pulse response	Small signal Large signal	24, 25 26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
V_n	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	32 33
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature	34 35
	Phase shift	vs Frequency	16

TYPICAL CHARACTERISTICS†

TLE2161
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

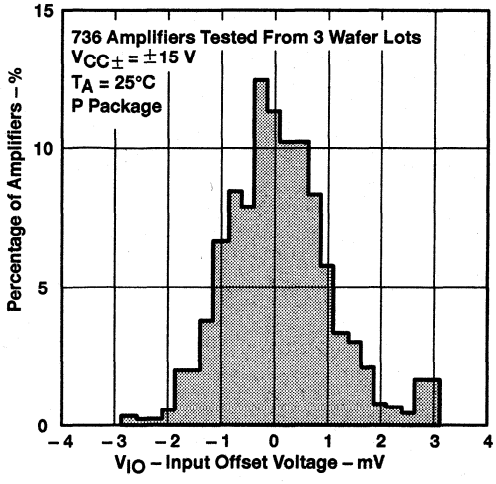

Figure 4

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

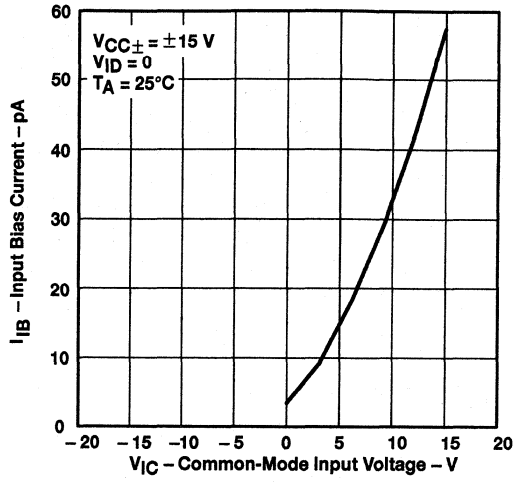

Figure 5

INPUT BIAS CURRENT
AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

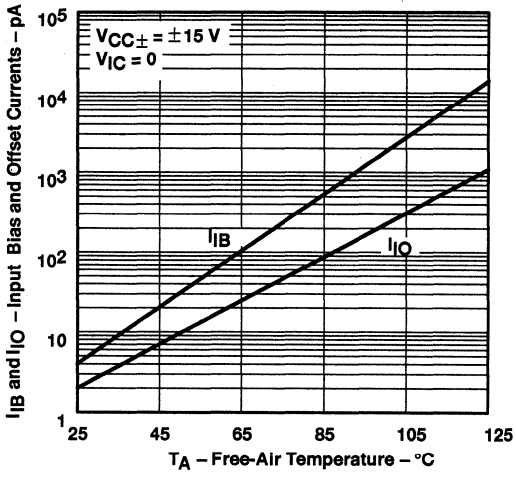

Figure 6

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

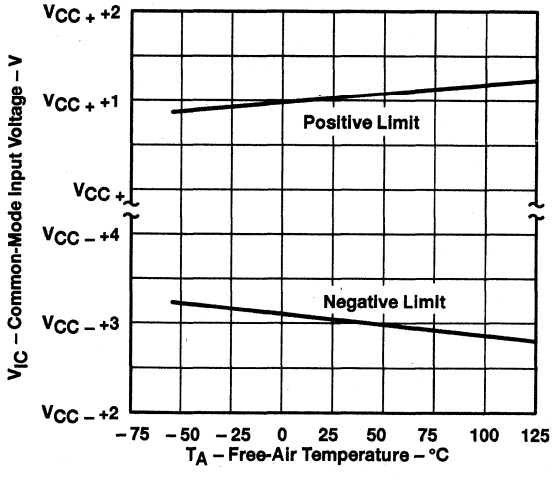

Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

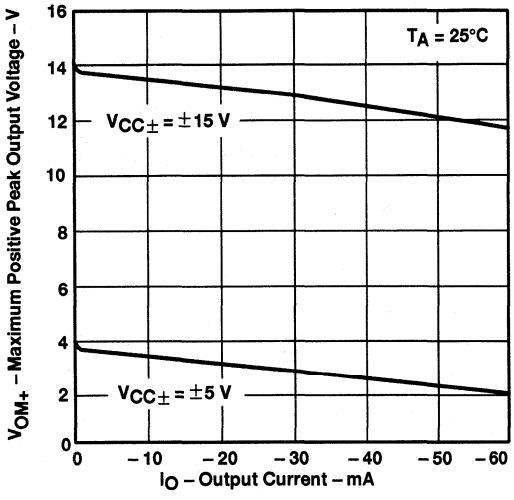

Figure 8

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

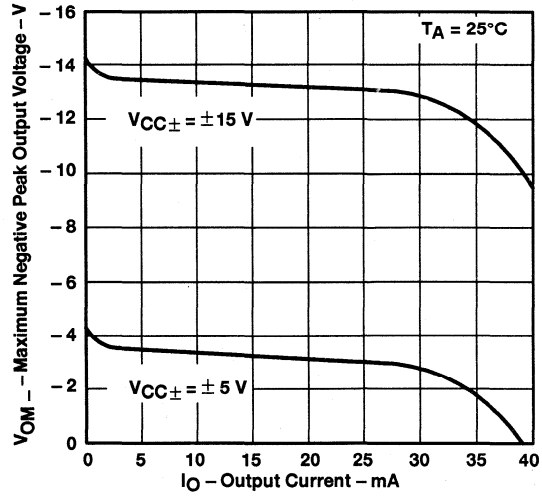

Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

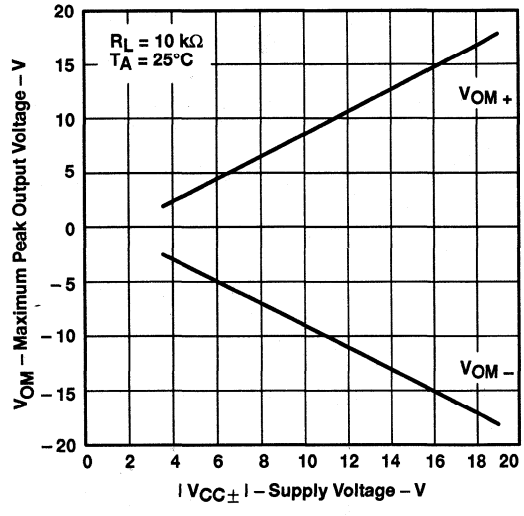

Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

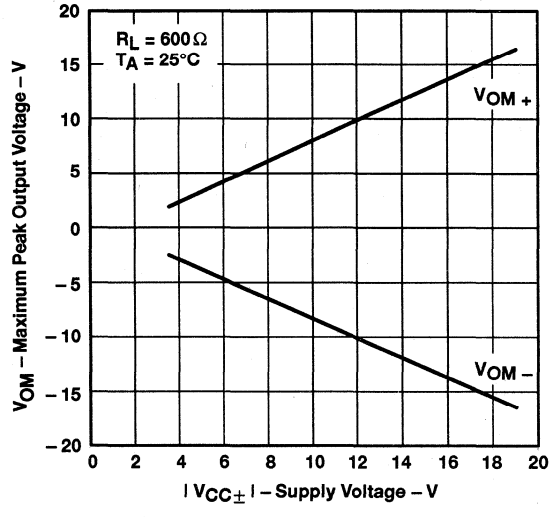

Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

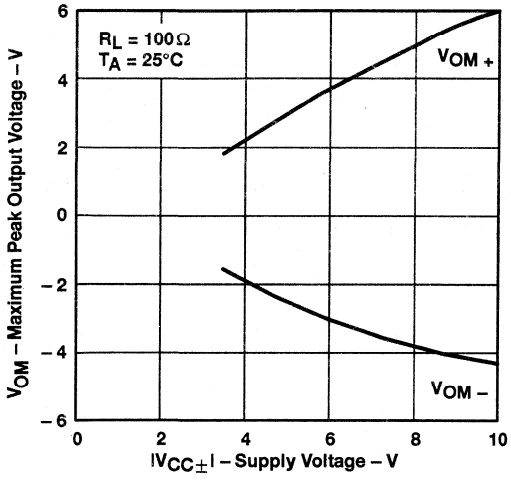

Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

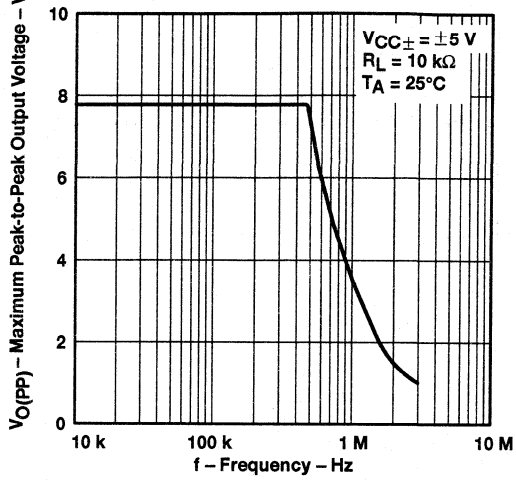

Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FRQUENCY

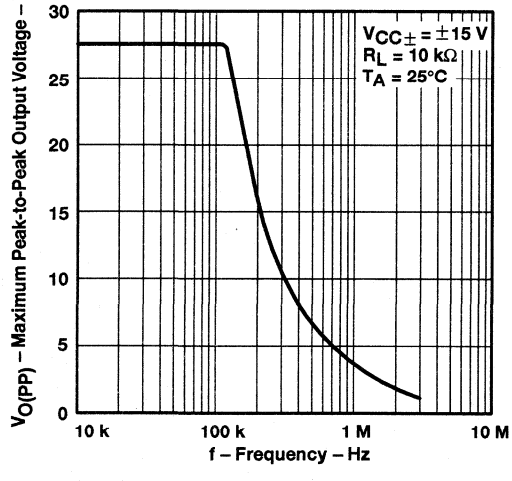

Figure 14

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

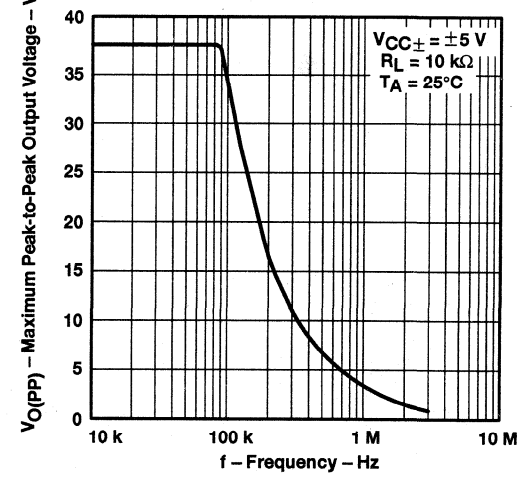

Figure 15

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FRQUENCY

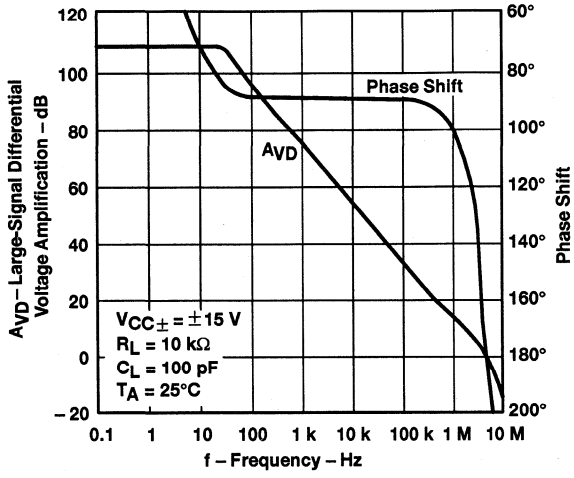

Figure 16

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

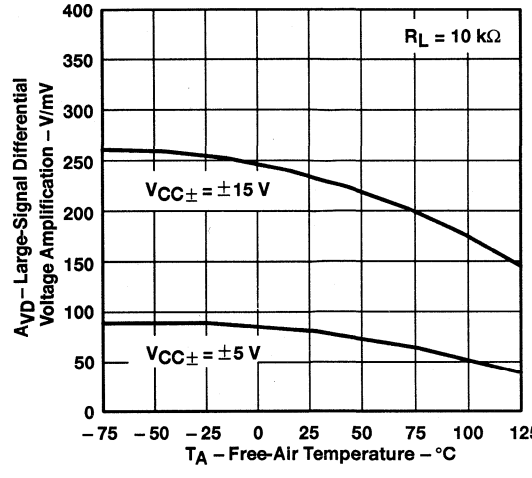

Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

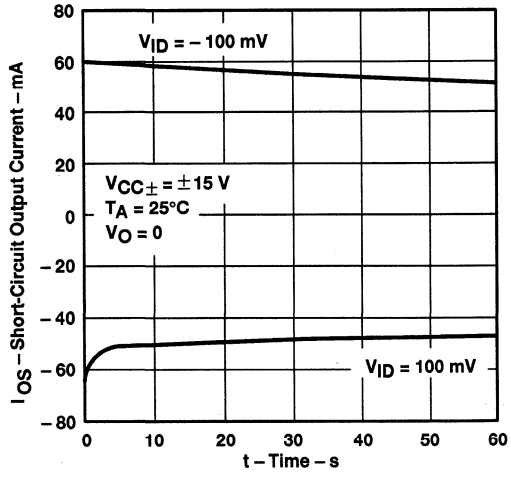

Figure 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

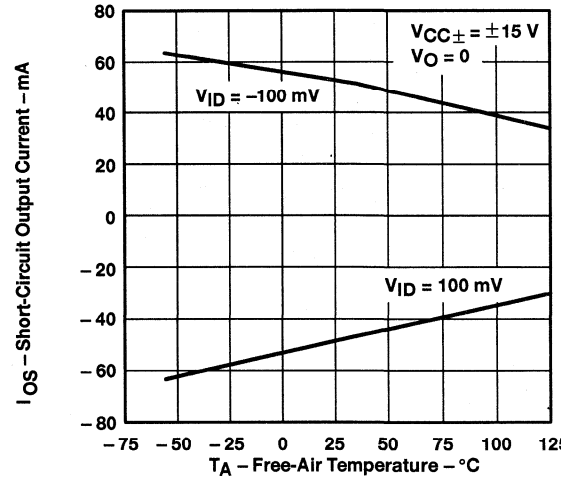

Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE vs FREQUENCY

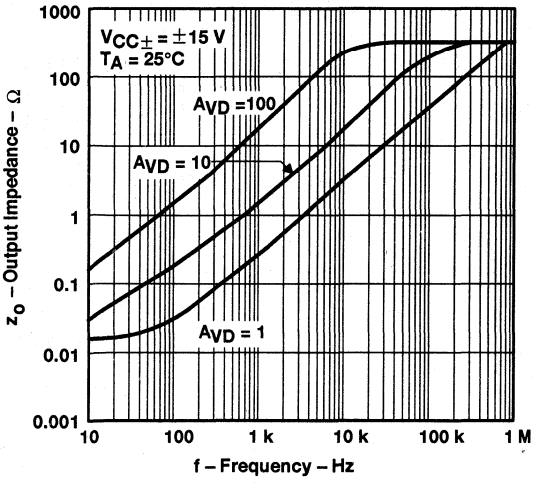

Figure 20

COMMON-MODE REJECTION RATIO vs FREQUENCY

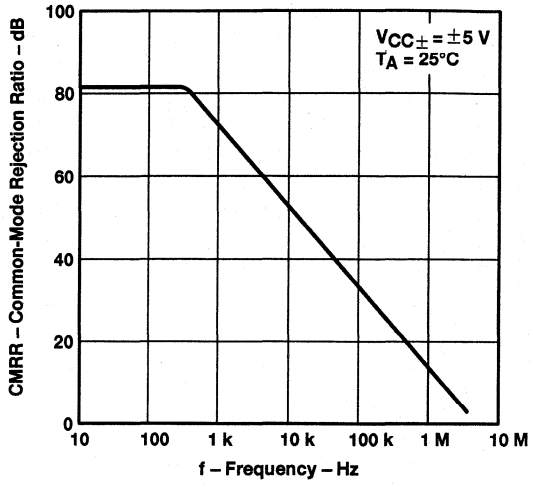

Figure 21

SUPPLY CURRENT vs SUPPLY VOLTAGE

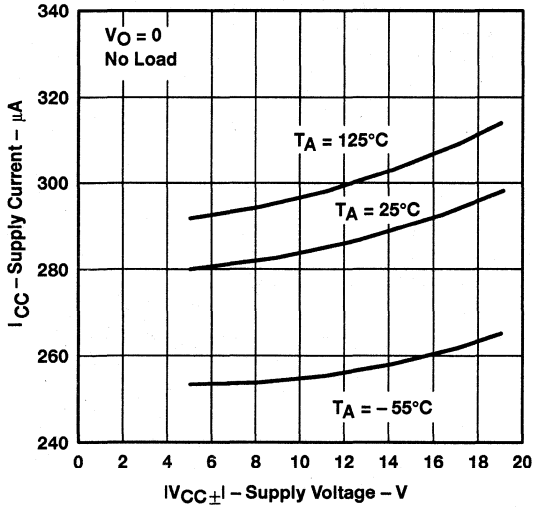

Figure 22

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

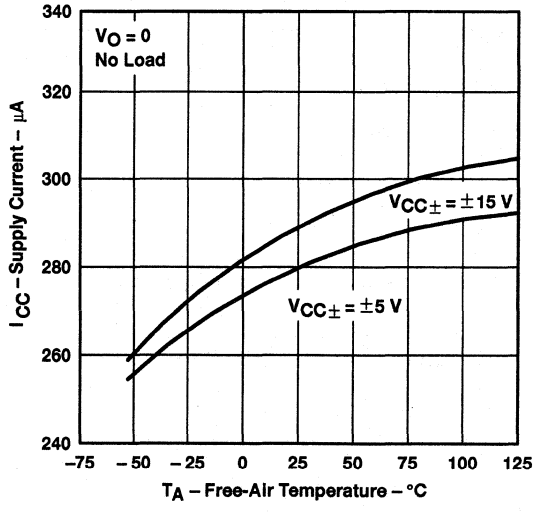

Figure 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SMALL-SIGNAL
PULSE RESPONSE

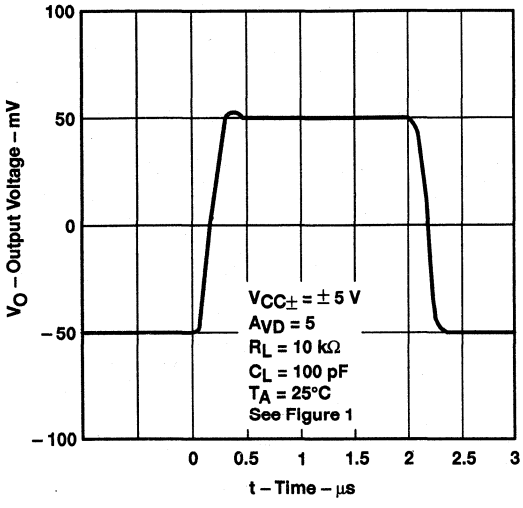

Figure 24

SMALL-SIGNAL
PULSE RESPONSE

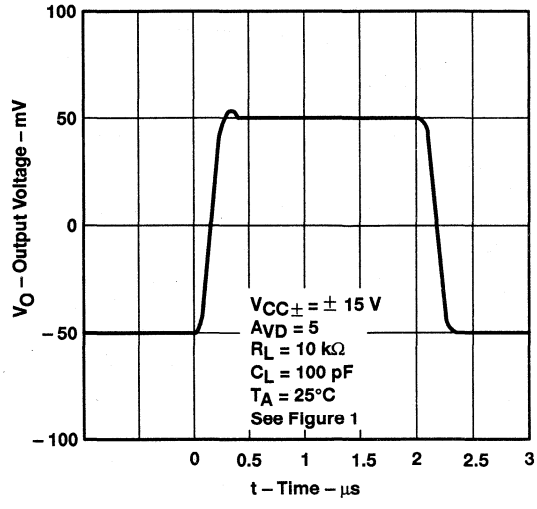

Figure 25

LARGE-SIGNAL
PULSE RESPONSE

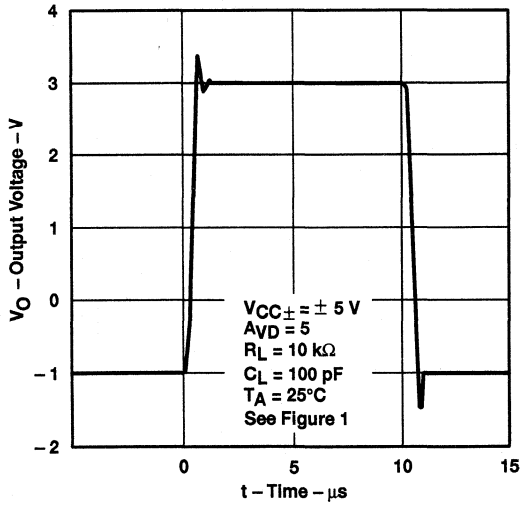

Figure 26

LARGE-SIGNAL
PULSE RESPONSE

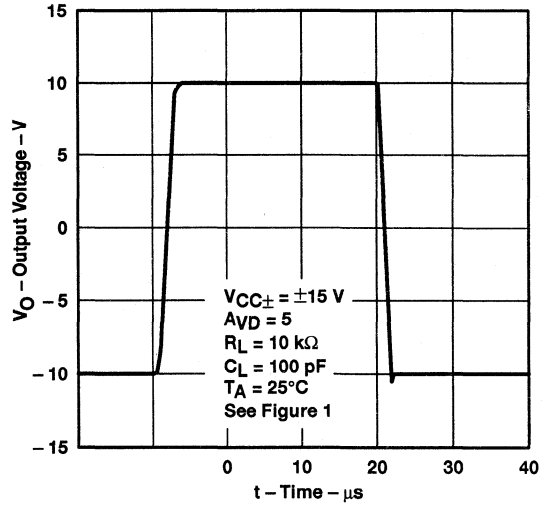

Figure 27

TYPICAL CHARACTERISTICS

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

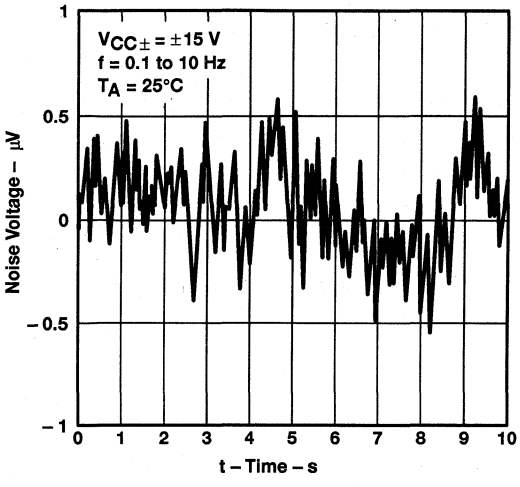

Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

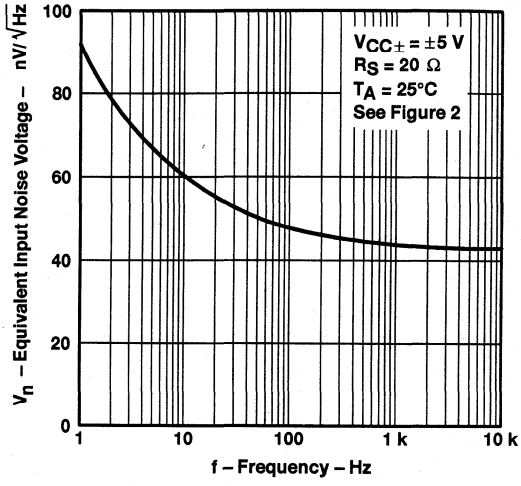

Figure 29

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

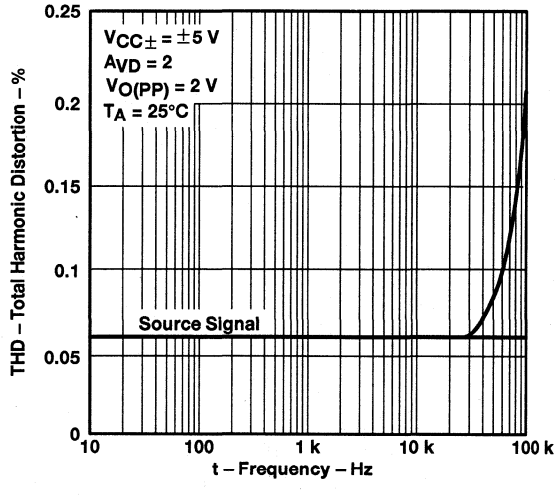

Figure 30

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

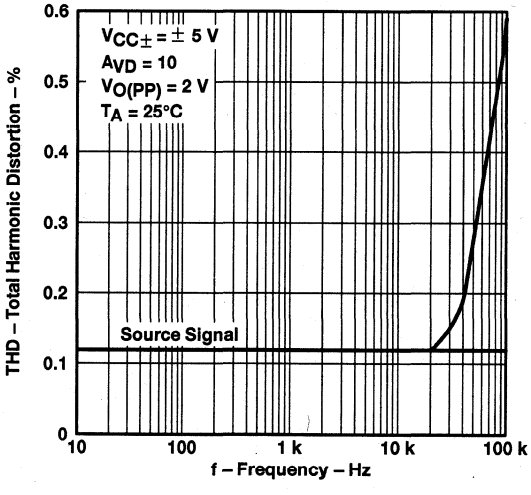

Figure 31

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

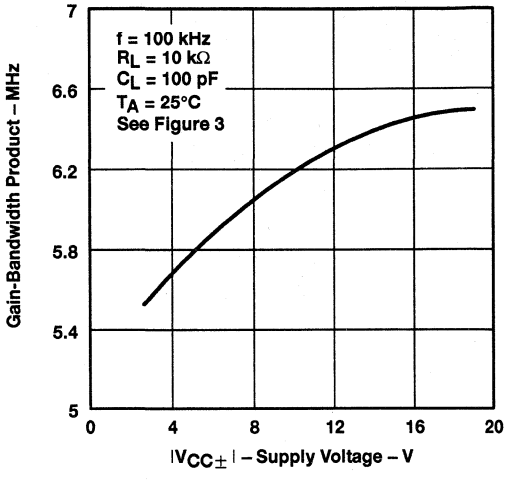

Figure 32

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

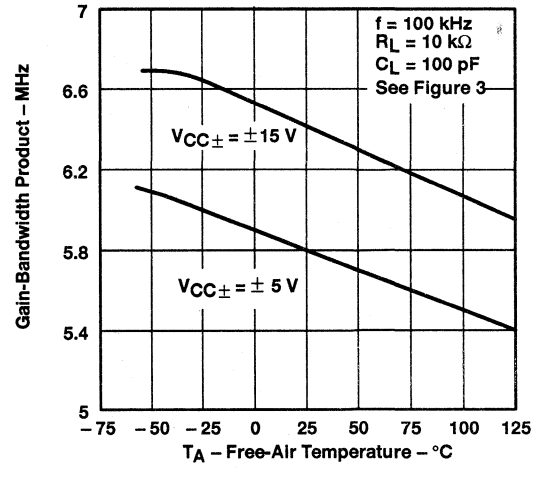

Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

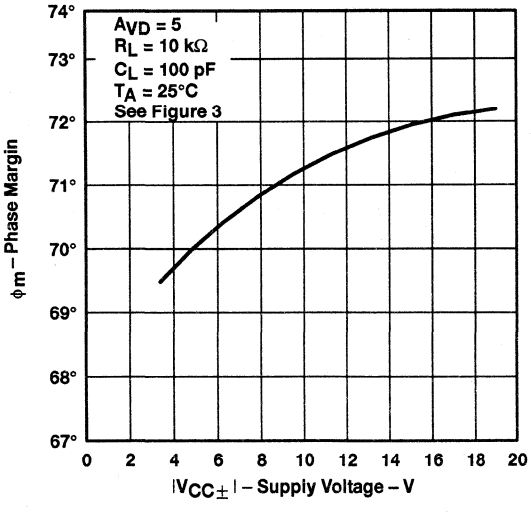

Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

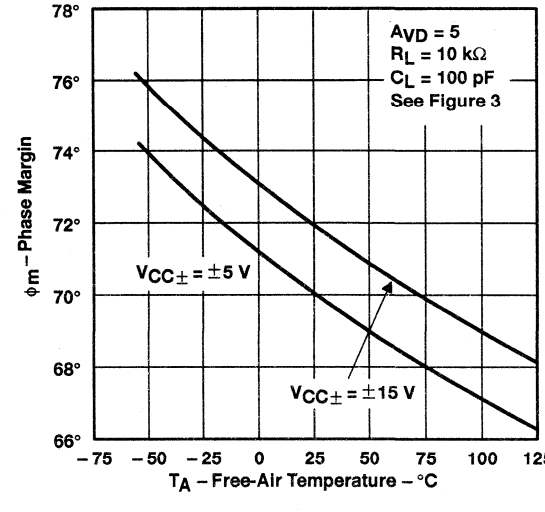

Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figures 36 and 37 were generated using the TLE2161 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

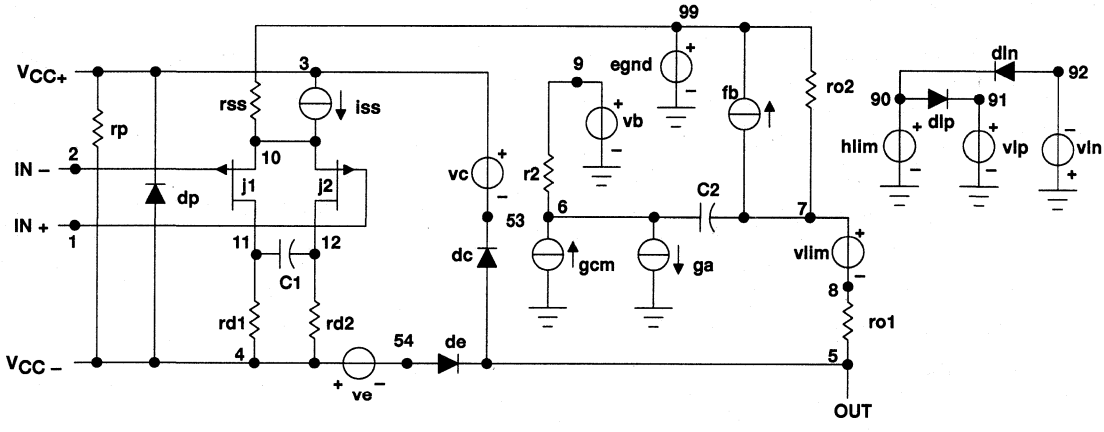

Figure 36. Boyle Macromodel

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2161 1 2 3 4 5
 c1    11  12  125.4E-14
 c2     6   7  5.000E-12
 dc     5  53  dx
 de    54  5d  x
 dlp   90  91  dx
 dln   92  90  dx
 dp     4   3  dx
 egnd  99   0  poly(2) (3,0) (4,0) 0 .5 .5
 fb     7  99  poly(5) vb vc ve vlp vln 0 4.085E6 -4E6 4E6 4E6 -4E6
 ga     6   0  11 12 201.1E-6
 gcm    0   6  10 99 3.576E-9
 iss    3  10  dc 45.00E-6
 hlim  90   0  vlim 1K
 j1    11   2  10 jx
 j2    12   1  10 jx
 r2     6   9  100.0E3
 rd1    4  11  4.973E3
 rd2    4  12  4.973E3
 ro1    8   5  280
 ro2    7  99  280
 rp     3   4  113.2E3
 rss   10  99  4.444E6
 vb     9   0  dc 0
 vc     3  53  dc 2
 ve    54   4  dc 2
 vlim   7   8  dc 0
 vlp   91   0  dc 50
 vln    0  92  dc 50
.model dx   D  (Is=800.0E-18)
.model jx PJF  (Is=1.000E-12 Beta=480E-6 Vto=-1)
.ends
```

Figure 37. Macromodel Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2161, TLE2161A and TLE2161B are specified with a minimum and a maximum input voltage that if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2161, TLE2161A, and TLE2161B are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

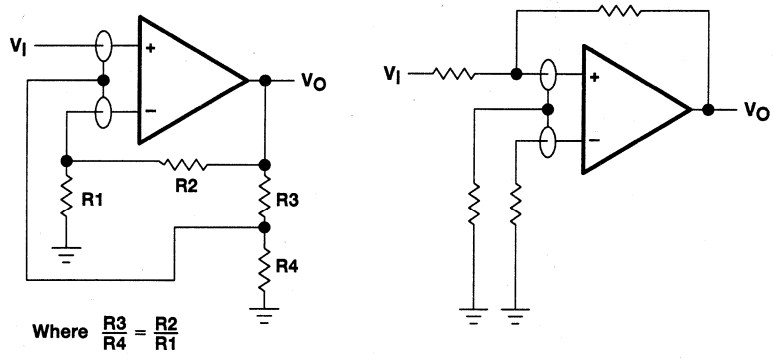


Figure 38. Use of Guard Rings

input offset voltage nulling

The TLE2161 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 39 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

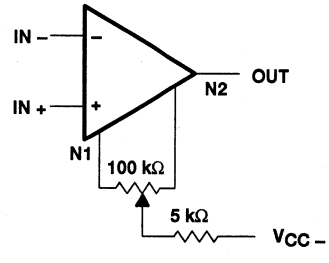


Figure 39. Input Offset Voltage Nulling

- **Outstanding Combination of DC Precision and AC Performance:**
  - **Unity-Gain Bandwidth . . . 15 MHz Typ**
  - **V_n . . . 3.3 nV/$\sqrt{Hz}$ at f = 10 Hz Typ, 2.5 nV/$\sqrt{Hz}$ at f = 1 kHz Typ**
  - **V_{IO} . . . 100 μV Typ**
  - **A_{VD} . . . 45 V/μV Typ With R_L = 2 kΩ, 38 V/μV Typ With R_L = 1 kΩ**
- **Available in 16-Pin Small-Outline Wide-Body Package**
- **Macromodels and Statistical Information Included**
- **Output Features Saturation Recovery Circuitry**

description

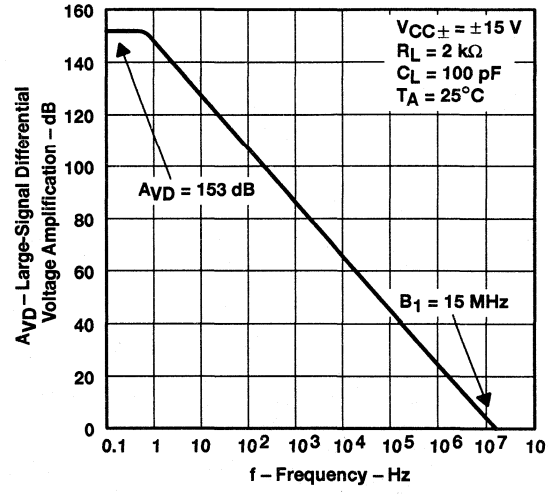
The TLE2227C combines innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in dual operational amplifiers. This device allows upgrades to systems that use lower-precision devices and is manufactured using Texas Instruments state-of-the-art Excalibur process.

In the area of dc precision, the TLE2227C offers a typical offset voltage of 100 μV, a common-mode rejection ratio of 115 dB (typ), a supply voltage rejection ratio of 120 dB (typ), and a dc gain of 45 V/μV (typ).

The ac performance is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/$\sqrt{Hz}$ and 2.5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz and 1 kHz, respectively.

The TLE2227C is available in a wide variety of packages, including the industry standard 16-pin small-outline wide-body version for high-density system applications. This device is characterized for operation from 0°C to 70°C.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

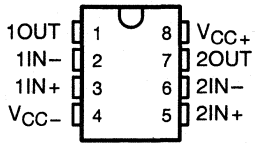


AVAILABLE OPTIONS

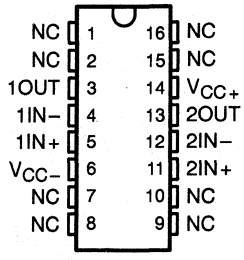
T_A	V_{IO}typ AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (DW)	PLASTIC DIP (P)	
0°C to 70°C	100 μV	TLE2227CDW	TLE2227CP	TLE2227Y

The DW package is available taped and reeled. Add R suffix to device type (e.g., TLE2227CDWR).

P PACKAGE
(TOP VIEW)

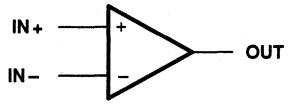


DW PACKAGE
(TOP VIEW)



NC – No internal connection

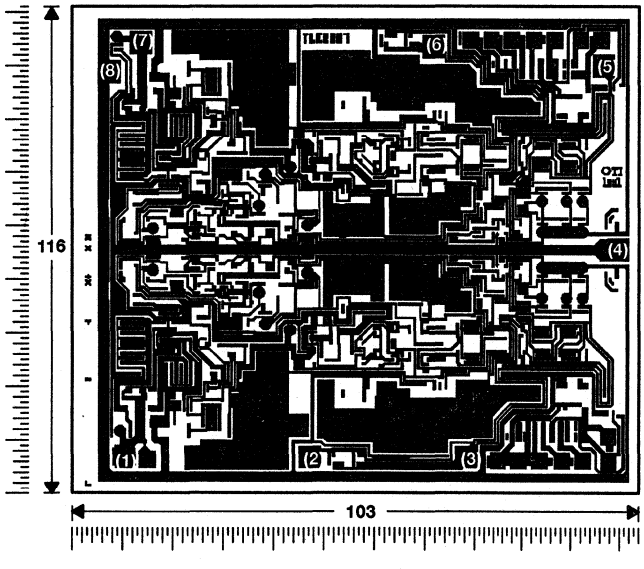
symbol (each amplifier)

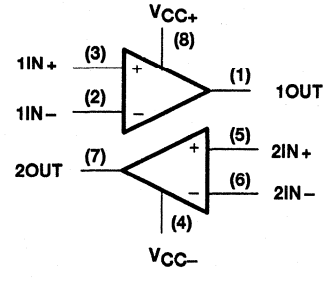


TLE2227Y chip information

This chip, properly assembled, displays characteristics similar to the TLE2227C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips my be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

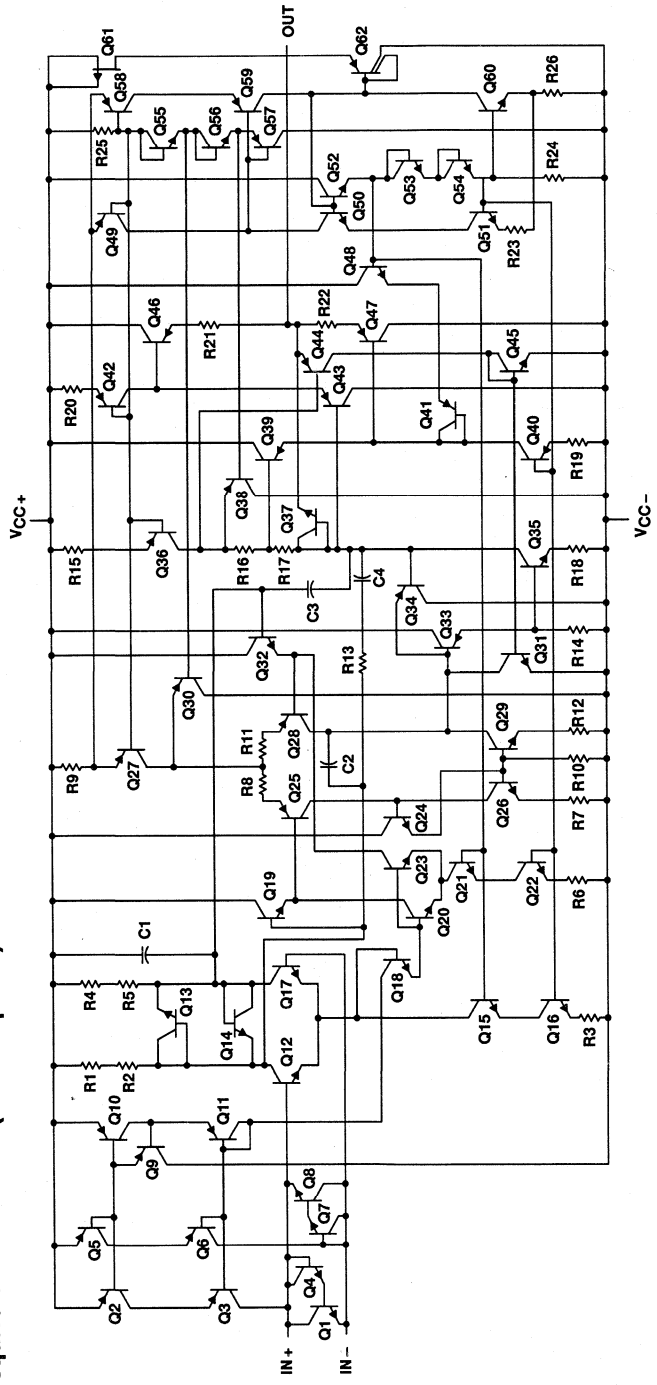
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	62
Diodes	0
Resistors	24
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} ..... −19 V
Differential input voltage, V_{ID} (see Note 2) ..... ±1.2 V
Input voltage range, V_I (any input) ..... $V_{CC\pm}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±50 mA
Total current into V_{CC+} ..... 50 mA
Total current out of,V_{CC-} ..... 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±4	±19	V
Common-mode input voltage, V_{IC}	T_A = 25°C		±11	V
	T_A = Full range†		±10.5	
Operating free-air temperature, T_A		0	70	°C

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2227C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		25°C		100	350	µV
				Full range			500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		0.4	1	µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.006	1	µV/mo
I_{IO}	Input offset current			25°C		7.5	90	nA
				Full range			150	
I_{IB}	Input bias current			25°C		15	90	nA
				Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−11 to 11	−13 to 13		V
				Full range	−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 1 kΩ		25°C	10.5			V
				Full range	10			
		R_L = 2 kΩ		25°C	12			
				Full range	11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 1 kΩ		25°C	−10.5	−13		V
				Full range	−10			
		R_L = 2 kΩ		25°C	−12	−13.5		
				Full range	−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V,	R_L = 2 kΩ	25°C	2.5	45		V/µV
		V_O = ±10 V,	R_L = 2 kΩ	Full range	2			
		V_O = ±10 V,	R_L = 1 kΩ	25°C	3.5	38		
				Full range	1			
c_i	Input capacitance			25°C		8		pF
z_o	Open-loop output impedance	I_O = 0		25°C		50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	98	115		dB
				Full range	95			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V,	R_S = 50 Ω	25°C	94	120		dB
		$V_{CC\pm}$ = ±4 V to ±18 V,	R_S = 50 Ω	Full range	92			
I_{CC}	Supply current	V_O = 0,	No load	25°C		7.3	10.6	mA
				Full range			11.2	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2227C			UNIT
				MIN	TYP	MAX	
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF	25°C	1.7	2.5		V/μs
			Full range	1.2			
V_n	Equivalent input noise voltage	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 1, See Note 5	25°C		<0.002%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF	25°C	7	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		30		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		40°		

† Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis is 0.002%.

electrical characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

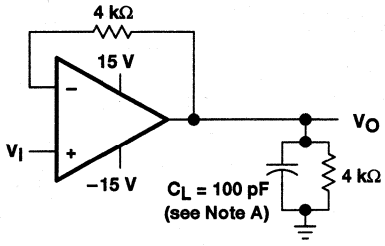
PARAMETER		TEST CONDITIONS	TLE2227Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		100	350	μV
	Input offset voltage long-term drift (see Note 4)			0.006	1	μV/mo
I_{IO}	Input offset current			7.5	90	nA
I_{IB}	Input bias current			15	90	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	−11 to 11	−13 to 13		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 1 kΩ	10.5			V
		R_L = 2 kΩ	12			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 1 kΩ	−10.5	−13		V
		R_L = 2 kΩ	−12	−13.5		
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	2.5	45		V/μV
		V_O = ±10 V, R_L = 1 kΩ	3.5	38		
c_i	Input capacitance			8		pF
z_o	Open-loop output impedance	I_O = 0		50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	98	115		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	94	120		dB
I_{CC}	Supply current	V_O = 0, No load		7.3	10.6	mA

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLE2227Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF	1.7	2.5		V/μs
V_n	Equivalent input noise voltage	R_S = 20 Ω, f = 10 Hz		3.3	8	nV/√Hz
		R_S = 20 Ω, f = 1 kHz		2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		50	250	nV
I_n	Equivalent input noise current	f = 10 Hz		1.5	4	pA/√Hz
		f = 1 kHz		0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 1, See Note 5		<0.002%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF	7	13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ		30		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF		40°		

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5 Measured distortion of the source used in the analysis is 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

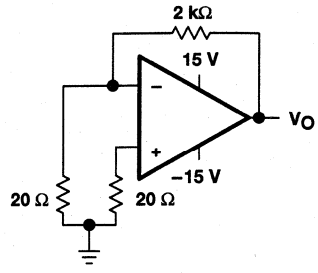
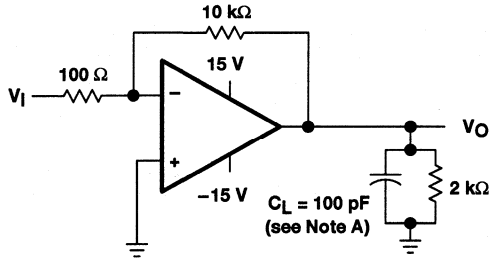
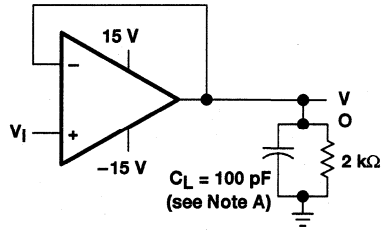


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
ΔV_{IO}	Input offset voltage change	vs Time after power on	6, 7
I_{IO}	Input offset current	vs Free-air temperature	8
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	9 10
I_I	Input current	vs Differential input voltage	11
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	12
V_{OM}	Maximum peak output voltage	vs Load resistance vs Free-air temperature	13, 14 15, 16
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	17 19 18, 20 21
z_o	Output impedance	vs Frequency	22
CMRR	Common-mode rejection ratio	vs Frequency	23
k_{SVR}	Supply voltage rejection ratio	vs Frequency	24
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	25, 26 27, 28 29, 30
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	31 32
	Pulse response	Small signal Large signal	33 34
V_n	Equivalent input noise voltage	vs Frequency	35
	Noise voltage (referred to input)	vs Time	36
B_1	Unity-gain bandwidth	vs Supply voltage vs Load capacitance	37 38
SR	Slew rate	vs Free-air temperature	39
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance	40 41
	Phase shift	vs Frequency	18, 20

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF
INPUT OFFSET VOLTAGE

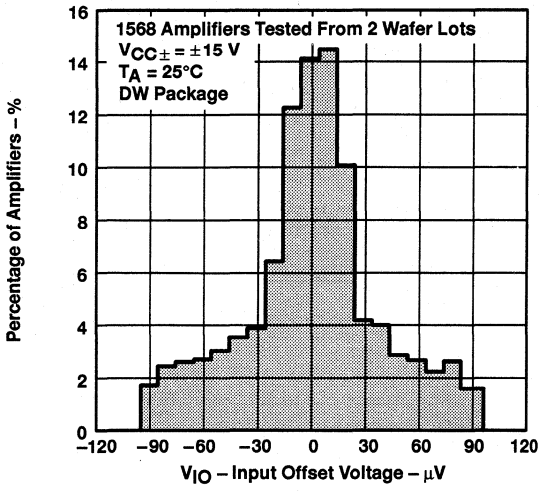


Figure 5

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

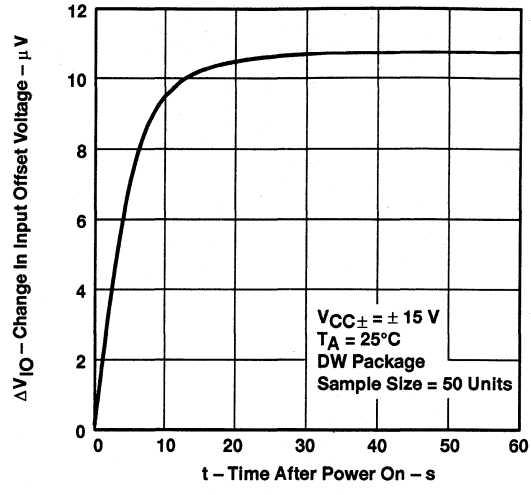


Figure 6

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

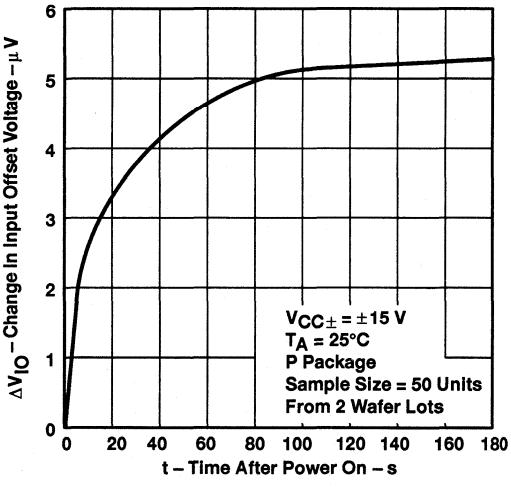


Figure 7

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

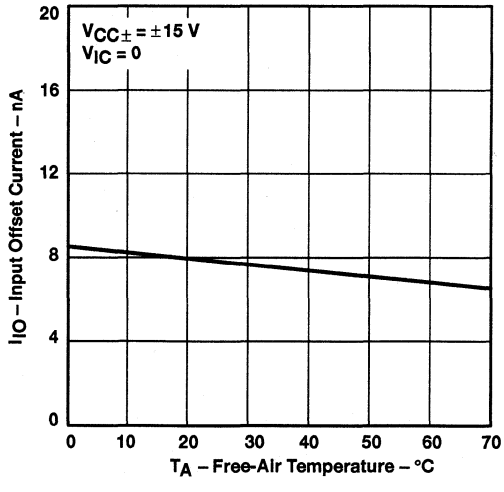


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

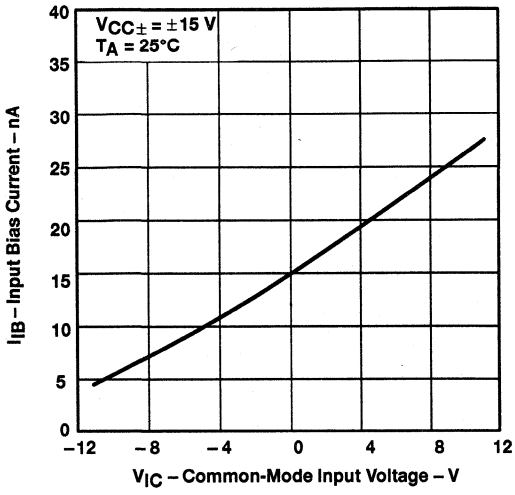


Figure 9

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

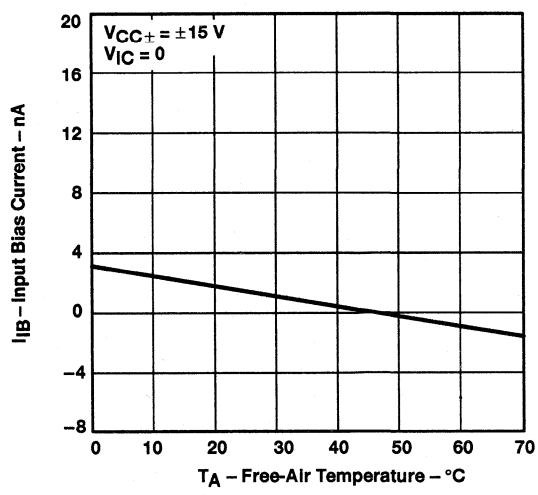


Figure 10

INPUT CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

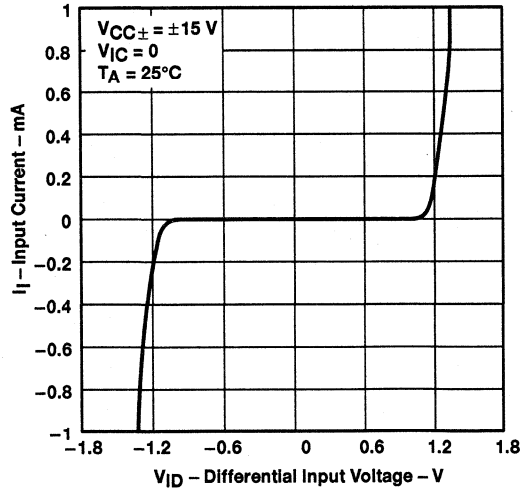


Figure 11

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

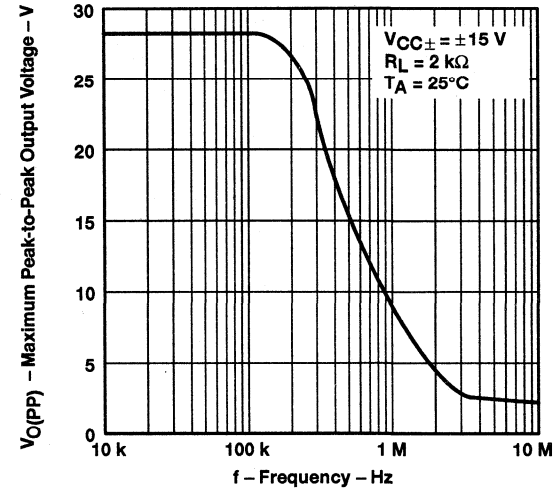


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

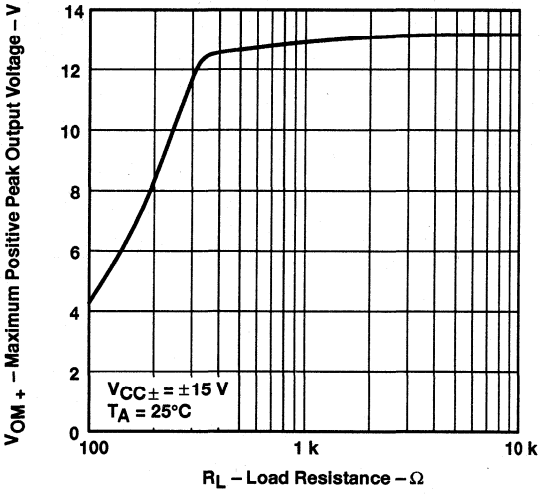


Figure 13

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

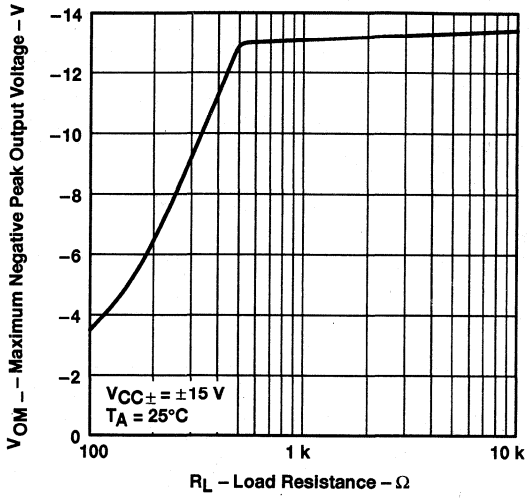


Figure 14

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

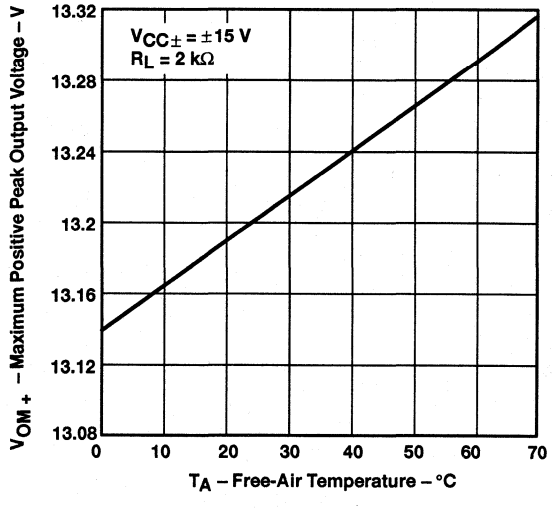


Figure 15

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

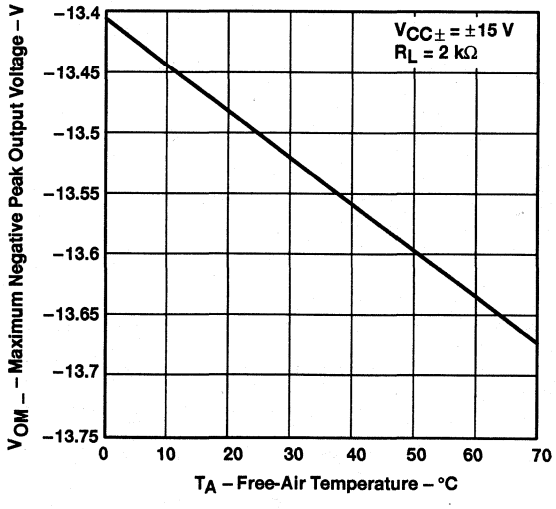


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

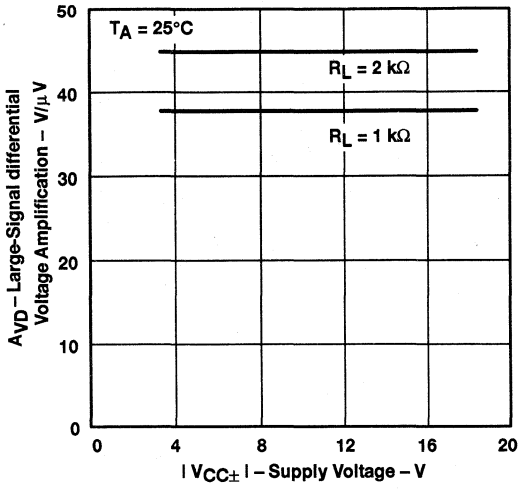


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

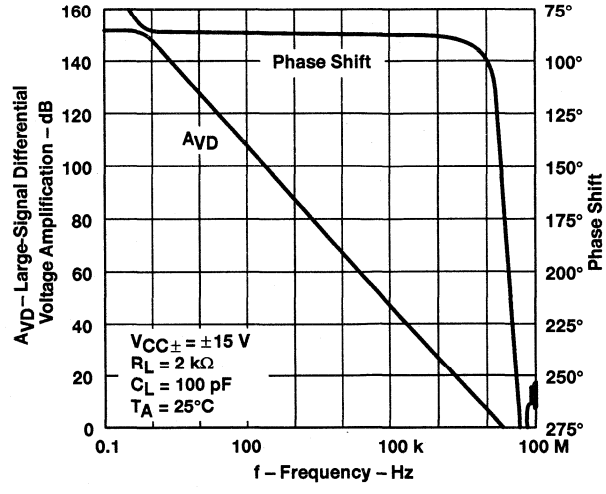


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

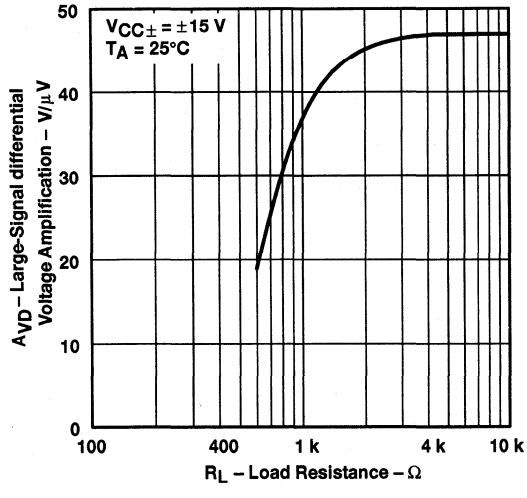


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

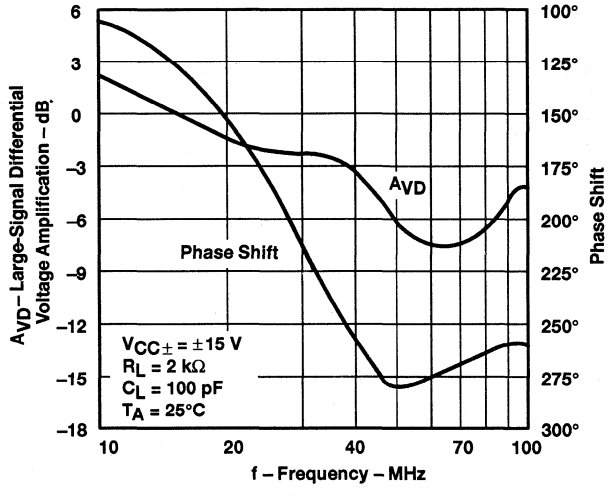


Figure 20

TYPICAL CHARACTERISTICS†

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

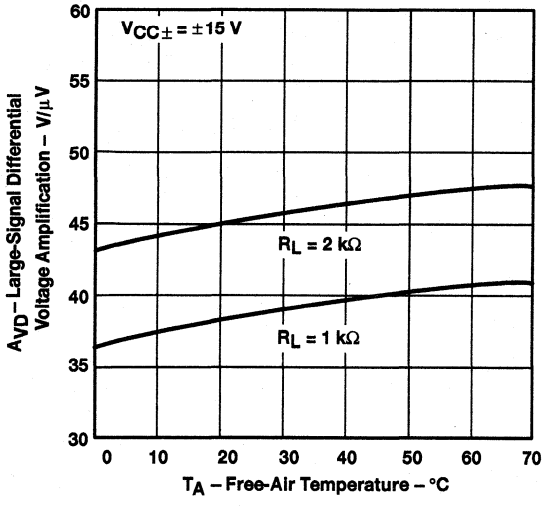


Figure 21

OUTPUT IMPEDANCE vs FREQUENCY

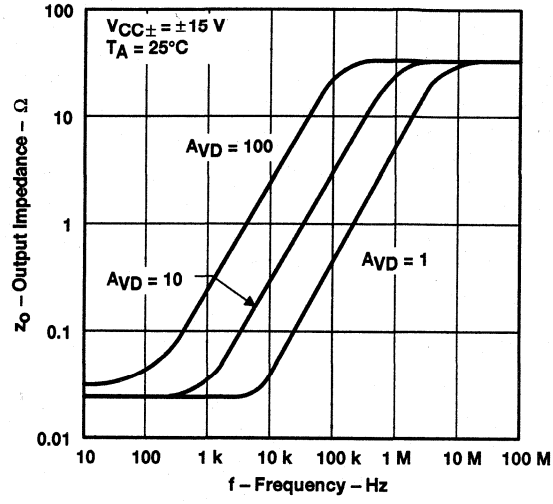


Figure 22

COMMON-MODE REJECTION RATIO vs FREQUENCY

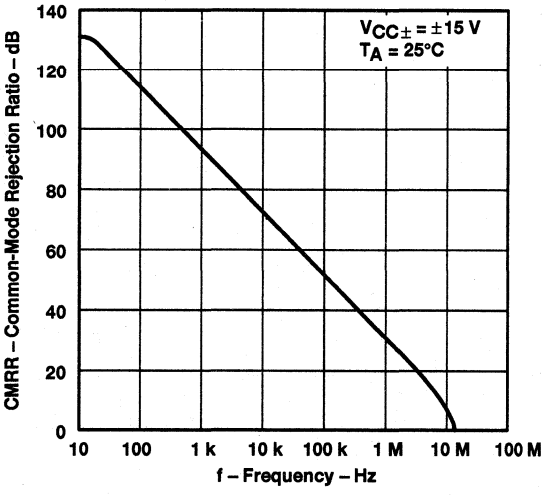


Figure 23

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

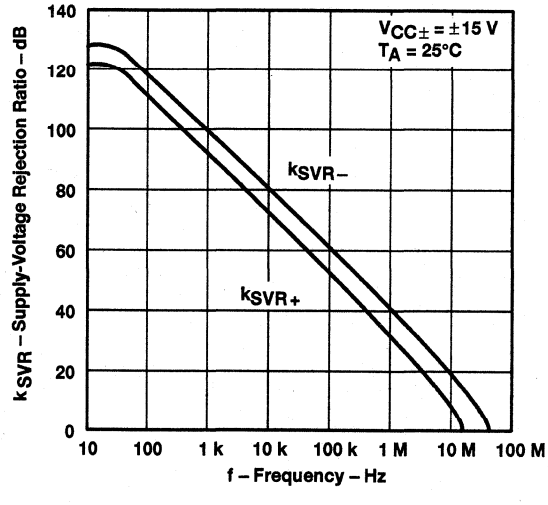


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

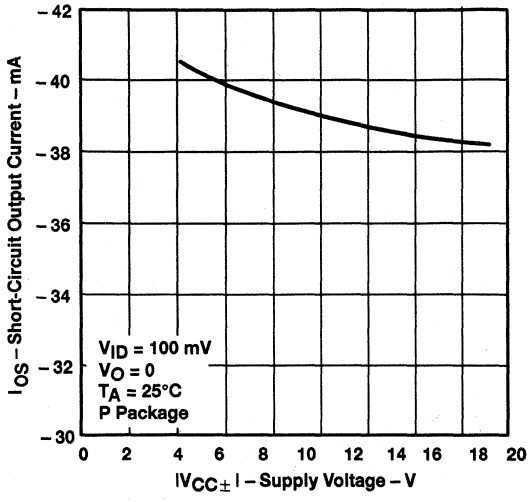


Figure 25

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

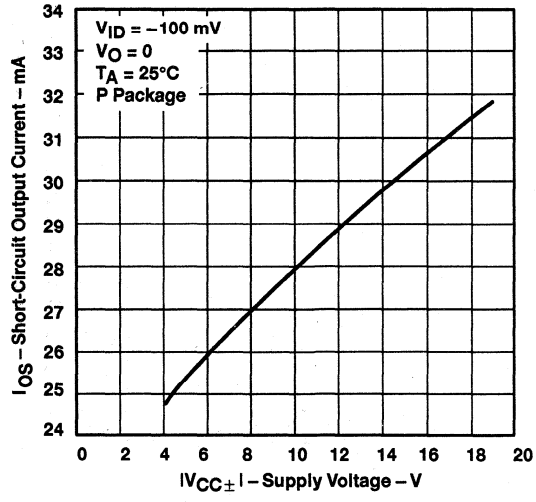


Figure 26

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

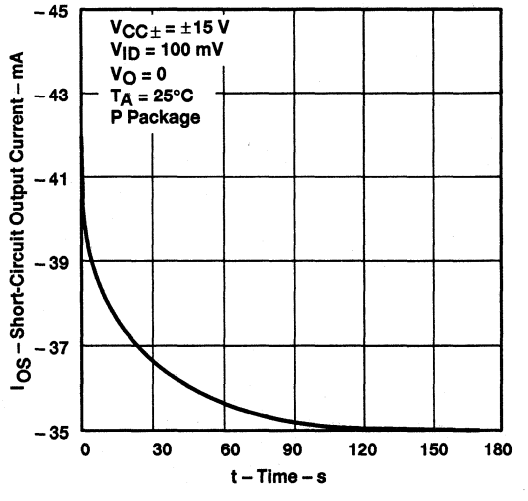


Figure 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

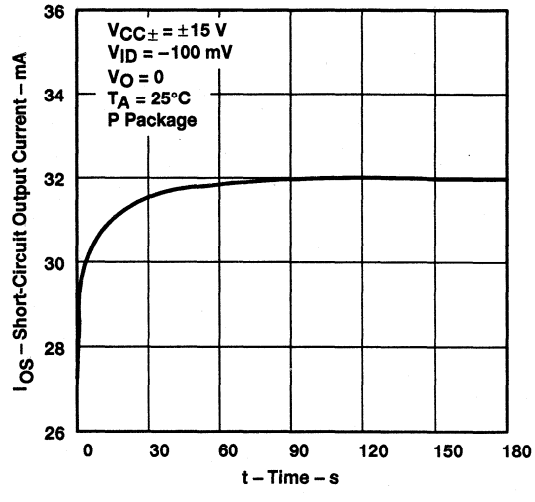


Figure 28

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

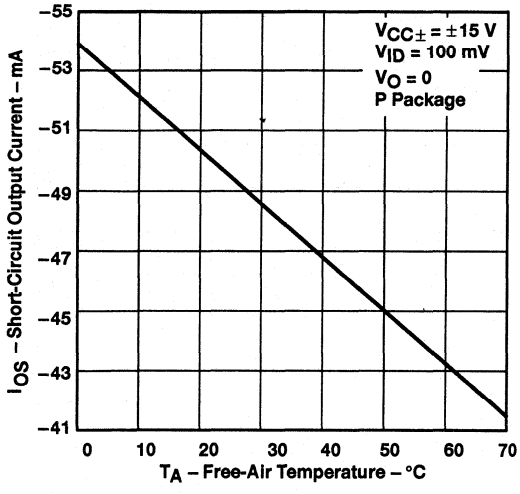


Figure 29

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

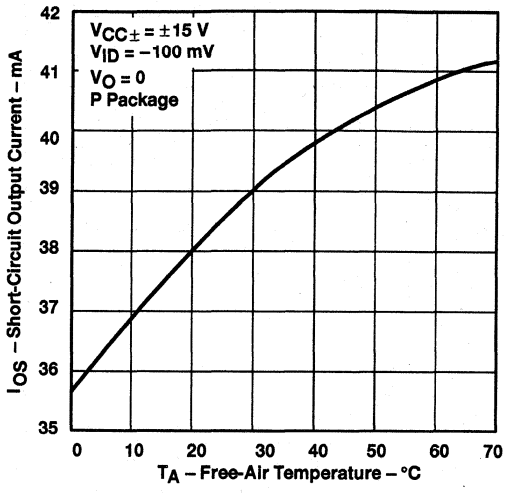


Figure 30

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

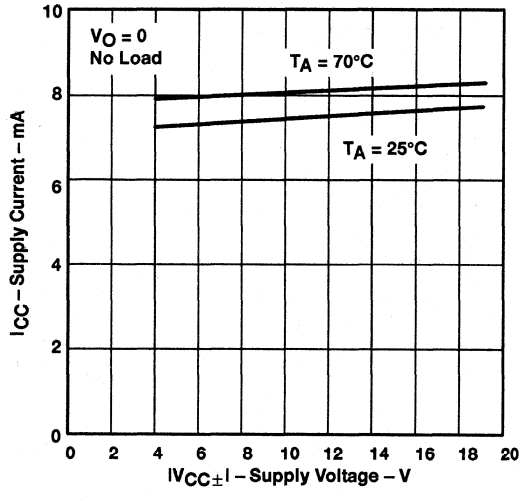


Figure 31

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

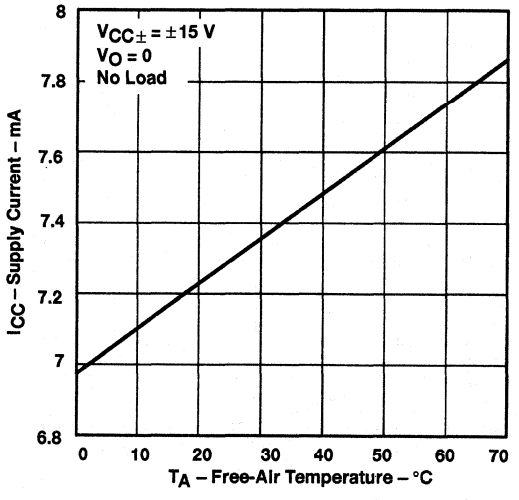


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

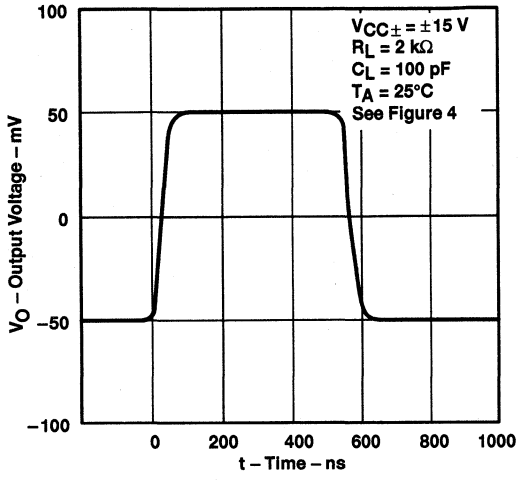


Figure 33

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

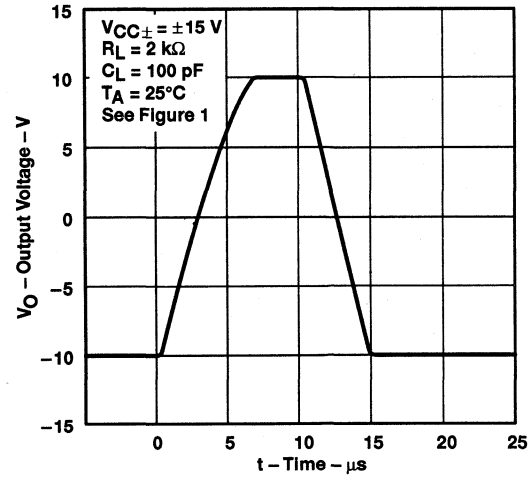


Figure 34

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

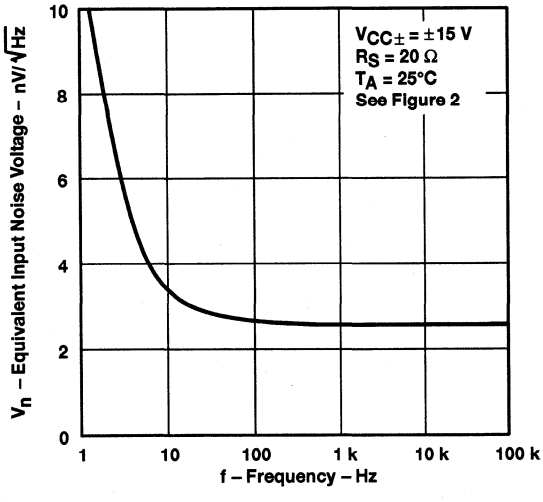


Figure 35

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

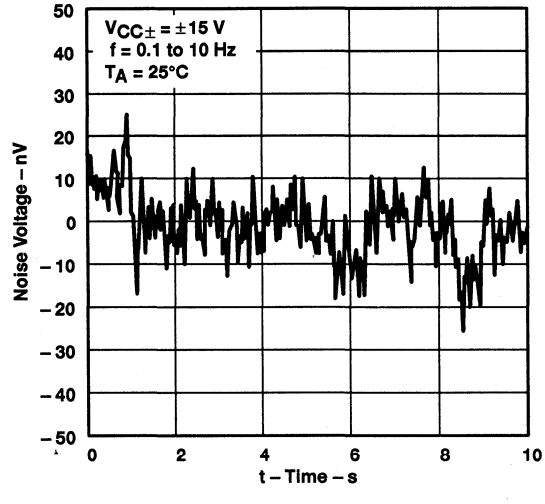


Figure 36

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

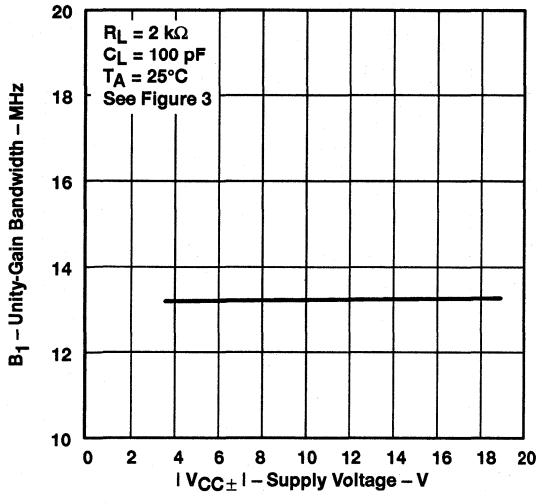


Figure 37

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

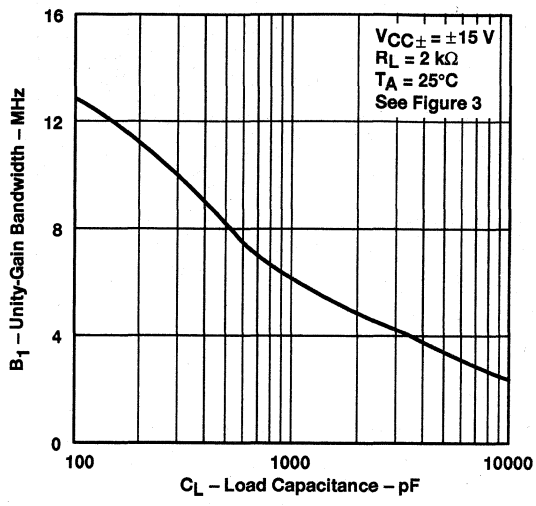


Figure 38

SLEW RATE vs FREE-AIR TEMPERATURE

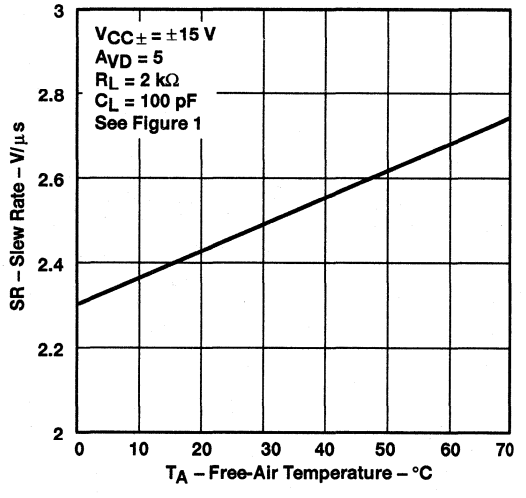


Figure 39

PHASE MARGIN vs SUPPLY VOLTAGE

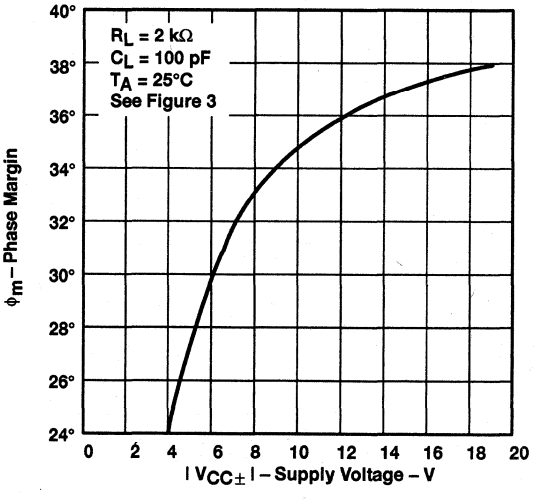


Figure 40

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

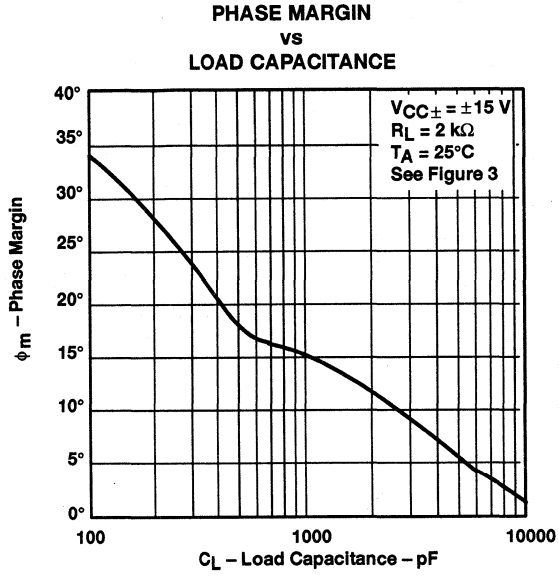


Figure 41

APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 42 and 43 are generated using the TLE2227C typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain bandwidth
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)

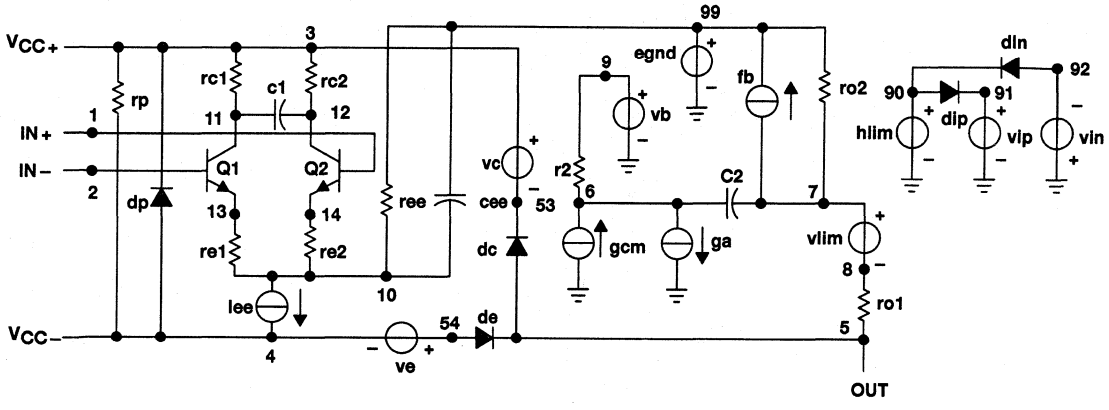


Figure 42. Boyle Macromodel

```
.subckt TLE2227  1   2   3   4   5
*
  c1     11    12  4.003E-12
  c2      6     7  20.00E-12
  dc      5    53  dx
  de     54     5  dx
  dlp    90    91  dx
  dln    92    90  dx
  dp      4     3  dx
  egnd   99     0  poly(2)   (3,0)  (4,0)  0   .5  .5
  fb      7    99  poly(5)   vb  vc  ve  vlp   vln    0   954.8E6   -1E9   1E9    1E9-1E9
  ga      6     0  11  12  2.062E-3
  gcm     0     6  10  99  531.3E-12
  iee    10     4  dc  56.01E-6
  hlim   90     0  vlim   1K
  ql     11     2  13  qx
  q2     12     1  14  qx
  r2      6     9  100.0E3
  rc1     3    11  530.5
  rc2     3    12  530.5
  rel    13    10  -393.2
  re2    14    10  -393.2
  ree    10    99  3.571E6
  ro1     8     5  25
  ro2     7    99  25
  rp      3     4  8.013E3
  vb      9     0  dc  0
  vc      3    53  dc  2.400
  ve     54     4  dc  2.100
  vlim    7     8  dc  0
  vlp    91     0  dc  40
  vln     0    92  dc  40
.model   dx D(Is=800.0E-18)
.model   qx NPN(Is=800.0E-18   Bf=7.000E3)
.ends
```

Figure 43. Macromodel Subcircuit

APPLICATION INFORMATION

voltage-follower applications

The TLE2227C circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. A feedback resistor is recommended to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 44).

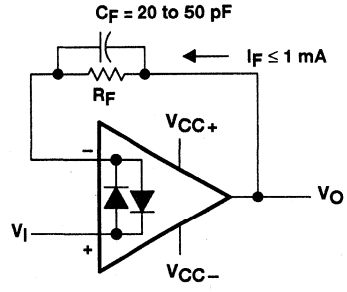
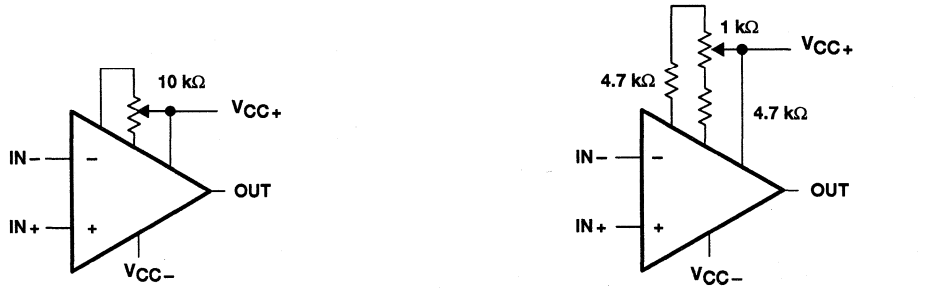


Figure 44. Voltage-Follower Circuit

input offset voltage nulling

The TLE2227C offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 45 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins can be left disconnected.



(a) STANDARD ADJUSTMENT

(b) ADJUSTMENT WITH IMPROVED SENSITIVITY

Figure 45. Input Offset Voltage Nulling Circuits

- **Outstanding Combination of DC Precision and AC Performance:**
  - **Gain Bandwidth-Product . . . 50 MHz Typ**
  - **V_n . . . 3.3 nV/$\sqrt{Hz}$ at f = 10 Hz Typ, 2.5 nV/$\sqrt{Hz}$ at f = 1 kHz Typ**
  - **V_{IO} . . . 25 μV Typ**
  - **A_{VD} . . . 45 V/μV Typ With R_L = 2 kΩ, 38 V/μV Typ With R_L = 1 kΩ**
- **Available in 16-Pin Small-Outline Wide-Body Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical Information Included**

description

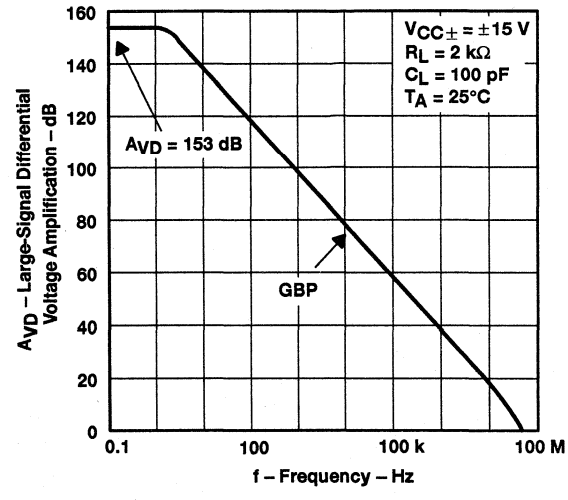
The TLE2237 combines innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in dual operational amplifiers. Using the Texas Instruments state-of-the-art Excalibur process, this device allows upgrades to systems that use lower-precision devices.

The TLE2237 is the noncompensated version of the TLE2027. The device is stable to a closed-loop gain of five. In the area of dc precision, the device offers an input offset voltage of 100 μV (typ), a common-mode rejection ratio of 115 dB (typ), a supply voltage rejection ratio of 120 dB (typ), and a dc gain of 45 V/μV (typ).

The ac performance is highlighted by a typical gain-bandwidth product specification of 50 MHz, 50° of phase margin, and noise voltage specifications of 3.3 nV/$\sqrt{Hz}$ and 2.5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz and 1 kHz, respectively.

The TLE2237 is available in a wide variety of packages, including the industry standard 16-pin small-outline wide-body version for high-density system applications. The device is characterized for operation from 0°C to 70°C.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

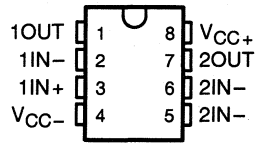


AVAILABLE OPTIONS

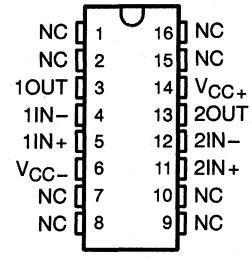
T_A	V_{IO}typ AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL-OUTLINE (DW)	PLASTIC DIP (P)	
0°C to 70°C	100 μV	TLE2237CDW	TLE2237CP	TLE2237Y

The DW package is available taped and reeled. Add R suffix to device type (e.g., TLE2237CDWR).

P PACKAGE
(TOP VIEW)

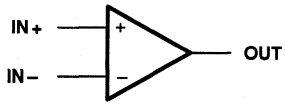


DW PACKAGE
(TOP VIEW)



NC – No internal connection

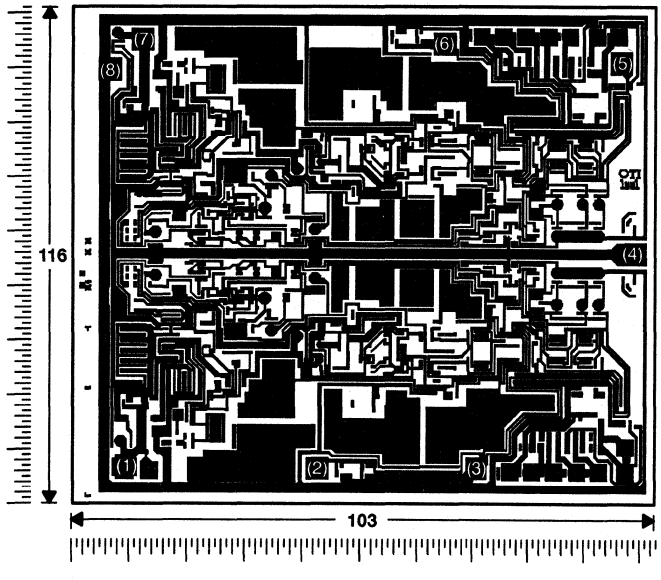
symbol (each amplifier)

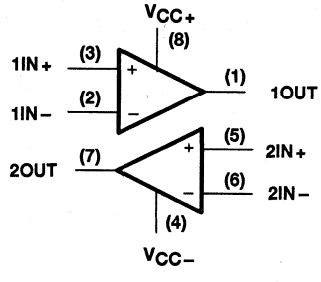


TLE2237Y chip information

This chip, when properly assembled, display characteristics similar to TLE2237. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

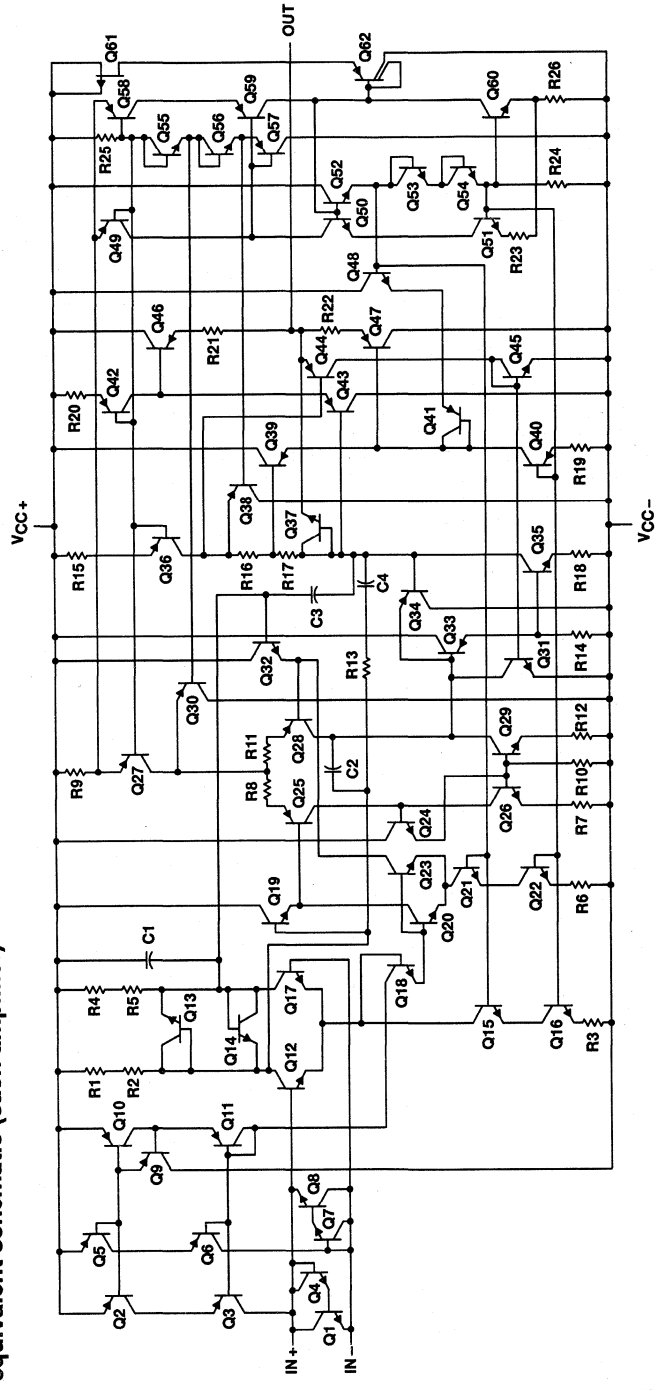
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	62
Diodes	4
Resistors	24
Capacitors	0

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 19 V
Supply voltage, V_{CC-} ..... −19 V
Differential input voltage, V_{ID} (see Note 2) ..... ±1.2 V
Input voltage range, V_I (any input) ..... $V_{CC\pm}$
Input current, I_I (each input) ..... ±1 mA
Output current, I_O ..... ±50 mA
Total current into V_{CC+} ..... 50 mA
Total current out of V_{CC-} ..... 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to the IN−. Excessive current flows if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs unless some limiting resistance is used.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±4	±22	V
Common-mode input voltage, V_{IC}	$T_A = 25°C$	−11	11	V
	T_A = Full range†	−10.5	10.5	
Operating free-air temperature, T_A		0	70	°C

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2237C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	350	μV
α_{VIO}	Temperature coefficient of input offset voltage		Full range			500	μV/°C
	Input offset voltage long-term drift (see Note 4)		Full range		0.4	1	
			25°C		0.006	1	μV/mo
I_{IO}	Input offset current		25°C		7.5	90	nA
			Full range			150	
I_{IB}	Input bias current		25°C		15	90	nA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	−11 to 11	−13 to 13		V
			Full range	−10.5 to 10.5			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 1 kΩ	25°C	10.5			V
			Full range	10			
		R_L = 2 kΩ	25°C	12			
			Full range	11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 1 kΩ	25°C	−10.5	−13		V
			Full range	−10			
		R_L = 2 kΩ	25°C	−12	−13.5		
			Full range	−11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11V, R_L = 2 kΩ	25°C	2.5	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		
			Full range	1			
c_i	Input capacitance		25°C		8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	98	115		dB
			Full range	95			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	120		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	92			
I_{CC}	Supply current	V_O = 0, No load	25°C		7.3	10.6	mA
			Full range			11.2	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2237C			UNIT
				MIN	TYP	MAX	
SR	Slew rate	A_{VD} = 5, RL = 2 kΩ, C_L = 100 pF	25°C	4	5		V/μs
			Full range	3			
V_n	Equivalent input noise voltage	R_S = 20 Ω, f = 10 Hz	25°C		3.3	8	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		50	250	nV
I_n	Equivalent input noise current	f = 10 Hz	25°C		1.5	4	pA/√Hz
		f = 1 kHz			0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 5 V, See Note 5	25°C		<0.002%		
GBP	Gain-bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ	25°C		80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF	25°C		40°		

† Full range is 0°C to 70°C.

NOTE 5: Measured distortion of the source used in the analysis was 0.002%.

electrical characteristics at specified free-air temperature $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLE2237Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω		100	350	μV
	Input offset voltage long-term drift (see Note 4)			0.006	1	μV/mo
I_{IO}	Input offset current			7.5	90	nA
I_{IB}	Input bias current			15	90	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	−11 to 11	−13 to 13		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 1 kΩ	10.5			V
		R_L = 2 kΩ	12			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 1 kΩ	−10.5	−13		V
		R_L = 2 kΩ	−12	−13.5		
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	2.5	45		V/μV
		V_O = ±10 V, R_L = 1 kΩ	3.5	38		
c_i	Input capacitance			8		pF
z_o	Open-loop output impedance	I_O = 0		50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	98	115		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	94	120		dB
I_{CC}	Supply current	V_O = 0, No load		7.3	10.6	mA

operating characteristics at specified free-air temperature $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	TLE2237Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF	4	5		V/μs
V_n	Equivalent input noise voltage	R_S = 20 Ω, f = 10 Hz		3.3	8	nV/√Hz
		R_S = 20 Ω, f = 1 kHz		2.5	4.5	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		50	250	nV
I_n	Equivalent input noise current	f = 10 Hz		1.5	4	pA/√Hz
		f = 1 kHz		0.4	0.6	
THD	Total harmonic distortion	V_O = ±10 V, A_{VD} = 1, See Note 5		<0.002%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF	35	50		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ		80		kHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 100 pF		40°		

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
5 Measured distortion of the source used in the analysis is 0.002%.

PARAMETER MEASUREMENT INFORMATION

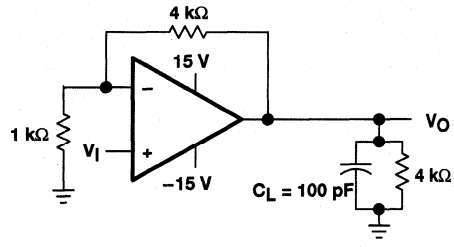


Figure 1. Slew-Rate Test Circuit

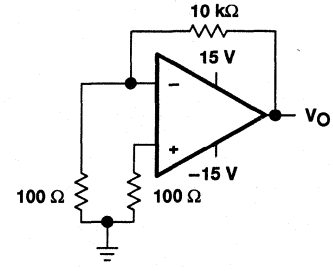


Figure 2. Noise-Voltage Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

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ΔV_{IO}	Input offset voltage change	vs Time after power on	4, 5
I_{IO}	Input offset current	vs Free-air temperature	6
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	7 8
I_I	Input current	vs Differential input voltage	9
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	10
V_{OM}	Maximum peak output voltage	vs Load resistance vs Free-air temperature	11, 12 13, 14
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Load resistance vs Frequency vs Free-air temperature	15 17 16, 18 19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
k_{SVR}	Supply voltage rejection ratio	vs Frequency	22
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	23, 24 25, 26 27, 28
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	Pulse response	Small signal Large signal	31 32
V_n	Equivalent input noise voltage	vs Frequency	33
	Noise voltage (referred to input)	vs Time	34
B_1	Unity-gain bandwidth	vs Supply voltage vs Load capacitance	35 36
SR	Slew rate	vs Free-air temperature	37
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance	38 39
	Phase shift	vs Frequency	16, 18

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

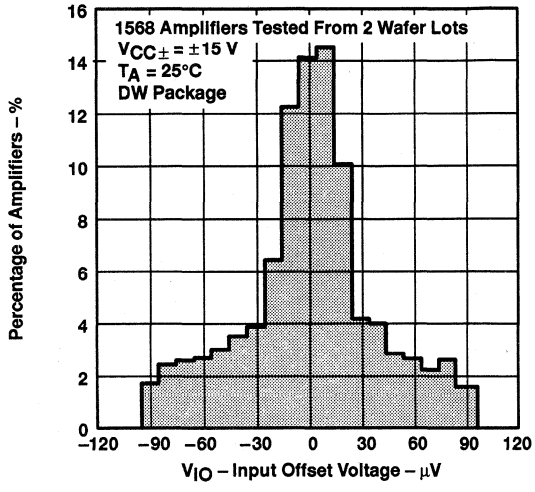

Figure 3

INPUT OFFSET VOLTAGE CHANGE vs TIME AFTER POWER ON

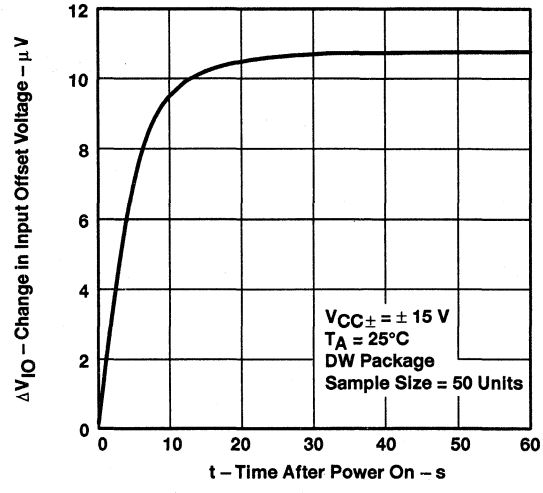

Figure 4

INPUT OFFSET VOLTAGE CHANGE vs TIME AFTER POWER ON

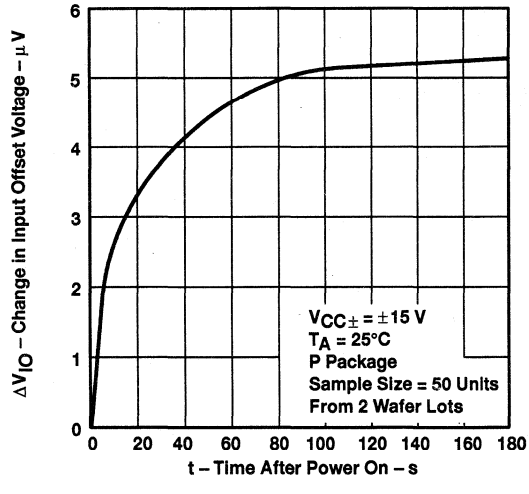

Figure 5

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

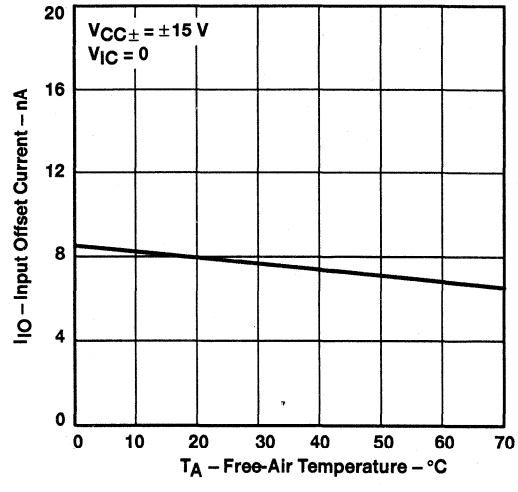

Figure 6

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

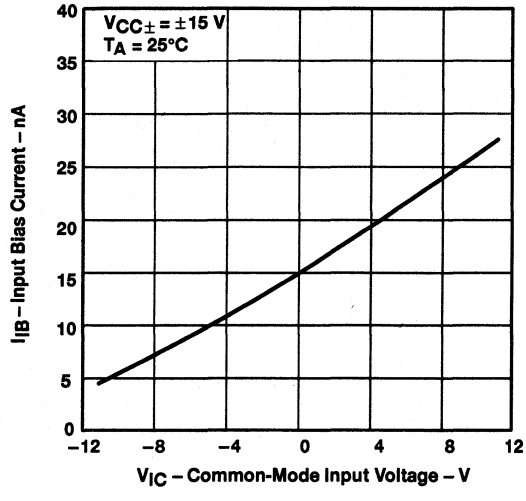

Figure 7

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

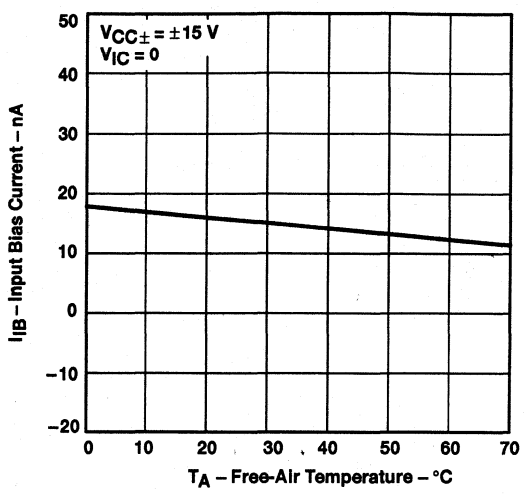

Figure 8

INPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

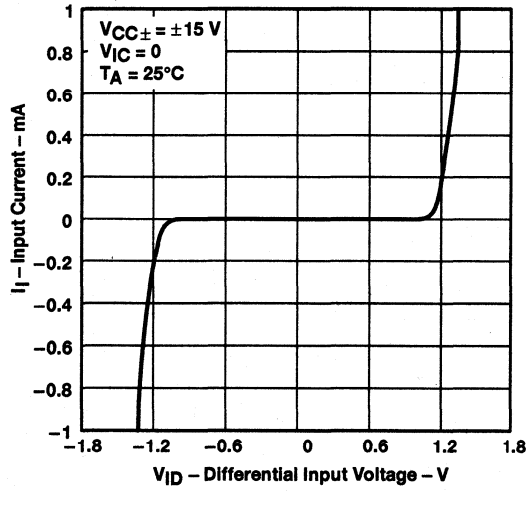

Figure 9

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

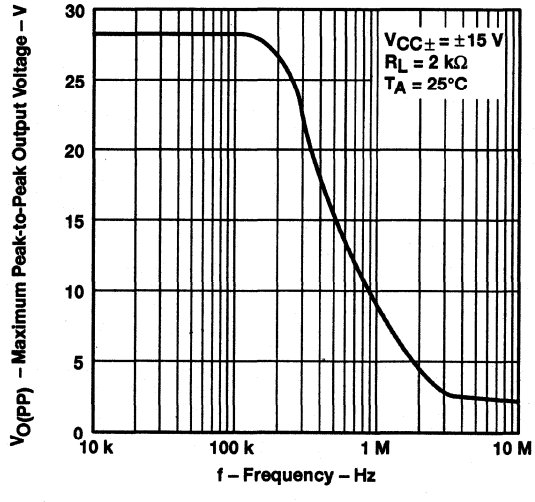

Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

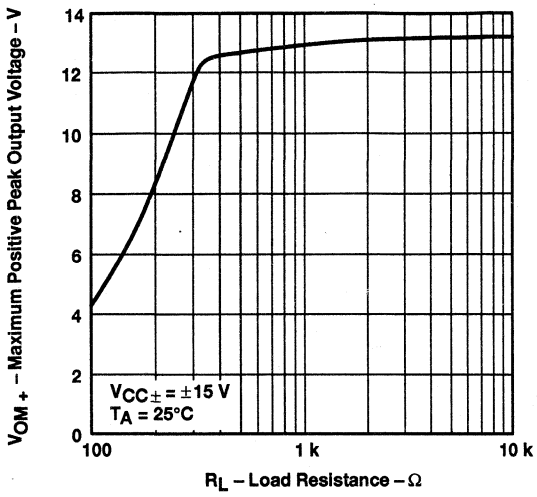

Figure 11

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

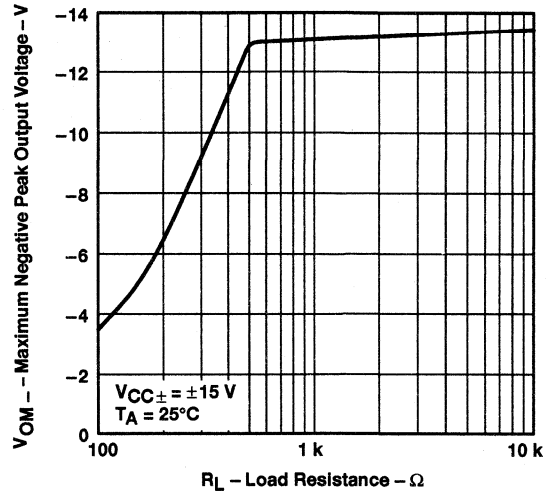

Figure 12

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

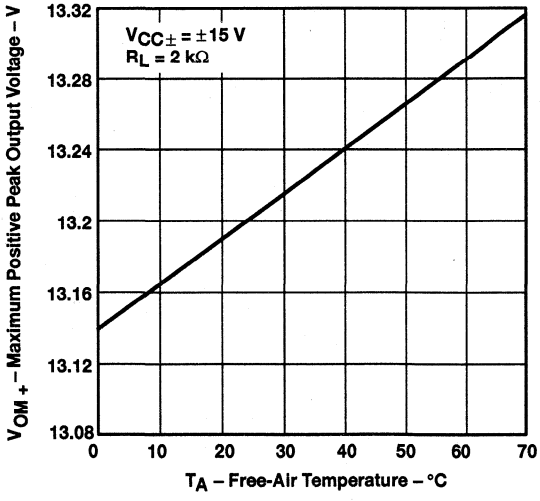

Figure 13

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

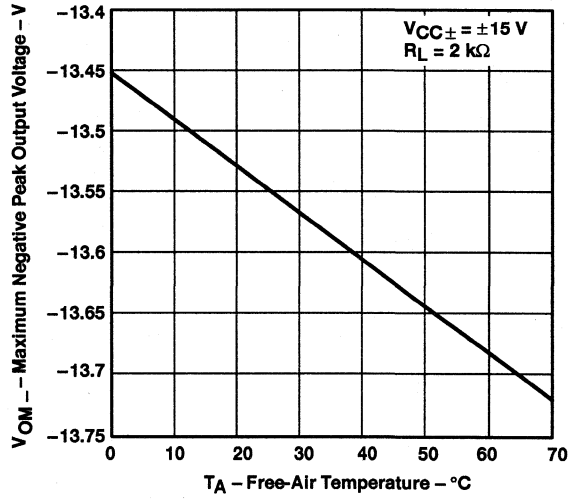

Figure 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

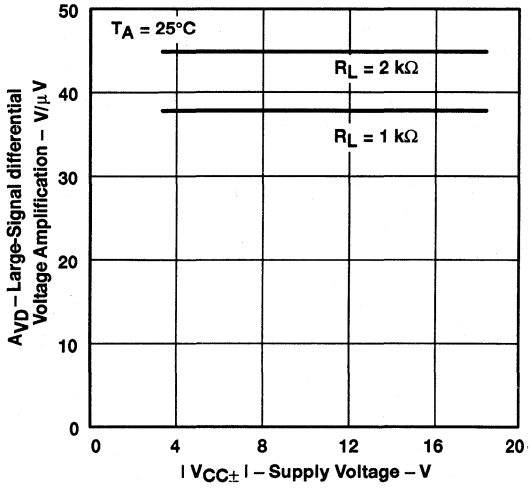

Figure 15

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

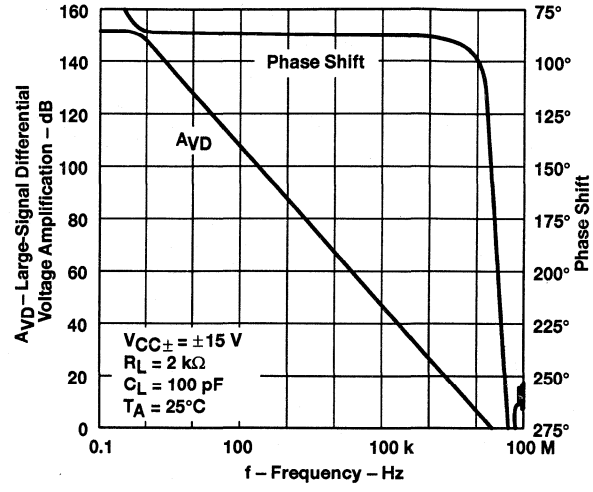

Figure 16

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

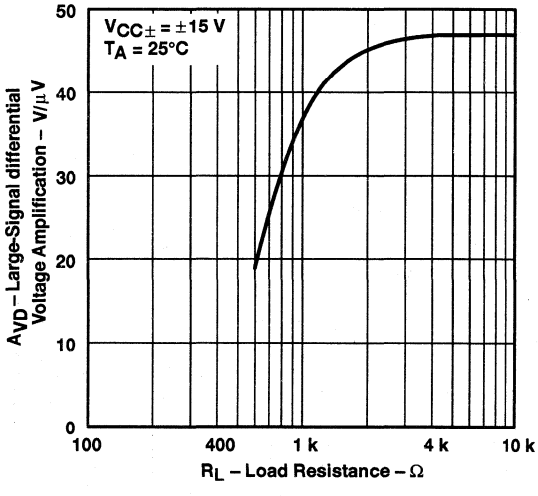

Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

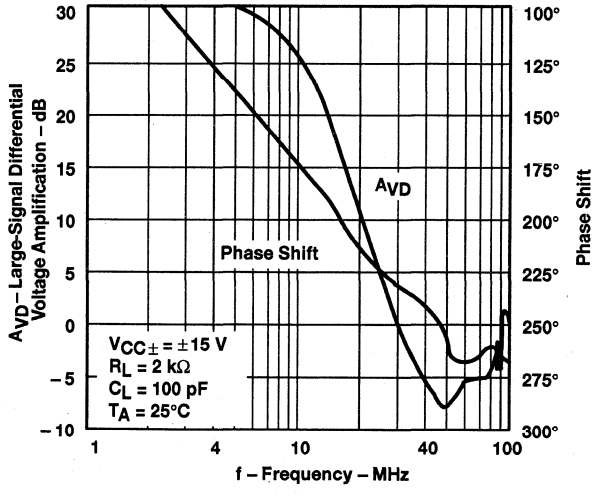

Figure 18

TYPICAL CHARACTERISTICS†

LARGE-SCALE DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

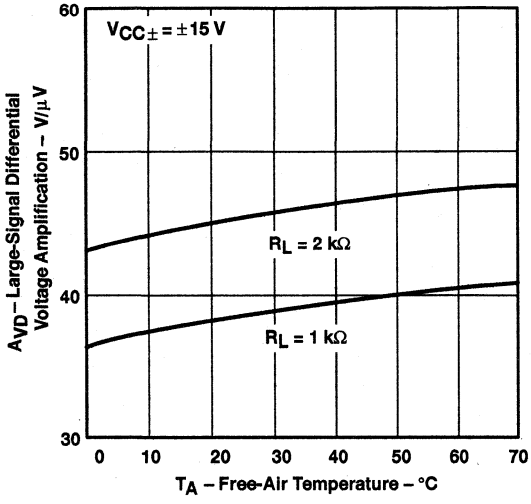

Figure 19

OUTPUT IMPEDANCE vs FREQUENCY

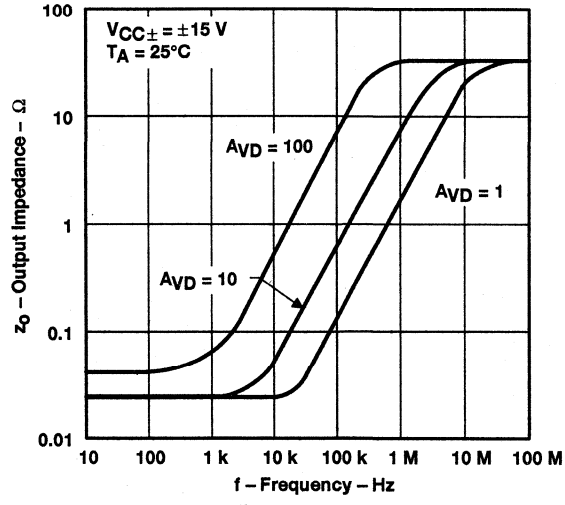

Figure 20

COMMON-MODE REJECTION RATIO vs FREQUENCY

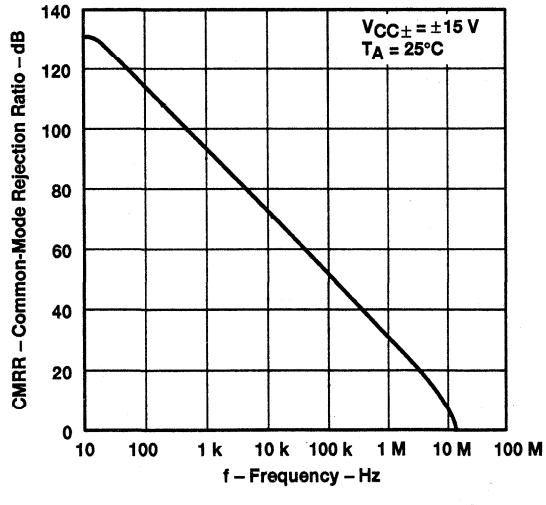

Figure 21

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

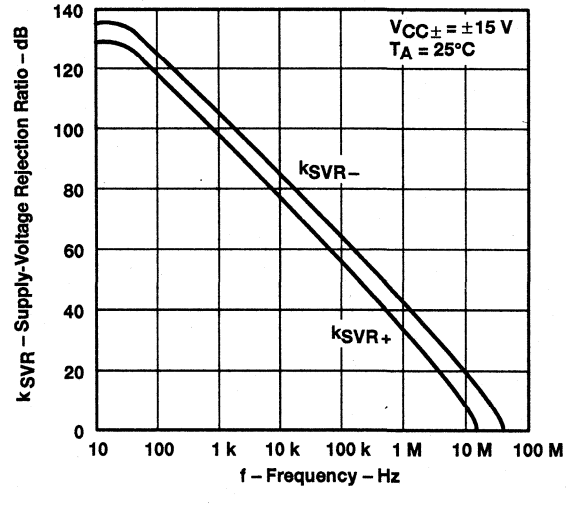

Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

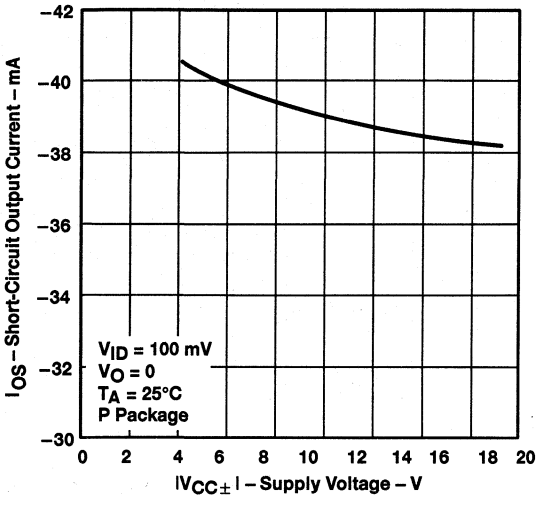

Figure 23

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

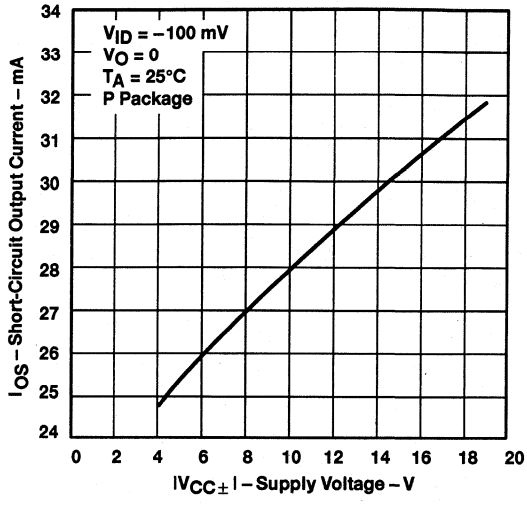

Figure 24

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

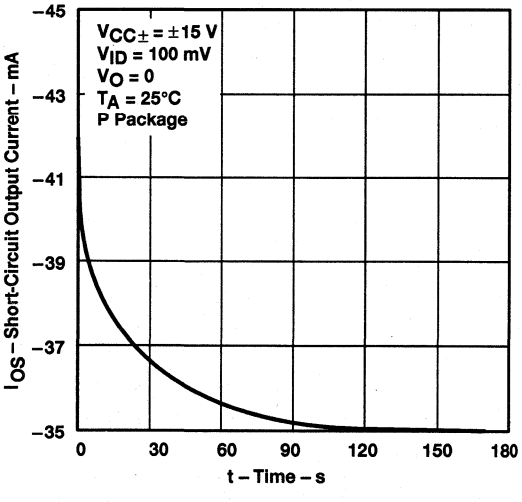

Figure 25

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

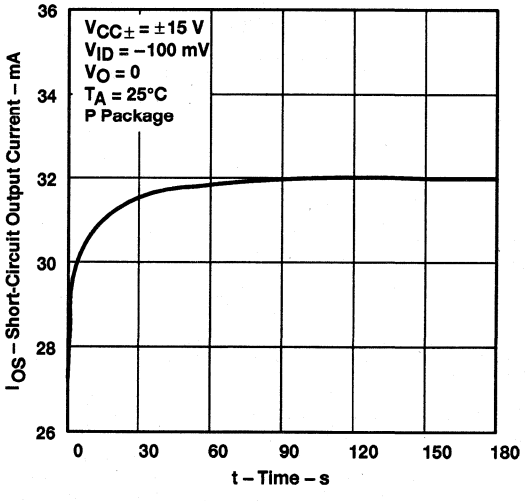

Figure 26

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

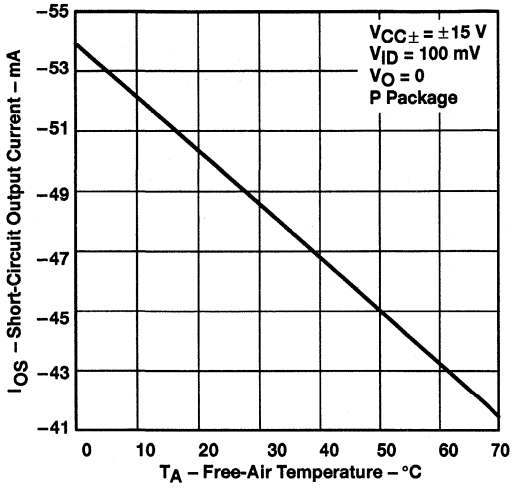

Figure 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

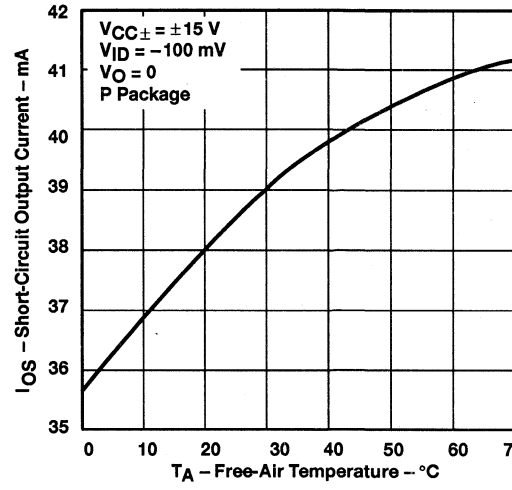

Figure 28

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

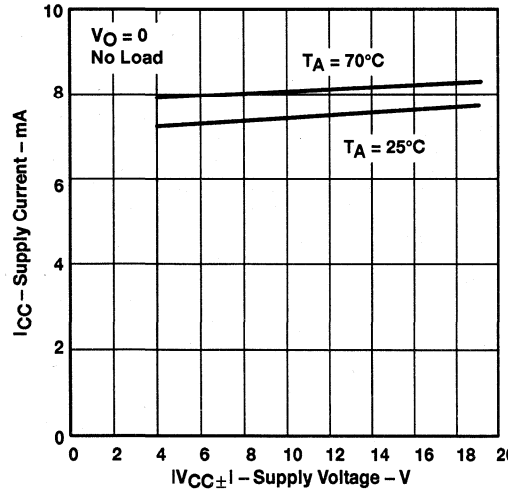

Figure 29

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

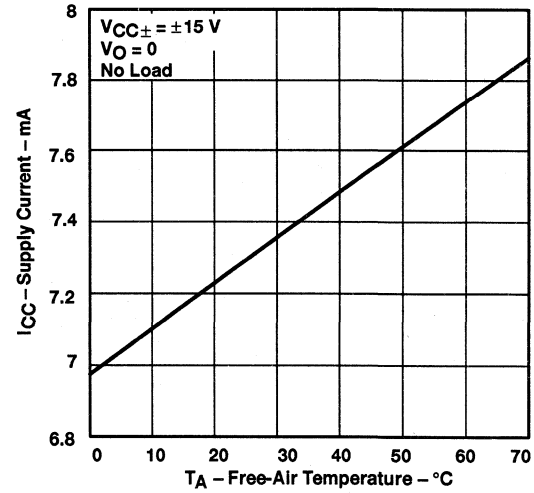

Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SMALL-SIGNAL
PULSE RESPONSE

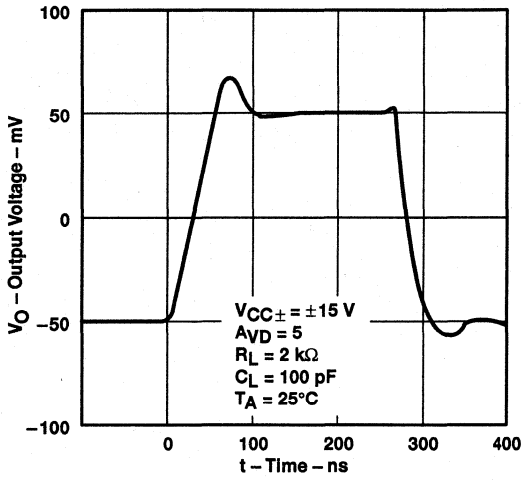

Figure 31

LARGE-SIGNAL
PULSE RESPONSE

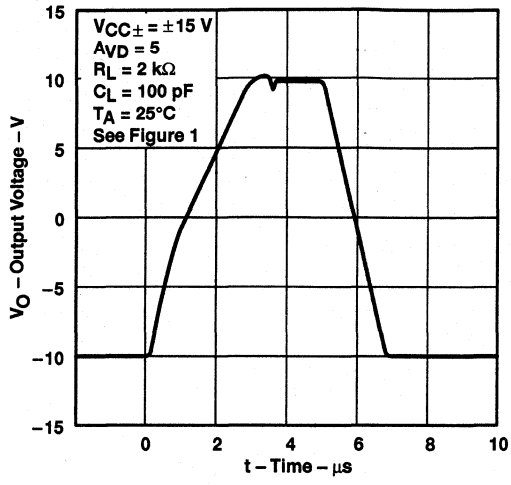

Figure 32

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

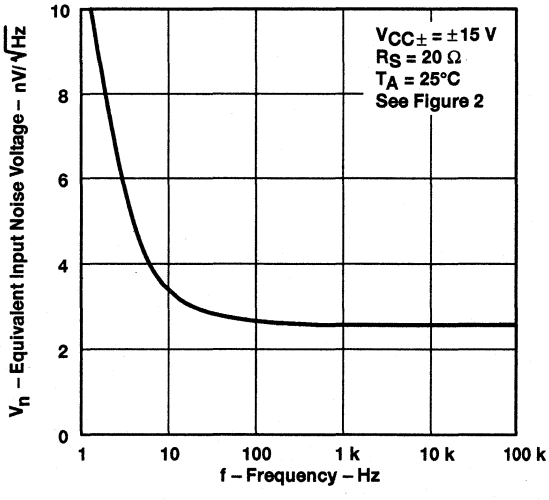

Figure 33

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-SECOND INTERVAL

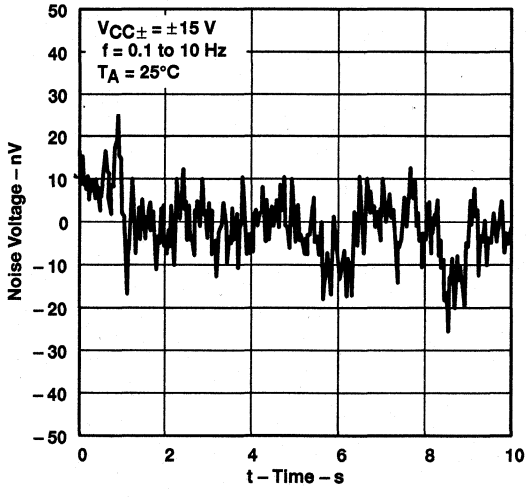

Figure 34

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

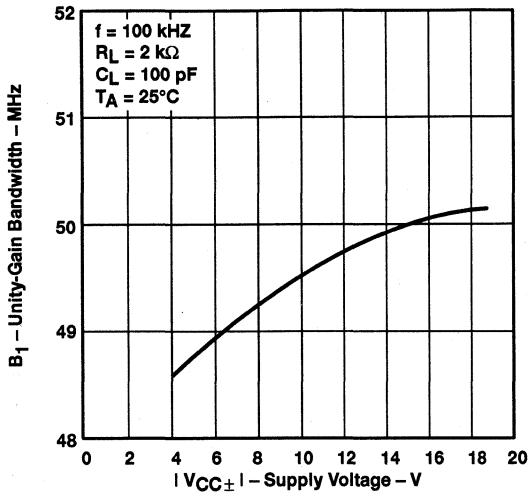

Figure 35

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

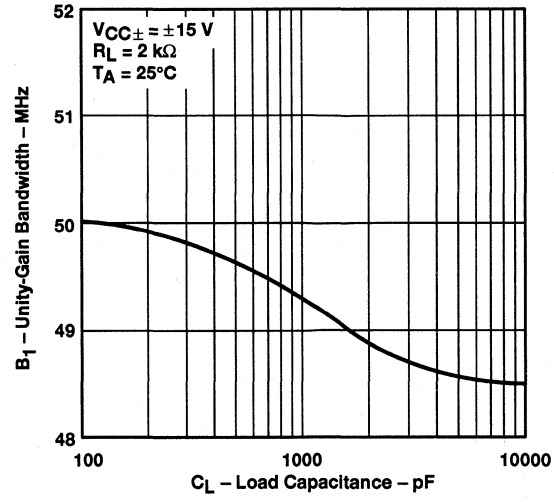

Figure 36

SLEW RATE vs FREE-AIR TEMPERATURE

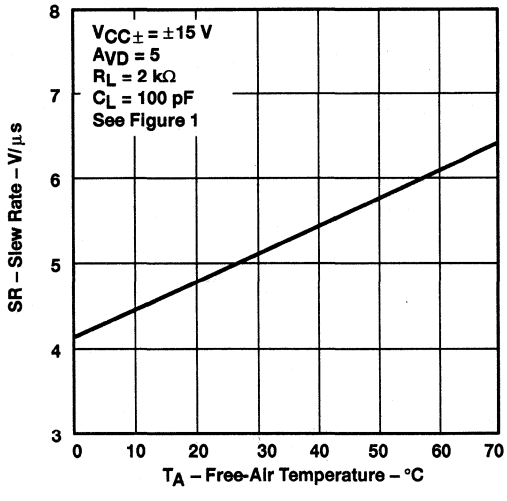

Figure 37

PHASE MARGIN vs SUPPLY VOLTAGE

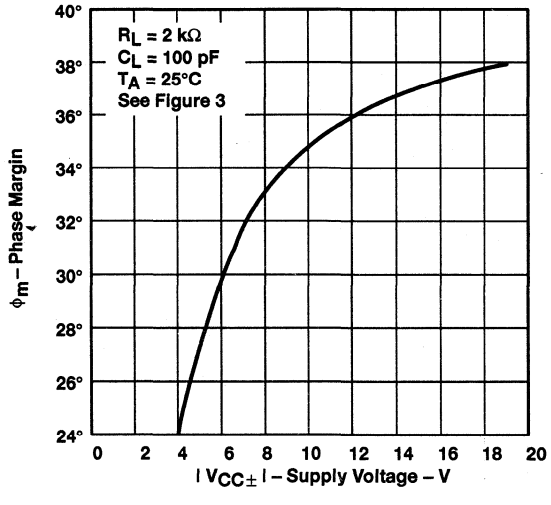

Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

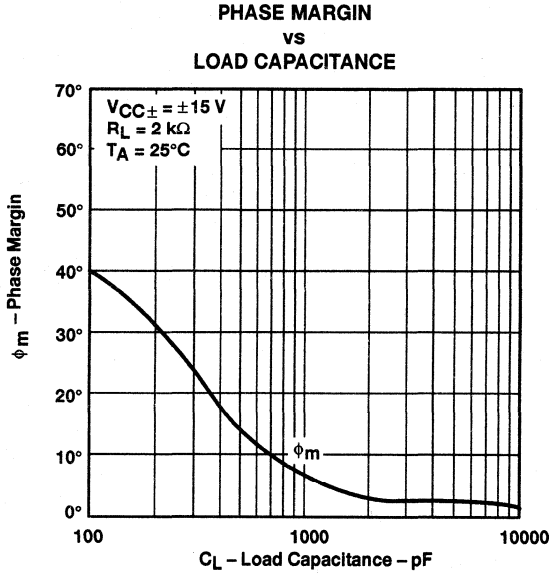

Figure 39

APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice™ Parts™* model generation software. The Boyle macromodel (see Note 6) and subcircuit in Figures 42 and 43 are generated using the TLE2227C typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain bandwidth
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)

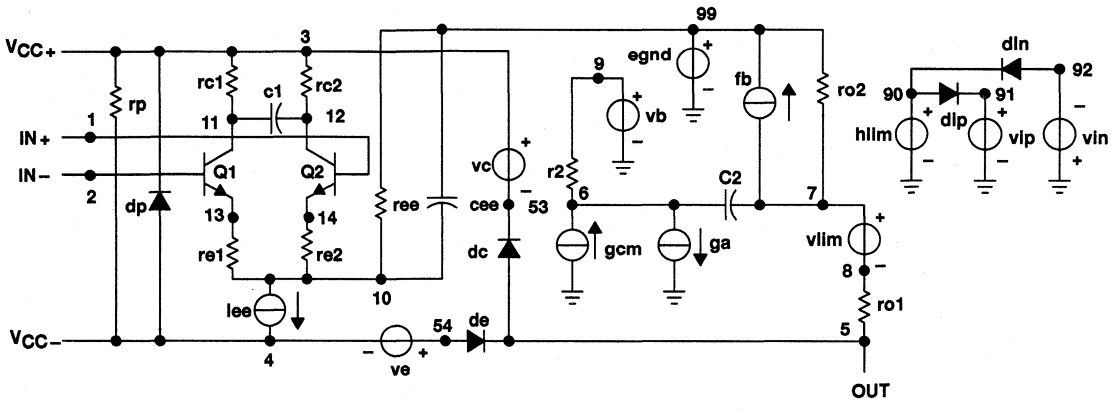


Figure 40. Boyle Macromodel

```
.subckt TLE2227  1   2   3   4   5
*
  c1     11    12  4.003E-12
  c2      6     7  20.00E-12
  dc      5    53  dx
  de     54     5  dx
  dlp    90    91  dx
  dln    92    90  dx
  dp      4     3  dx
  egnd   99     0  poly(2)   (3,0)  (4,0)  0   .5  .5
  fb      7    99  poly(5)   vb  vc  ve  vlp    vln     0   954.8E6   -1E9   1E9    1E9-1E9
  ga      6     0  11  12  2.062E-3
  gcm     0     6  10  99  531.3E-12
  iee    10     4  dc  56.01E-6
  hlim   90     0  vlim   1K
  q1     11     2  13  qx
  q2     12     1  14  qx
  r2      6     9  100.0E3
  rc1     3    11  530.5
  rc2     3    12  530.5
  re1    13    10  -393.2
  re2    14    10  -393.2
  ree    10    99  3.571E6
  ro1     8     5  25
  ro2     7    99  25
  rp      3     4  8.013E3
  vb      9     0  dc  0
  vc      3    53  dc  2.400
  ve     54     4  dc  2.100
  vlim    7     8  dc  0
  vlp    91     0  dc  40
  vln     0    92  dc  40
.model   dx D(Is=800.0E-18)
.model   qx NPN(Is=800.0E-18   Bf=7.000E3)
.ends
```

Figure 41. Macromodel Subcircuit

APPLICATION INFORMATION

voltage-follower

The TLE2237 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. A feedback resistor is recommended to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier's phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 42).

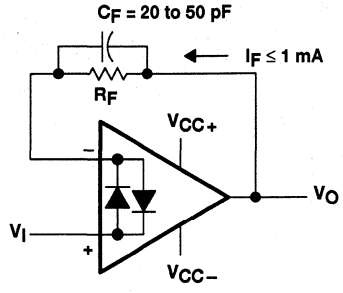
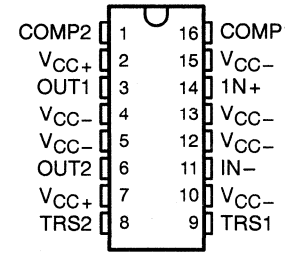


Figure 42. Voltage-Follower Circuit

- **High Output Drive Capability . . . 1 A Min**
- **3-State Outputs**
- **High Gain-Bandwidth Product 8 MHz Typ**
- **Low Total Harmonic Distortion <0.08% Typ**
- **High Slew Rate . . . 12 V/μs Typ**
- **Class AB Output Stage**
- **Thermal Shutdown**
- **Mains-Line Driver Circuit Application Included**

NE PACKAGE
(TOP VIEW)



Terminals 4, 5, 12 and 13 are connected to the lead frame.

description

The TLE2301 is a power operational amplifier that can deliver an output current of 1 A at high frequencies with very low total harmonic distortion. The device has an integral 3-state mode to drive the output stage into a high-impedance state and also to reduce the supply current to less than 3.5 mA.

The combination of high output current and 3-state outputs makes the TLE2301 ideal for implementing the signalling transformer driver in mains-based telemetering modems. This combination of features also makes the device well suited for other high-current applications (e.g., motor drivers and audio circuits).

Using the Texas Instruments established Excalibur process, the TLE2301 is able to achieve slew rates in excess of 12 V/μs and a gain-bandwidth product of 8 MHz. The TLE2301 uses a 16-pin NE power package to provide better power handling capabilities than standard dual-in-line packages.

The TLE2301 is characterized for operation over the industrial temperature range of –40°C to 85°C.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

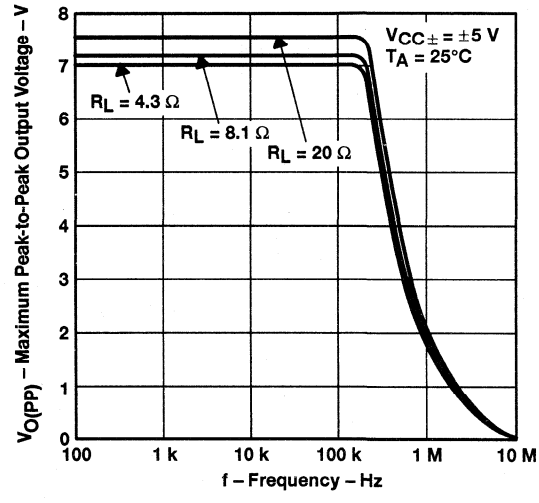
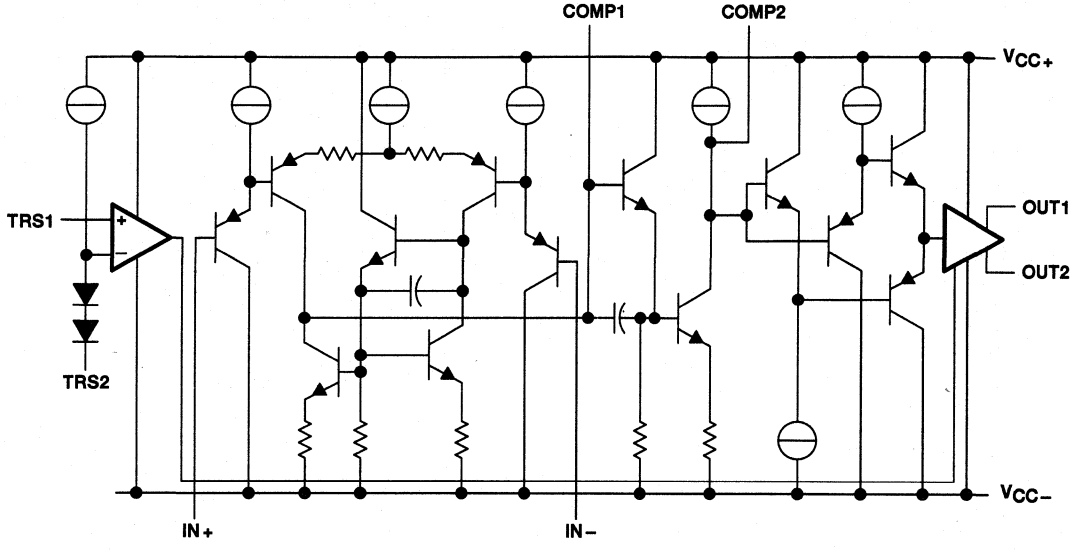


Figure 1

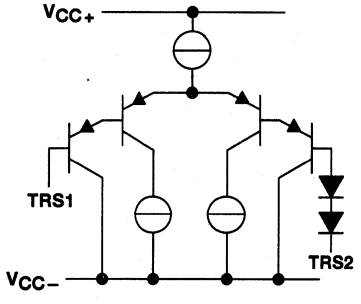
AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE
		THERMALLY-ENHANCED PLASTIC DIP (NE)
–40°C to 85°C	10 mV	TLE2301INE

equivalent schematic (entire device)



equivalent schematic (TRS1 and TRS2 inputs)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
COMP1 COMP2	16 1	COMP1 and COMP2 are compensation network terminals
IN+	14	Noninverting input
IN−	11	Inverting input
OUT1 OUT2	3 6	Two low-distortion class-AB output stages. Each is capable of sourcing more than 500 mA. OUT1 and OUT2 should be connected together for all applications.
TRS1 TRS2	9 8	TRS1 and TRS2 are 3-state input terminals. TRS2 should be connected to the ground of the circuit generating the 3-state command (normally μP ground). The TLE2301 is brought into 3-state mode by raising TRS1 2 V above TRS2. Placing the TLE2301 in a 3-state mode reduces the supply current to below 2.2 mA (typ). Normal operation resumes by bringing TRS1 to within 0.8 V of TRS2. The 3-state function can be disabled by connecting both TRS1 and TRS2 to V_{CC-}.
V_{CC-}	10, 15	High-impedance V_{CC-} input terminals. Although these do not carry any of the device's supply current, they increase the stability of the device and should be connected to the negative supply terminal (V_{CC-}).
V_{CC-}	4, 5, 12, 13	Negative supply terminals and substrate. As with all NE packages, the substrate is directly connected to the lead frame. The result is that the junction-to-ambient thermal impedance ($Z_{\theta JA}$) is greatly reduced by soldering the negative supply terminals to the copper area of the printed-circuit board (PCB).
V_{CC+}	2, 7	Positive supply terminals. Both terminals should be connected to the positive voltage supply.

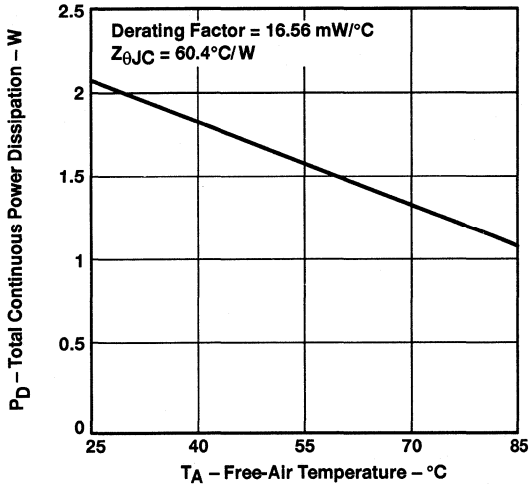
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Differential input voltage, V_{ID} (see Note 2)	±44 V
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 4 and 5)	2075 mW
Continuous total dissipation at 85°C case temperature (see Note 5)	4640 mW
Operating free-air temperature range, T_A	−40°C to 85°C
Operating case or virtual junction temperature range	−40°C to 150°C
Storage temperature range	−65°C to 150°C

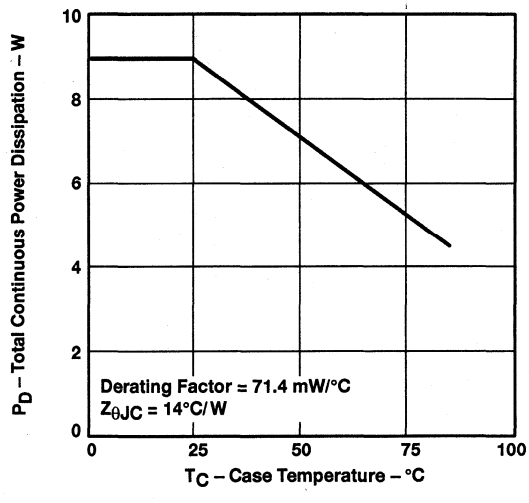
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The outputs when connected together may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 16.56 mW/°C.
5. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE



CASE TEMPERATURE DISSIPATION DERATING CURVE



recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±4.5	±20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	−4	1.6	V
	$V_{CC\pm}$ = ±15 V	−14	11.8	V
High-level 3-state enable voltage, V_{IH}		2		V
Low-level 3-state enable voltage, V_{IL}			0.8	V
Continuous output current			1	A
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V, C_C = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		0.4	7	mV
				Full range			10	
I_{IB}	Input bias current	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		283	450	nA
				Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		Full range	−4 to 1.6			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	3.3	3.5		V
				Full range	3.2			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	−3.2	−3.4		V
				Full range	−3.1			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2 V, R_L = 20 Ω	V_{IC} = 0,	25°C	65	87		dB
				Full range	60			
r_i	Differential input resistance			25°C		1		MΩ
r_o	Output resistance (see Note 7)	TRS1 = 0.8 V		25°C		1		Ω
		TRS1 = 2 V,	3-state mode			100		kΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	V_O = 0,	25°C	65	88		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4.5 V to ±20 V, V_{IC} = 0,	No load	25°C	70	100		dB
I_{IH}	Enable input current, high	V_I = 2 V,	3-state mode	25°C		0.01	0.5	μA
				Full range			0.5	
I_{IL}	Enable input current, low	V_I = 0.8 V		25°C		0.01	0.5	μA
				Full range			0.5	
I_{OS}	Short-circuit output current (see Note 8)	V_O = 0,	$t_p \le 50$ μs	25°C	1	1.8		A
I_{CC}	Supply current	V_O = 0,	No load	25°C		10	21	mA
				Full range			25	
		V_O = 0, 3-state mode	No load,	25°C		1.73	2.7	
				Full range			3.5	

† Full range is −40°C to 85°C.

NOTES: 6. OUT1 and OUT2 are connected together for all tests.
7. TRS1 voltage is measured with respect to TRS2 potential.
8. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately (t_p = pulse duration time).

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, C_C = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		0.3	10	mV
				Full range			15	
I_{IB}	Input bias current	V_O = 0, R_S = 50 Ω	V_{IC} = 0,	25°C		260	450	nA
				Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		Full range	−14 to 11.8			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	13	13.5		V
				Full range	13			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 20 Ω,	See Note 6	25°C	−12.6	−13		V
				Full range	−12.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±6 V, R_L = 20 Ω	V_{IC} = 0,	25°C	70	102		dB
				Full range	65			
r_i	Differential input resistance			25°C		1		MΩ
r_o	Output resistance (see Note 7)	TRS1 = 0.8 V		25°C		1		Ω
		TRS1 = 2 V,	3-state mode			100		kΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	V_O = 0,	25°C	70	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±4.5 V to ±20 V, V_{IC} = 0,	No load	25°C	70	100		dB
I_{IH}	Enable input current, high	V_I = 2 V,	3-state mode	25°C		0.01	0.5	μA
				Full range			0.5	
I_{IL}	Enable input current, low	V_I = 0.8 V		25°C		0.01	0.5	μA
				Full range			0.5	
I_{OS}	Short-circuit output current (see Note 8)	V_O = 0,	$t_p \leq 50$ μs	25°C	1	3		A
I_{CC}	Supply current	V_O = 0,	No load	25°C		11	25	mA
				Full range			30	
		V_O = 0, 3-state mode	No load,	25°C		2.2	3.5	
				Full range			5	

† Full range is −40°C to 85°C.

NOTES: 6. OUT1 and OUT2 are connected together for all tests.
7. TRS1 voltage is measured with respect to TRS2 potential.
8. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately (t_p = pulse duration time).

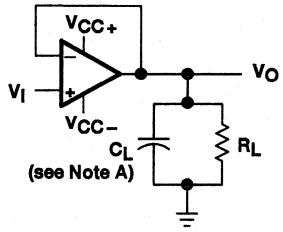
operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V, C_C = 15 pF, T_A = 25°C (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	V_O = ±1.5 V, R_L = 20 Ω, C_L = 100 pF	9	12		V/μs
t_s	Settling time (see Figure 1)	R_L = 20 Ω, C_L = 100 pF, 3-V step to 30 mV (1%)		0.7		μs
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 50 Ω, f = 1 kHz		44		nV/√Hz
THD	Total harmonic distortion	V_O = 1 V_{rms}, f = 50 kHz, R_L = 20 Ω, C_L = 100 pF		0.04%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		8		MHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		30°		

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, C_C = 15 pF, T_A = 25°C (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	V_O = ±10 V, R_L = 20 Ω, C_L = 100 pF	9	14		V/μs
t_s	Settling time (see Figure 1)	R_L = 20 Ω, C_L = 100 pF, 20-V step to 200 mV (1%)		1.8		μs
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 50 Ω, f = 1 kHz		44		nV/√Hz
THD	Total harmonic distortion	V_O = 2 V_{rms}, f = 50 kHz, R_L = 20 Ω, C_L = 100 pF		0.08%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		8		MHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 20 Ω, C_L = 100 pF		35°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes the fixture capacitance.

Figure 2. Slew-Rate Test Circuit

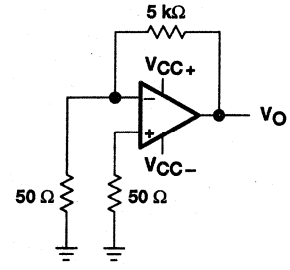
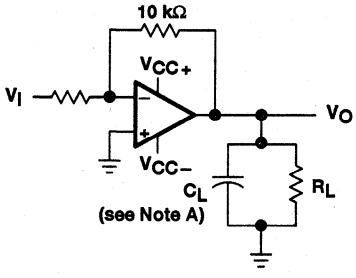


Figure 3. Noise-Voltage Test Circuit



NOTE A: C_L includes the fixture capacitance.

Figure 4. Gain-Bandwidth and Phase-Margin Test Circuit

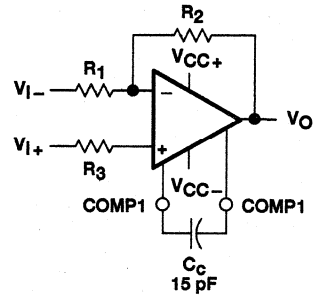


Figure 5. Compensation Configuration

typical values

Typical values presented in this data sheet represent the median (50% point) of the device parametric performance.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	6, 7
I_{IO}	Input offset current	vs Free-air temperature	6, 7
A_{VD}	Differential voltage amplification	vs Frequency	8
		vs Free-air temperature	9
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	10, 11
V_{OM}	Maximum peak output voltage	vs Output current	12, 13
		vs Supply voltage	14
$Z_{\theta JA}$	Transient junction-to-ambient thermal impedance	vs Time	15
I_{CC}	Supply current	vs Supply voltage	16
		vs Free-air temperature	17
	Pulse response	Small signal	18, 19
		Large signal	20, 21
z_o	Output impedance	vs Frequency	22, 23

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

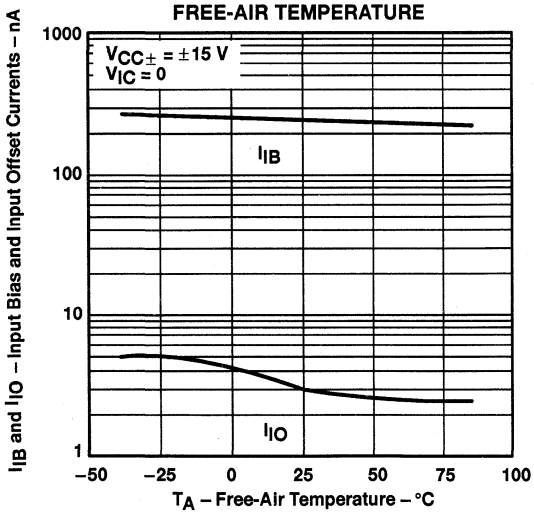


Figure 6

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

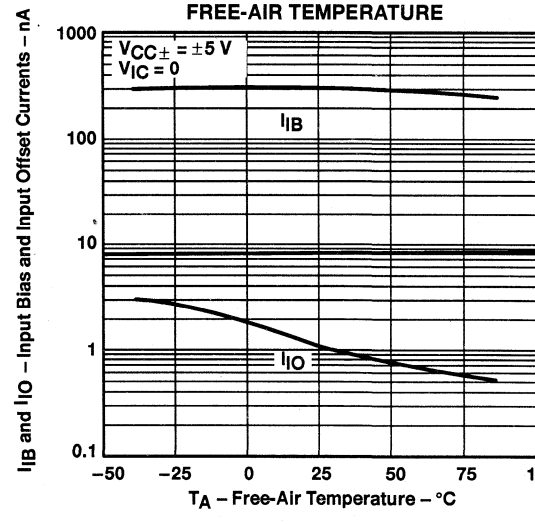


Figure 7

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

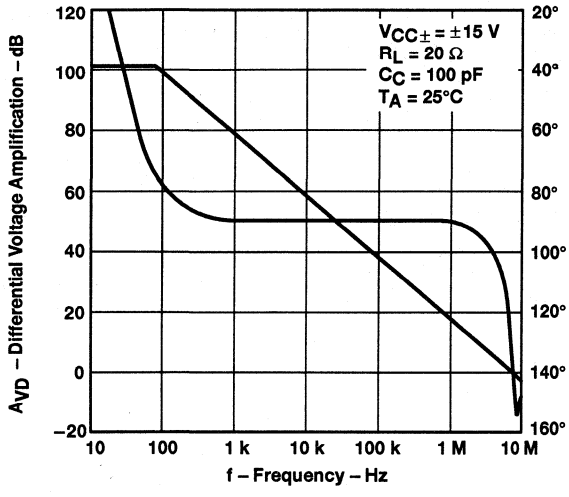


Figure 8

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

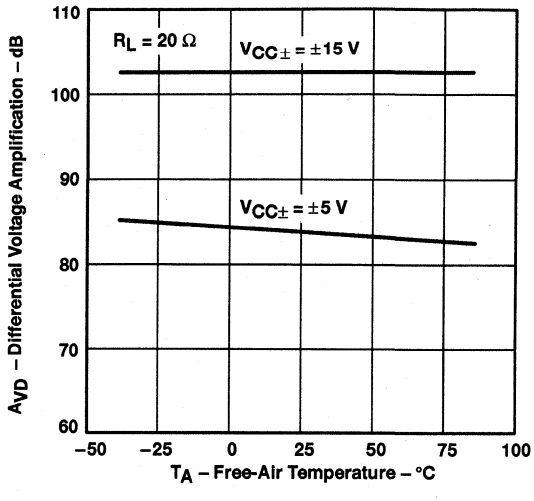


Figure 9

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

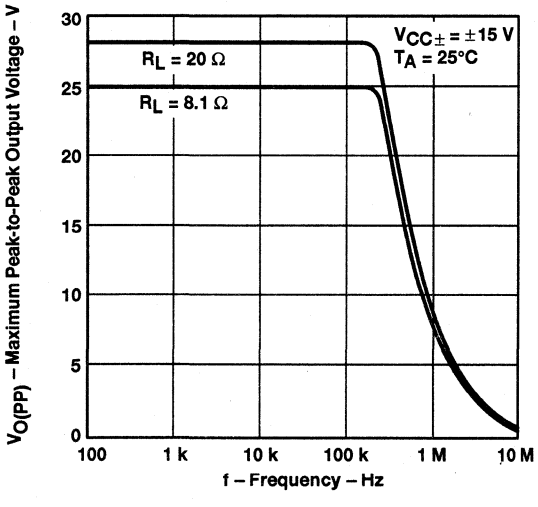


Figure 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

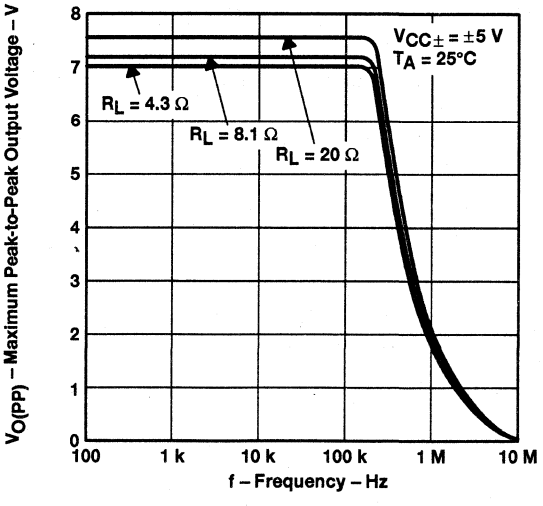


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

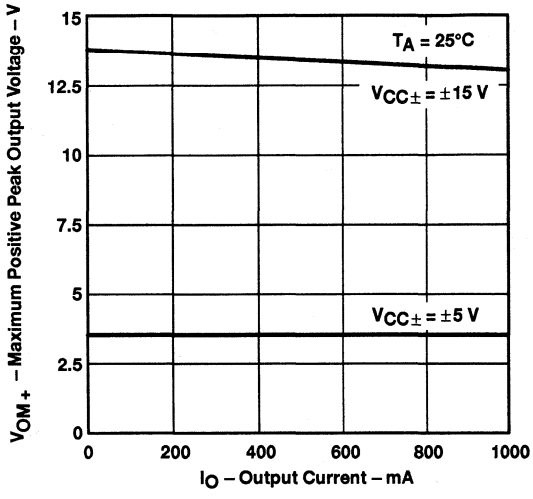


Figure 12

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

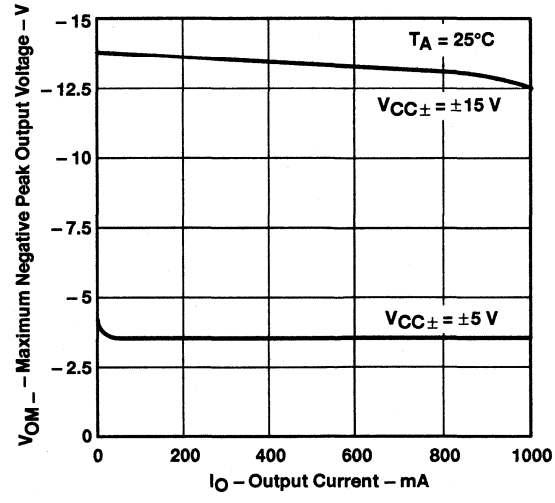


Figure 13

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

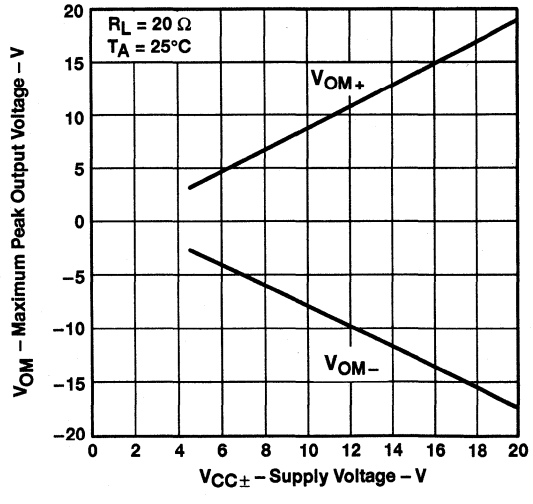


Figure 14

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE†
vs
ON TIME

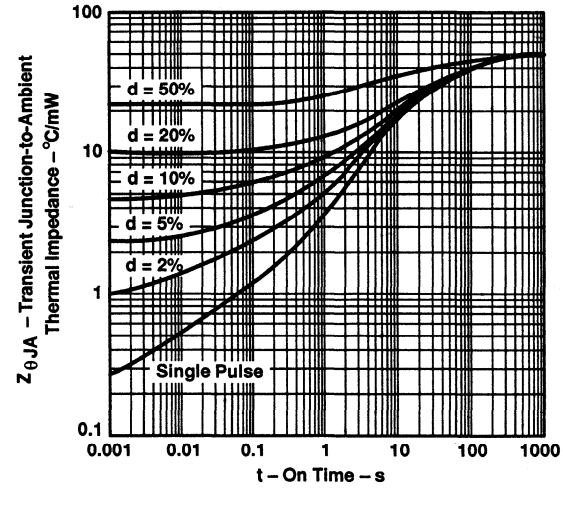


Figure 15

† d = duty cycle

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

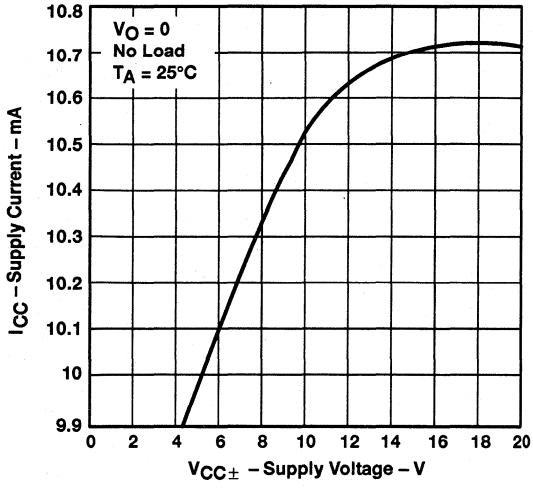


Figure 16

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

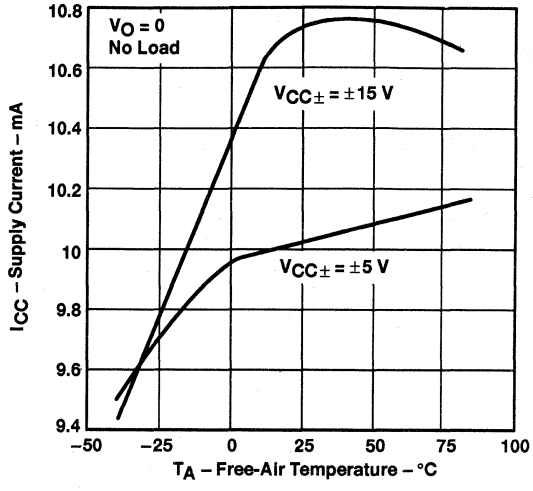


Figure 17

VOLTAGE FOLLOWER SMALL-SIGNAL PULSE RESPONSE

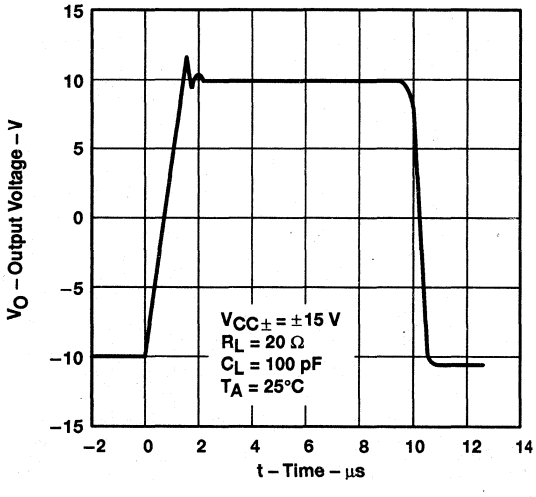


Figure 18

VOLTAGE FOLLOWER SMALL-SIGNAL PULSE RESPONSE

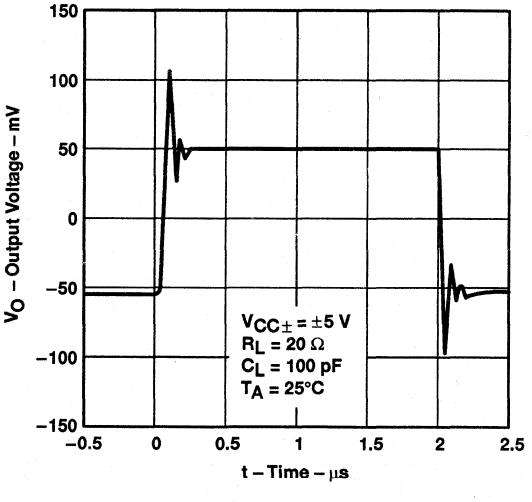


Figure 19

TYPICAL CHARACTERISTICS

VOLTAGE FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

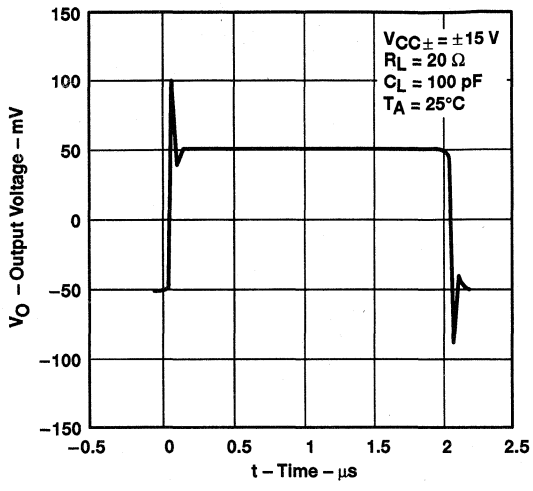


Figure 20

VOLTAGE FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

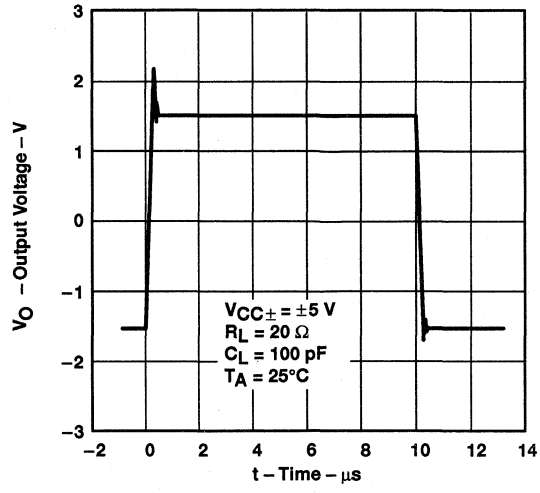


Figure 21

OUTPUT IMPEDANCE
vs
FREQUENCY

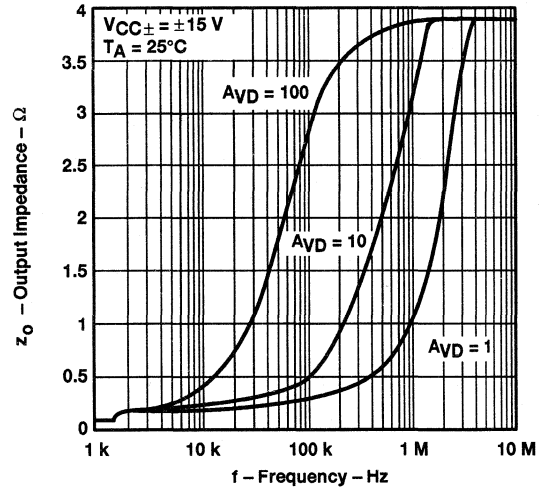


Figure 22

OUTPUT IMPEDANCE
vs
FREQUENCY

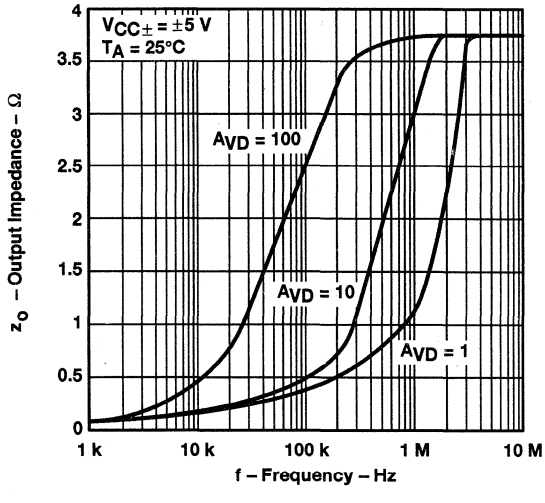


Figure 23

APPLICATION INFORMATION

circuit for mains-line driver over 40-kHz-to-90-kHz utility band

The following application is a circuit for *a mains-line driver over 40-kHz-to-90-kHz utility band* and is based around the European standard (EN56065–1) describing utility and consumer applications. This example shows a possible implementation for differential transmission on the mains line. This applications circuit is designed around the requirements of a domestic electricity meter operating over a utility band of 40 kHz to 90 kHz. A dual-rail power supply of ±5 V is used for this design example to limit device power dissipation. The same design principles, however, can be applied to other applications.

frequency band

The frequency band for utility applications extends over an enormous range from 3 kHz to 95 kHz. In order to have a coupling network that is economical and implemented with readily available components, this circuit is designed for a subband from 40 kHz to 90 kHz.

This subband is sufficiently wide to support multichannel operation; i.e., 10 channels of 5 kHz width or more if the channel widths are smaller. To avoid transmission spillover into the next band, a guard band of 5 kHz is allowed. The upper frequency of this circuit is set to 90 kHz, and the lower frequency is chosen for an economical coupling network and still has sufficient bandwidth to support multichannel operation.

output drive

The impedance of the mains network at these signalling frequencies is relatively low (<1 Ω to 30 Ω). This circuit has been designed to drive a 4-Ω mains line over the 40-kHz-to-90-kHz bandwidth.

The signalling impedance of the mains network fluctuates as different loads are switched on during the day or over a season, and it is influenced by many factors such as:

- Localized loading from appliances connected to the mains supply near to the connection of the communication equipment; e.g., heavy loads such as cookers and immersion heaters and reactive loads such as EMC filters and power factor correctors
- Distributed loading from consumers connected to the same mains cable, where their collective loading reduces the mains signalling impedance during times of peak electricity consumption; e.g., meal times
- Network parameters; e.g., transmission properties of cables and the impedance characteristics of distribution transformers and other system elements

With such a diversity of factors, the signalling environment fluctuates enormously, irregularly, and can differ greatly from one installation to another. The signalling system should be designed for reliable communications over a wide range of mains impedances and signalling conditions. Consequently, the transmitter must be able to drive sufficient signal into the mains network under these loading conditions.

The TLE2301 amplifier has 1-A output drive capability with short-circuit protection; hence, it adequately copes with the high current demands required for implementing mains signalling systems.

3-state facility

When transmitting, the transmitter appears as a low-impedance signal source on the mains network. If transmitters are left in the active mode whether transmitting or not and a large number of transmitters are installed in close proximity, their combined loading would reduce the mains impedance to unacceptable levels. Not only would each transmitter need to drive into an extremely low mains impedance, but signals arriving from distant transmitters would be severely attenuated.

To overcome this problem, the transmitters need to present a high impedance to the mains network when they are not transmitting. The mains network is then only loaded by a few transmitters at any one time, and the mains signalling impedance is not adversely affected.

APPLICATION INFORMATION

3-state facility (continued)

The TLE2301 incorporates an output 3-state facility, removing the need for additional circuitry to achieve this function. In addition, the TLE2301 has a low standby current in the 3-state mode, making it ideal for applications where low power consumption is also essential.

circuit configuration

The design methodology is to minimize power dissipation in the TLE2301 by maximizing the use of the available output voltage swing of the amplifier. The amplifier's output can swing to within 2 V of the supply rail before saturation begins. With a chosen supply of ± 5 V, the maximum peak-to-peak voltage swing is 6 V. To ensure that the amplifier's output is not likely to clip under heavy loads, the maximum output voltage swing has been reduced by 0.5 V, giving a usable peak-to-peak output voltage swing of 5.5 V.

It is assumed that the input signal to the transmitter stage has a peak-to-peak amplitude of 2.8 V (1 Vrms) as might be expected if the transmission signal is digitally synthesized by circuitry operating solely from the 5-V supply. The gain of the amplifier stage is appropriately set to:

$$\text{Gain} = \frac{\text{peak-to-peak output voltage swing}}{\text{peak-to-peak input voltage}}$$

$$= \frac{5.5\ \text{V}}{2.8\ \text{V}}$$

$$= 1.96$$

An inverting amplifier configuration is chosen for this example, as the input signal source is assumed to have a relatively low impedance in relation to the gain-setting resistors.

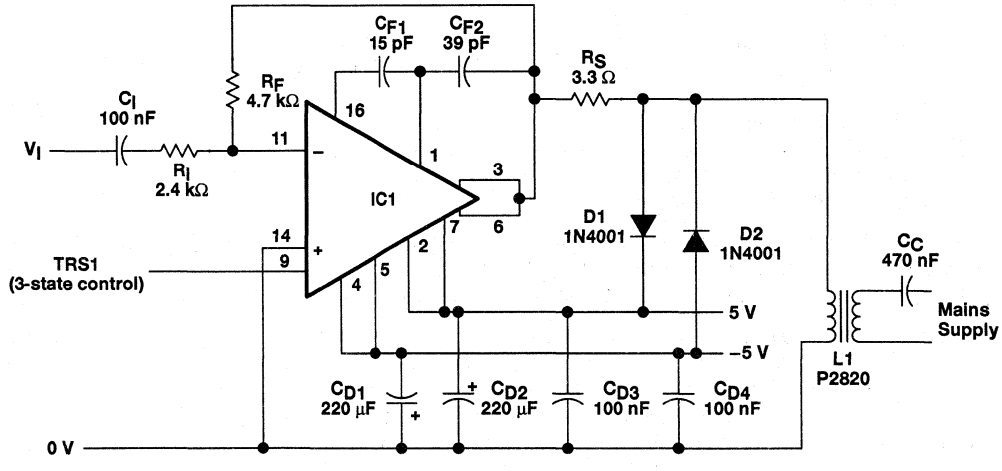


Figure 24. Full-Circuit Diagram for Utility Band

A noninverting amplifier configuration could be used when the input signal needs to be terminated with high impedance, but the user should take care that the amplitude of the input signal does not exceed the common-mode input range ($-4\ \text{V} < V_{ICM} < 1.8\ \text{V}$ at $V_{CC} = \pm 5\ \text{V}$) for low-gain implementations.

APPLICATION INFORMATION

component calculations

The following sections contain the calculations for input capacitors, gain resistors, coupling network, coupling capacitors, transformer-leakage inductance, series resistors, decoupling, and frequency compensation.

input capacitor

The incoming signal is ac coupled to remove any incoming dc offset and to provide only unity gain for the amplifier's input offset voltage. The value of 100 nF is chosen for this input capacitor as it has very little influence on the amplifier's signal gain over the frequency band.

gain resistors

The gain-setting resistors are chosen for a gain of 1.96; i.e., choosing:

$$\text{Gain} = \frac{R_F}{R_I}$$

$$R_F = 4.7\ \text{k}\Omega \text{ and } R_I = 2.4\ \text{k}\Omega$$

$$= \frac{4.7\ \text{k}\Omega}{2.4\ \text{k}\Omega}$$

$$= 1.96$$

The resistor values are low enough to ensure that the circuit does not suffer from stray capacitance and signal pick-up problems but not too low as to significantly load the mains impedance when the amplifier is in its high-impedance state.

coupling network

The function of the line interface is to provide isolation from the mains supply while coupling the communication signals onto the mains network. As the mains voltage is large in comparison with the communication signals, the mains voltage needs to be isolated from the electronic circuitry. The simple coupling network limits the current flowing from the mains supply as well as providing a convenient point at which to implement the safety isolation barrier between the mains supply and the communications circuitry. The transformer can easily achieve an isolation of 4 kV between primary and secondary windings, and the capacitor provides the low frequency roll-off to impede the mains voltage.

The transformer has two other useful properties. First, the turns ratio can be selected to provide efficient power transfer between the TLE2301 amplifier and the mains network. Second, the transformer possesses leakage inductance that can be tuned with the coupling capacitor to form a band-pass filter.

By altering the turns ratio, the power dissipated in the TLE2301 can be reduced while maintaining the required voltage levels on the mains line. A turns ratio of 1.67:1 was selected in this design to apply a 120-μdBV signal onto the mains line. The calculation for the turns ratio is not straightforward due to the presence of numerous complex impedances. The simplest method for deriving the turns ratio is to model the circuit with an analog simulation program such as PSpice™. It is from these simulations that the 1.67:1 turns ratio has been selected.

PSpice is a registered trademark of MicroSim Corporation.

APPLICATION INFORMATION

coupling capacitor

With such a wide frequency band, the quality factor of the coupling filter needs to be low in order to avoid unacceptably large attenuation at the band edges and to achieve a good coupling performance that is insensitive to a wide range of loads. For a band-pass filter of this configuration, the quality factor is proportional to the reciprocal of the coupling capacitance. For low Q, the value of C_C needs to be large.

Q = quality factor and C_C = coupling capacitor

$$Q \propto \frac{1}{C_C}$$

Counterbalancing this need for a large value of C_C creates two more considerations. First, the capacitance should not be so large as to allow significant 50-Hz mains current through the transformer ($I = 2 \times \pi \times f \times C_C \times V$). Second, the coupling capacitor is required to meet certain safety standards. The coupling capacitor is actually an RFI-suppression capacitor that has been designed by the manufacturers to provide an adequate level of protection when connected across the various conductors of the mains supply (consult the UL1283 or UL1414 standards for RFI capacitors). These types of capacitors can be expensive, physically large, restricted in capacitance value, and limited in the number of manufacturers.

As a reasonable compromise between all these factors, a coupling capacitor of 470 nF is chosen. This value is multisourced, moderately priced, limits the mains current through the transformer to less than 36 mA rms, and has sufficient capacitance to form the desired low-Q filter.

transformer leakage inductance

The transformer leakage inductance, inherent to the transformer, can be used to form an LC band-pass filter. If the capacitor alone is used to couple onto the mains network, its capacitance value needs to be quite large for it to have a reasonably low reactance at the signalling frequencies. Forming an LC filter greatly reduces the value of capacitor required. The center frequency of the filter is not the same as the midband frequency of 65 kHz. Band-pass filters show a symmetrical shape only when plotted against the logarithm of frequency, so the center frequency (f_o) is given by the following formula:

$$f_o = \sqrt{f_{lower} \times f_{upper}}$$

$$= \sqrt{(40 \times 90)}\ \text{kHz}$$

$$= 60\ \text{kHz}$$

The leakage inductance of the transformer, as viewed from the winding connected to the coupling capacitor, is derived from $2\pi f_O = 1/\sqrt{LC}$. The required leakage inductance of the transformer is:

$$L = \frac{1}{(2\pi f_o)^2 \times C_C}$$

$$= \frac{1}{(2\pi \times 60\ \text{kHz})^2 \times 470\ \text{nF}}$$

$$= 15\ \mu\text{H}$$

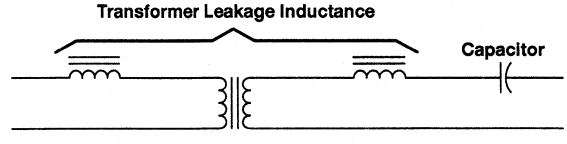


Figure 25. Band-Pass Coupling Filter

APPLICATION INFORMATION

series resistor

The series resistor, R_S, is included to limit the turn-on current, the amplifier's offset current, and the signalling current through the filter. With dual supply rails, there is always a potential problem of large turn-on currents as the amplifier powers up. If one supply rail turns on before the other, the output of the TLE2301 amplifier could saturate near to the applied supply rail, causing a large current to flow through the transformer winding ($R_{winding}$ = 0.1 Ω for the P2820 transformer). The power supply needs to be of sufficient rating to ensure that its rails could rise to the minimum operating voltage of the amplifier, at which point the amplifier is ensured to have returned to stable operation.

With a series resistor of 3.3 Ω and assuming the output saturates at the maximum peak-to-peak voltage excursion of 3 V, this turn-on current is limited to less than the device's 1-A rating ($I_{transient}$ = 3 V/3.3 Ω = 0.91 A). Further reduction of this turn-on current by raising the value of the series resistor deteriorates the filter's performance into low signalling impedances on the mains network.

Alternatively, this turn-on current could be blocked by means of a series capacitor, but for this frequency band the capacitor has to be large in value (≥3.3 μF) so as not to adversely affect the filter. A nonpolarized capacitor of this value is relatively expensive, and the resistor is still required to fulfill other functions.

Another way of preventing overcurrent at power up is to use the TLE2301 3-state mode. As the TRS2 control line is intended to be tied to the microprocessor's 0-V rail, the TRS1 control line must be taken high to activate the 3-state mode, which implies that the positive rail is required to turn on first. Other schemes could be devised to take TRS2 below the 0-V rail until the power supply has stabilized if the negative rail turns on first. Instead of relying on a definite power-supply sequence or elaborate control circuitry, it is simpler to limit the current either with a series resistor or capacitor.

The second function of the series resistor is to limit the dc current flow through the transformer winding due to the dc offset at the amplifier's output, which is caused by its input offset voltage. For a worst case input offset of 20 mV, the output offset is also 20 mV as the dc gain of the circuit is unity. Offsets due to input bias currents are negligible since the values of the gain-setting resistors are low. The dc current through the transformer is therefore less than 7 mA (20 mV/3.3 Ω). This low level of dc current does not appreciatively increase the power dissipation of the amplifier or noticeably diminish the harmonic performance of the transformer.

The final function of the series resistor is to limit the signalling current in the event that the mains impedance might appear as solely reactive; i.e., without a resistive component. As a rough estimate, the peak signal current from the amplifier is:

$$I_{OM} = \frac{V_{O(PP)}}{R_S} = \frac{\left(\frac{5.5\ V}{2}\right)}{3.3\ \Omega} = 833\ mA$$

where:

$V_{O(PP)}$ = Peak-to-peak output voltage swing

I_{OM} = Peak-output-signalling current from amplifier

APPLICATION INFORMATION

series resistor (continued)

Again, the value of the series resistor is sufficient to limit the peak-signal current below the device's maximum rating. This calculation does not take into account other resistive impedances in the signal path, which would further reduce the peak signal current from the amplifier.

decoupling

Power-supply decoupling for the amplifier is provided by a 220-µF electrolytic capacitor and a 100-nF ceramic capacitor per supply rail located close to the supply terminals of the TLE2301 device.

The decoupling capacitors for the negative supply should be connected to a pair of V_{CC-} terminals (4 and 5 or 12 and 13), whichever pair is most convenient from a printed-circuit-board (PCB) layout point of view. In order to minimize parasitic lead inductances, these capacitors should be located as close as possible to the device terminals to which they are connected. As the V_{CC+} terminals are not adjacent on the package, the decoupling capacitors should be connected to one terminal with a thick PCB track going to the other terminal.

The 220-µF electrolytic capacitor is chosen to provide good decoupling performance (less than 25-mV ripple under the worst-case loading for the utility circuit). This value could be reduced to 100 µF for higher-frequency consumer bands. The level of ripple depends on the source impedance of the power supply and the equivalent series resistance of the chosen decoupling capacitors. The 100-nF ceramic capacitor provides high-frequency decoupling for the amplifier.

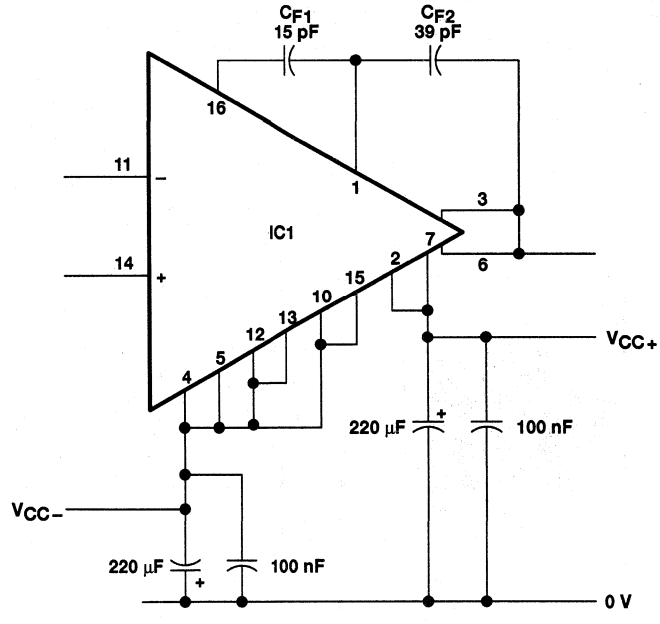


Figure 26. Amplifier Decoupling and Compensation

APPLICATION INFORMATION

frequency compensation

The TLE2301 amplifier requires one compensation capacitor. However, when driving heavy loads, stability can be increased by connecting V_{CC-} terminals 10 and 15 to V_{CC-} terminals 12 and 13 and using another capacitor between COMP2 and the outputs. The circuit included in this application has been designed with two compensation capacitors. The component values chosen are:

C_{F1} = 15 pF
C_{F2} = 33 pF

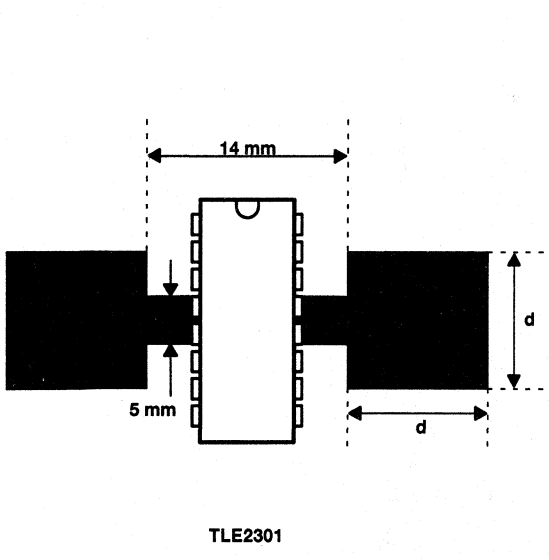
These component values could be adjusted if the amplifier is used for higher-frequency applications.

power dissipation

The impedance of the mains network fluctuates greatly for many reasons, but its impedance at the supply-distribution transformer is typically very low, less than 1 Ω, whereas the mains impedance in a house commonly has a higher value, from 4 Ω to 40 Ω. For utility-metering applications, a master transmitter may be sited at the supply-distribution transformer and would need to deliver more power into the mains network than the household transmitter when generating comparable signal amplitudes.

NE thermally-enhanced dual in-line package

The TLE2301 utilizes the four center terminals of the dual-in-line package (NE) to transfer heat to a copper area on the PCB. A copper area of 1290 mm^2 provides a junction-to-ambient thermal impedance, $Z_{\theta JA}$, of 34°C/W, allowing the device to dissipate up to 1.9 W at 85°C for a junction temperature of 150°C or up to 1.5 W at 85°C for a junction temperature of 135°C.



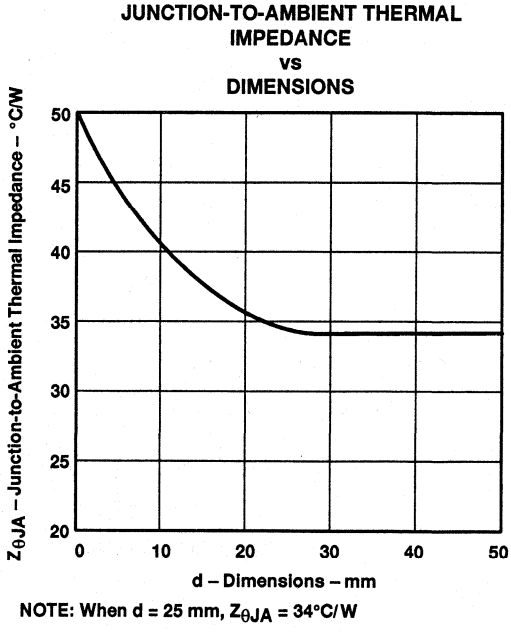


Figure 27. PCB Heatsink

APPLICATION INFORMATION

power dissipation in amplifier

For sinusoidal waveforms, the dissipation in the amplifier, P_{AMP}, is:

$$P_{AMP} = \left(2 \times V_{CC} \times I_{CC}\right) + \frac{\left(2 \times V_{CC} \times I_{OM}\right)}{\pi} - P_O$$

where:

I_{CC} = Amplifier's quiescent current
I_{OM} = Peak-output-signalling current from amplifier
P_O = Output power consumed by coupling network and load

The power dissipated in the amplifier is minimized if the amplifier's peak output current, I_{OM}, is minimized. Since the output power consumed by the coupling and load is a function of current and voltage ($P_O \approx I_O \times V_O$), the amplifier's peak output current can be minimized by maximizing the amplifier's output voltage swing.

circuit parts list

The associated parts list is:

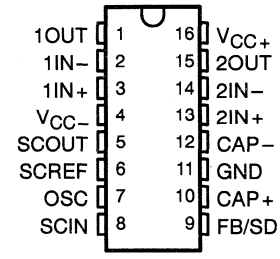
REFERENCE	FIGURE	COMPONENT	DESCRIPTION
IC1	Figure 24, Figure 26	TLE2301 operational amplifier	Texas Instruments TLE230INE
L1	Figure 24	1.67:1, 15-µH leakage transformer	Electronics Techniques P2820 (European manufacturer)
C_C	Figure 24	470-nF capacitor	Metalized paper, safety standards UL1414
C_I	Figure 24	100-nF capacitor	Ceramic, general purpose
C_{F1}	Figure 24, Figure 26	15-pF capacitor	Ceramic, general purpose
C_{F2}	Figure 24, Figure 26	39-pF capacitor	Ceramic, general purpose
C_{D1}, C_{D2}	Figure 24	220-µF, 10-V min capacitors	Aluminum electrolytic, general purpose
C_{D3}, C_{D4}	Figure 24	100-nF capacitors	Ceramic, general purpose
R_F	Figure 24	4.7-kΩ, 0.125-W min resistor	Metal film, general purpose
R_I	Figure 24	2.4-kΩ, 0.125-W min resistor	Metal film, general purpose
R_S	Figure 24	3.3-kΩ, 1-W min, resistor	
D1, D2	Figure 24	1N4001 series, 1-A min diodes	General purpose

DUAL μPOWER JFET-INPUT OPERATIONAL AMPLIFIER WITH SWITCHED-CAPACITOR VOLTAGE CONVERTER

SLOS118B – DECEMBER 1992 – REVISED AUGUST 1994

- **Single-Supply Operation With Rail-to-Rail Inputs**
- **V_{OL} = 0.000 V While Sinking 25 mA**
- **Wide V_{CC} Range . . . 3.5 V to 15 V**
- **SCOUT Supplies up to 100 mA for External Loads**
- **Shutdown Mode**
- **External 2.5-V Voltage Reference Available**

DW PACKAGE
(TOP VIEW)



description

The TLE2662 offers the advantages of JFET-input operational amplifiers and rail-to-rail common-mode input voltage range with the convenience of single-supply operation. By combining a switched-capacitor voltage converter with a dual operational amplifier in a single package, Texas Instruments now gives circuit designers new options for conditioning low-level signals in single-supply systems.

The TLE2662 features two low power, high-output drive JFET-input operational amplifiers with a switched-capacitor building block. Using two external capacitors, the switched-capacitor network can be configured as a voltage inverter, generating a negative supply voltage capable of sourcing up to 100 mA. This supply functions not only as the amplifier negative rail but is also available to drive external circuitry. In this configuration, the amplifier common-mode input voltage range extends from the positive rail to below ground, providing true rail-to-rail inputs from a single supply. Furthermore, the outputs can swing to and below ground while sinking over 25 mA. This feature was previously unavailable in operational amplifier circuits. The TLE2662 operational amplifier section has output stages that can drive 100-Ω loads to 2.5 V from a 5-V rail. With a 10-kΩ load, the output swing extends to 3.5 V and can include the positive rail with a pullup resistor.

This operational amplifier offers the high slew rate, wide bandwidth, and high input impedance commonly associated with JFET-input amplifiers, making the TLE2662 operational amplifier section suited for amplifying fast signals without loading the signal source. When not sourcing or sinking current into a load, the amplifier consumes only microamperes of supply current, thereby reducing the drain on and extending the life of the power supply.

The TLE2662 features a shutdown pin (FB/SD), which can be used to disable the switched capacitor section. When disabled, the voltage converter block draws less than 150 μA from the power supply. This feature, combined with the operational amplifier's low quiescent current, makes the TLE2662 a real power saver in the standby mode.

The switched-capacitor building block also provides an on-board regulator; with the addition of an external divider, a well-regulated output voltage is easily obtained. Additional filtering can be added to minimize switching noise. The internal oscillator runs at a nominal frequency of 25 kHz. This can be synchronized to an external clock signal or can be varied using an external capacitor. A 2.5-V reference is brought out to SCREF for use with the on-board regulator or external circuitry.

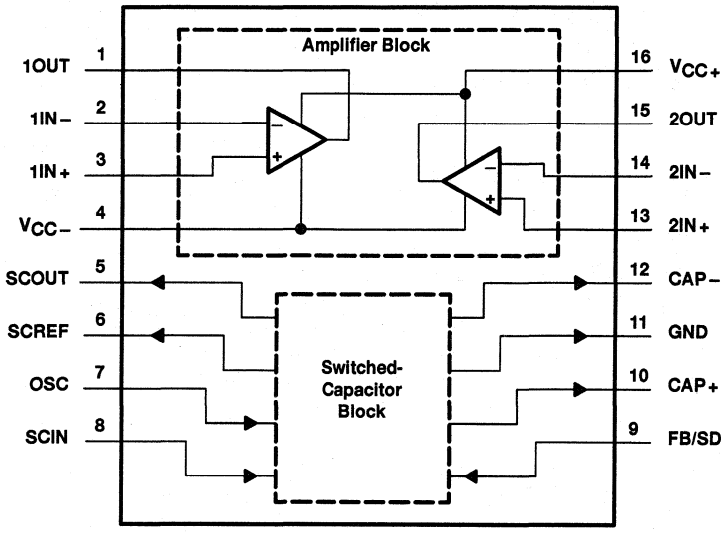
The TLE2662 is characterized for operation over the industrial temperature range of −40°C to 85°C. This device is available in a 16-pin wide-body surface-mount package.

AVAILABLE OPTION

T_A	PACKAGE
	SMALL OUTLINE (DW)
−40°C to 85°C	TLE2662IDW

The DW package is available taped and reeled. Add the suffix R to the device type (i.e., TLE2662IDWR).

functional block diagram



ACTUAL DEVICE COMPONENT COUNT

AMPLIFIER BLOCK		SWITCHED-CAPACITOR BLOCK	
Transistors	42	Transistors	71
Resistors	9	Resistors	44
Diodes	3	Diodes	2
Capacitors	2	Capacitors	5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, SCIN (see Note 1) ..... 16 V
Supply voltage, V_{CC+} (see Note 2) ..... 16 V
Supply voltage, V_{CC-} (see Note 2) ..... −16 V
Differential input voltage, V_{ID} (see Note 3) ..... 32 V
Input voltage, V_I (any input of amplifier) (see Note 2) ..... $V_{CC\pm}$
FB/SD (see Note 1) ..... 0 V to SCIN
OSC (see Note 1) ..... 0 V to SCREF
Input current, I_I (each input of amplifier) ..... ±1 mA
Output current, I_O (each output of amplifier) ..... ±80 mA
Total current into V_{CC+} ..... 80 mA
Total current out of V_{CC-} ..... 80 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 4) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Junction temperature (see Note 5) ..... 150°C
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the switched-capacitor block GND.
2. Voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at IN+ with respect to IN−.
4. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
5. The devices are functional up to the absolute maximum junction temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC+}/SCIN		3.5	15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	−1.6	4	V
	$V_{CC\pm}$ = ±15 V	−11	13	
Operating free-air temperature, T_A		−40	85	°C
Output current at SCOUT, I_O		0	100	mA

OPERATIONAL AMPLIFIER SECTION

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		1	5	mV
				Full range			6.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 6)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing	I_L = 2 mA		25°C	3.4	3.7		V
				Full range	3			
		I_L = 20 mA		25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing	I_L = 2 mA		25°C	−3.4	−3.9		V
				Full range	−3			
		I_L = 20 mA		25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.8 V,	R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		V_O = 0 to 2 V,	R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
		V_O = 0 to −2 V,	R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
C_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance	I_O = 0		25°C		560		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, V_{IC} = V_{ICR}min		25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current	I_L = 0		25°C		560	620	μA
				Full range			640	

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.
‡ Full range is −40°C to 85°C.
NOTE 6: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF	25°C		1.3		
t_s	Settling time	To 0.1%		25°C		5		μs
		To 0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF	25°C		75°		

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.
‡ Full range is −40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		0.9	4	mV
				Full range			5.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 6)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing	I_L = 2 mA		25°C	13.2	13.7		V
				Full range	13			
		I_L = 20 mA		25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing	I_L = 2 mA		25°C	−13.2	−13.7		V
				Full range	−13			
		I_L = 20 mA		25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V,	R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
		V_O = 0 to 8 V,	R_L = 600 Ω	25°C	25	100		
				Full range	10			
		V_O = 0 to −8 V,	R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
C_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance	I_O = 0		25°C		560		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, V_{IC} = V_{ICR}min		25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω		25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current	I_L = 0		25°C		625	690	μA
				Full range			720	

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.
‡ Full range is −40°C to 85°C.
NOTE 6: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
t_s	Settling time	To 0.1%		25°C		5		μs
		To 0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.
‡ Full range is −40°C to 85°C.

SWITCHED-CAPACITOR SECTION

electrical characteristics over recommended supply voltage range and at specified free-air temperature

PARAMETER	TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
Regulated output voltage, SCOUT	$R_{L(SCOUT)}$ = 500 Ω	SCIN = 7 V, See Note 7	25°C	−5.2	−5	−4.7	V
		SCIN = 5 V, See Note 8		−4.25	−4	−3.75	
Input regulation	$R_{L(SCOUT)}$ = 500 Ω	SCIN = 7 V to 12 V, See Note 7	Full range		5	25	mV
		SCIN = 5 V to 15 V, See Note 8				27	
Output regulation	$R_{L(SCOUT)}$ = 100 Ω to 500 Ω	SCIN = 7 V, See Note 7	Full range		10	50	mV
		SCIN = 5 V, See Note 8				100	
Voltage loss, SCIN – |SCOUT| (see Note 9)	SCIN = 7 V, CIN = COUT = 100-μF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
		I_O = 100 mA			1.1	1.6	
Output resistance	SCIN = 7 V, ΔI_O = 10 mA to 100 mA, See Note 10		Full range		10	15	Ω
Oscillator frequency			Full range	15	25	35	kHz
Reference voltage, V_{ref}	SCIN = 7 V, I_{ref} = 60 μA		25°C	2.35	2.5	2.65	V
			Full range	2.25		2.75	
	SCIN = 5 V, I_{ref} = 50 μA		25°C	2.35	2.5	2.65	V
			Full range	2.25		2.75	
Maximum switch current			25°C		300		mA
Supply current, I_S	I_O = 0	SCIN = 3.5 V	Full range		2.5	3.5	mA
		SCIN = 15 V			3	4.5	
Supply current in shutdown	$V_{(FB/SD)}$ = 0, I_O = 0	SCIN = 5 V	Full range		100	150	μA

† Data applies for the switched-capacitor block only. Amplifier block is not connected.
‡ Full range is −40°C to 85°C.

NOTES: 7. All regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, CIN = 10 μF (tantalum), COUT = 100 μF (tantalum) and C1 = 0.002 μF (see Figure 63).
8. All regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator with R1 = 23.7 kΩ, R2 = 102.2 kΩ, CIN = 10 μF (tantalum), COUT = 100 μF (tantalum) and C1 = 0.002 μF (see Figure 63).
9. For voltage-loss tests, the switched-capacitor section is connected as a voltage inverter, with SCREF, OSC, and FB/SD unconnected. The voltage losses may be higher in other configurations.
10. Output resistance is defined as the slope of the curve (ΔV_O vs ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

AMPLIFIER AND SWITCHED-CAPACITOR SECTIONS CONNECTED

electrical characteristics, V_{CC+} = 5 V, T_A = 25°C (see Figure 4)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Maximum positive peak output voltage swing, V_{OM+}	R_L = 10 kΩ			3.7		V
	R_L = 600 Ω			3.5		
	R_L = 100 Ω			3.1		
Maximum negative peak output voltage swing, V_{OM-}	R_L = 10 kΩ			−3.7		V
	R_L = 600 Ω			−3.0		
	R_L = 100 Ω			−2.2		
Voltage loss, SCIN – ISCOUTI (see Note 9)	CIN = COUT = 100-μF tantalum, V_{ID} = −100 mV, Both amplifiers	R_L = 10 kΩ		0.46		V
		R_L = 600 Ω		0.50		
		R_L = 100 Ω		0.9		

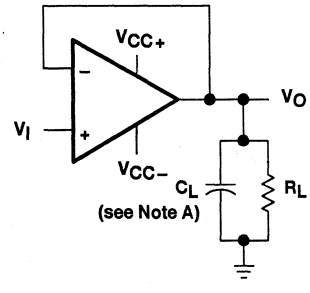
NOTES: 7. All regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, CIN = 10 μF (tantalum), COUT = 100 μF (tantalum) and C1 = 0.002 μF (see Figure 63).
8. All regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator with R1 = 23.7 kΩ, R2 = 102.2 kΩ, CIN = 10 μF (tantalum), COUT = 100 μF (tantalum) and C1 = 0.002 μF (see Figure 63).
9. For voltage-loss tests, the switched-capacitor section is connected as a voltage inverter with SCREF, OSC, and FB/SD unconnected. The voltage losses may be higher in other configurations.
10. Output resistance is defined as the slope of the curve (ΔV_O vs ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

supply current (no load), T_A = 25°C

PARAMETER	TEST CONDITIONS				MIN	TYP	MAX	UNIT
Supply current	V_{CC+} = 5 V,	SCIN = 5 V,	$V_{(FB/SD)}$ = 2.5 V,	V_O = 0		3.4		mA
Supply current in shutdown	V_{CC+} = 5 V,	SCIN = 5 V,	$V_{(FB/SD)}$ = 0 V,	V_O = 0		265		μA

PARAMETER MEASUREMENT INFORMATION

operational amplifier



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

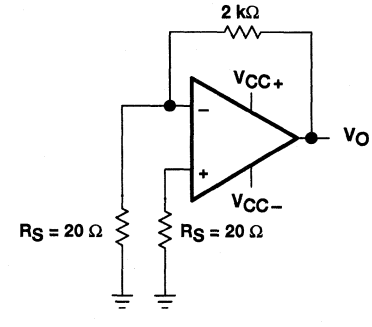
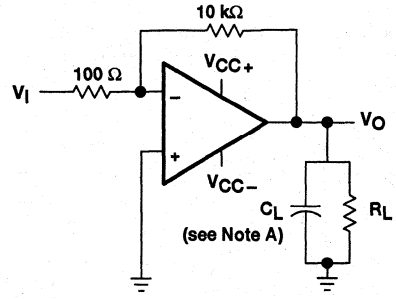


Figure 2. Noise-Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

amplifier input bias offset current

At the picoampere bias-current level typical of the TLE2662, accurate measurement of the amplifier's bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

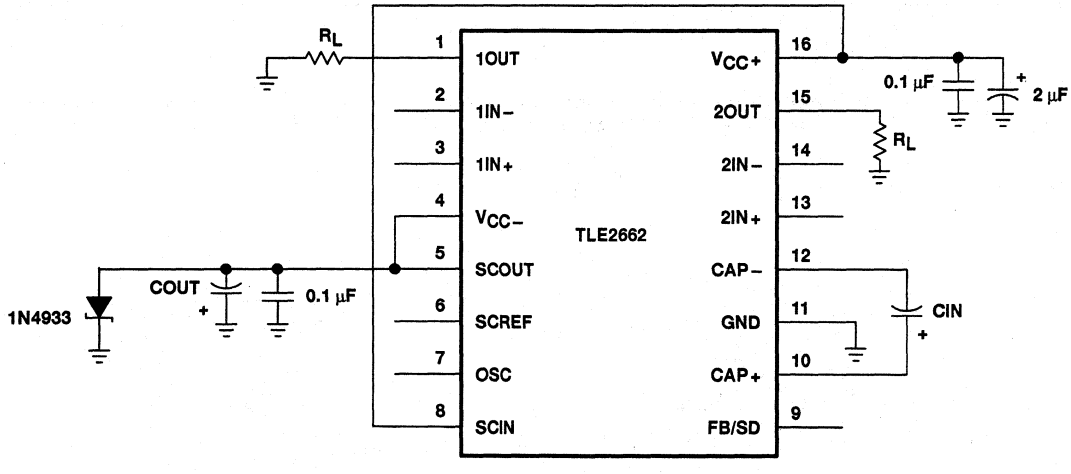


Figure 4. Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

operational amplifier section

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Free-air temperature	6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{IC}	Common-mode input voltage	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage	vs Output current vs Supply voltage	8, 9 10,11,12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14
A_{VD}	Differential voltage amplification	vs Frequency vs Free-air temperature	15 16
I_{OS}	Short-circuit output current	vs Time vs Free-air temperature	17 18
z_o	Output impedance	vs Frequency	19
CMRR	Common-mode rejection ratio	vs Frequency	20
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	21 22
	Pulse response	Small signal Large signal	23, 24 25, 26
	Noise voltage (referenced to input)	0.1 to 10 Hz	27
V_n	Equivalent input noise voltage	vs Frequency	28
THD	Total harmonic distortion	vs Frequency	29, 30
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	31 32
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	33 34 35
	Phase shift	vs Frequency	15

switched-capacitor section

	Shutdown threshold voltage	vs Free-air temperature	36
I_{CC}	Supply current	vs Input voltage	37
f_{osc}	Oscillator frequency	vs Free-air temperature	38
	Supply current in shutdown	vs Input voltage	39
	Average supply current	vs Output current	40
	Output voltage loss	vs Input capacitance vs Oscillator frequency	41 42, 43
V_O	Regulated output voltage	vs Free-air temperature	44
	Reference voltage change	vs Free-air temperature	45
	Voltage loss	vs Output current	46

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

DISTRIBUTION OF INPUT OFFSET VOLTAGE

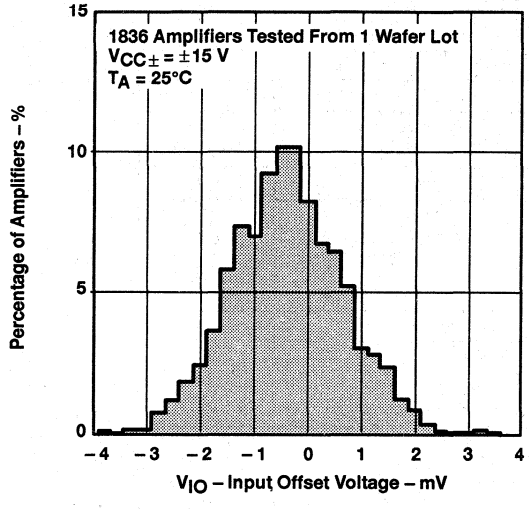


Figure 5

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

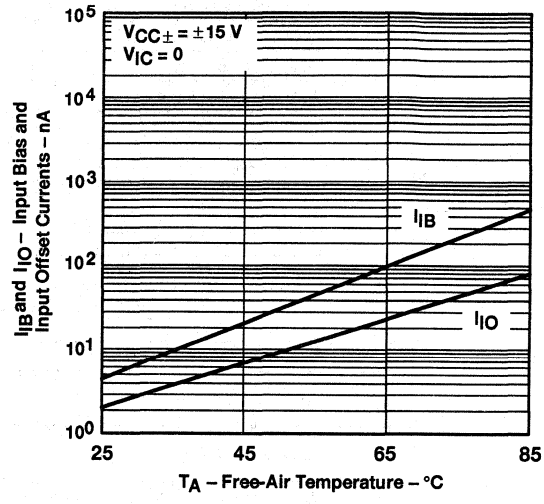


Figure 6

COMMON-MODE INPUT VOLTAGE vs FREE-AIR TEMPERATURE

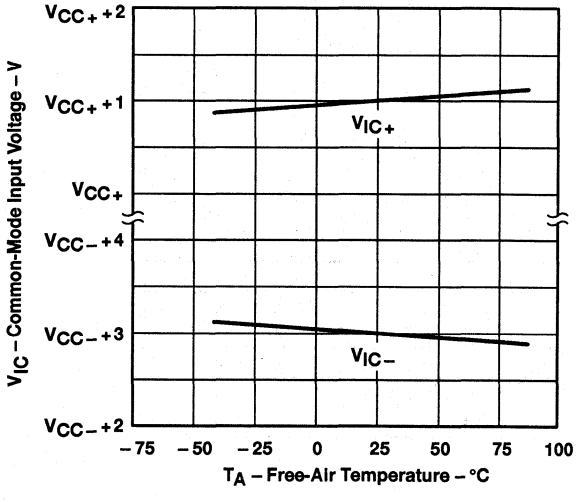


Figure 7

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

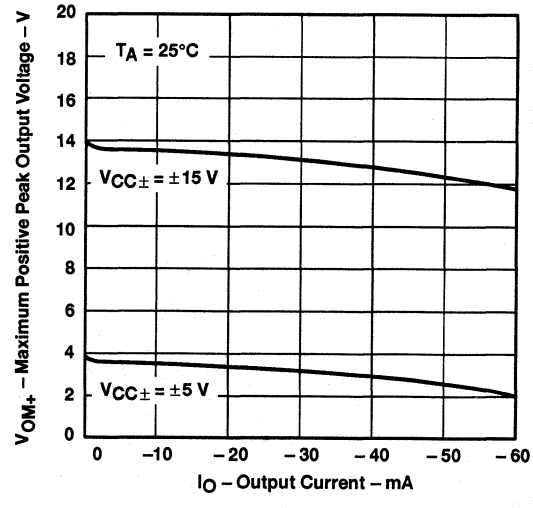


Figure 8

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

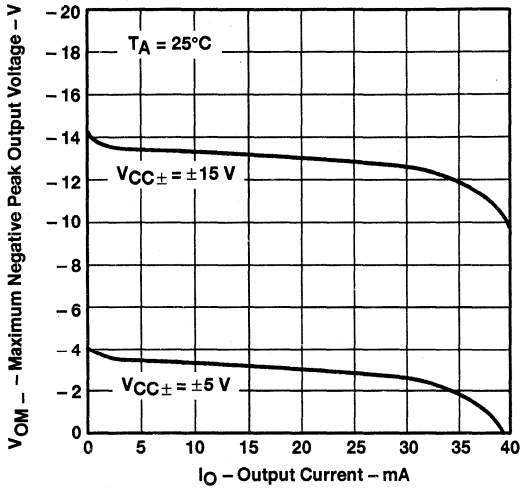


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

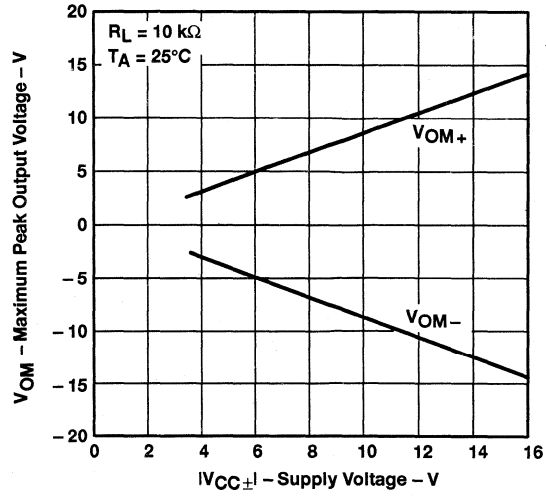


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

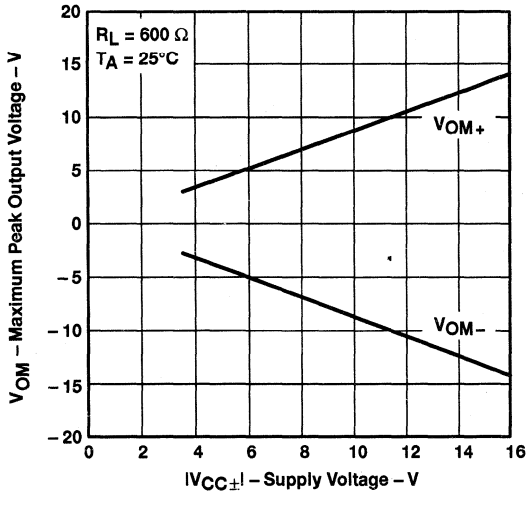


Figure 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

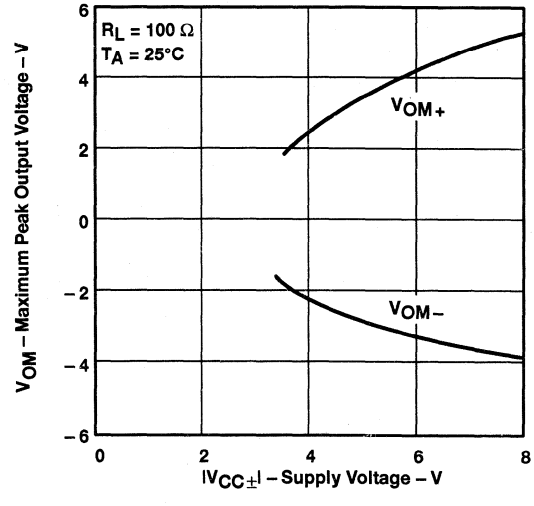


Figure 12

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

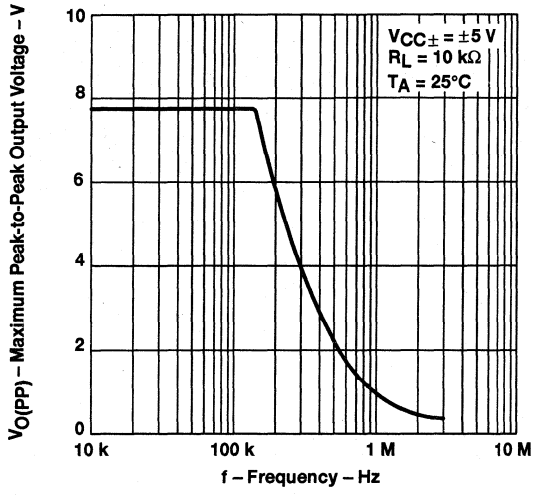


Figure 13

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

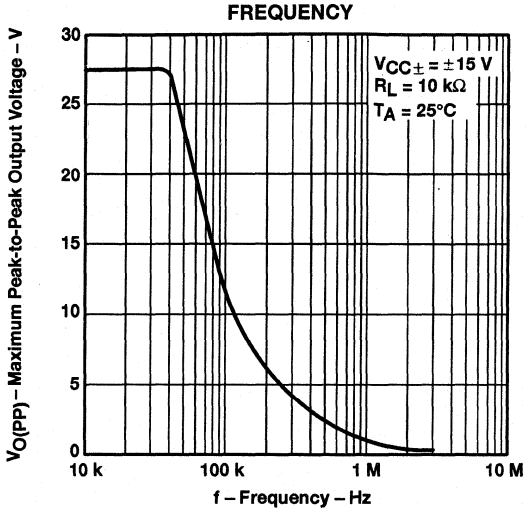


Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

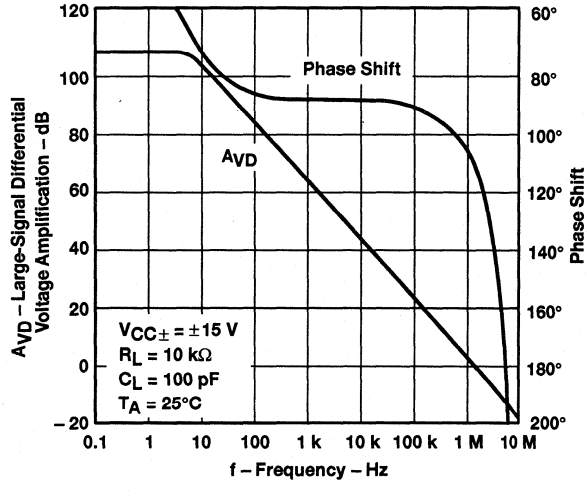


Figure 15

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION
vs
FREE-AIR TEMPERATURE

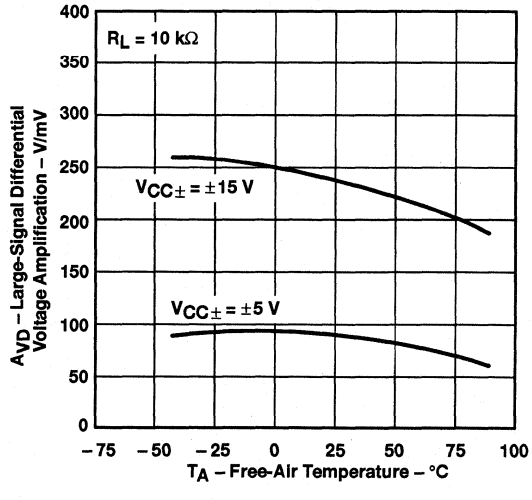


Figure 16

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS† OPERATIONAL AMPLIFIER SECTION

SHORT-CIRCUIT OUTPUT CURRENT vs TIME

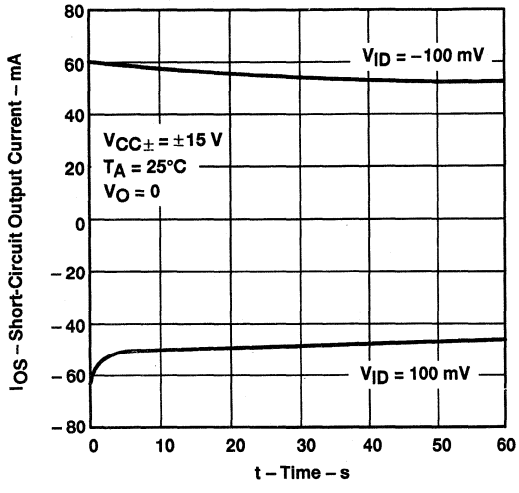


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

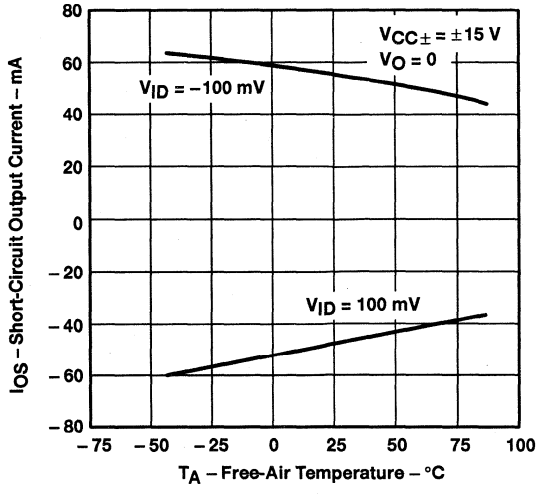


Figure 18

OUTPUT IMPEDANCE vs FREQUENCY

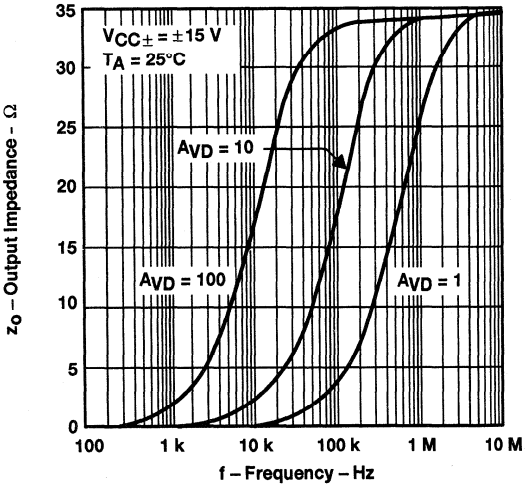


Figure 19

COMMON-MODE REJECTION RATIO vs FREQUENCY

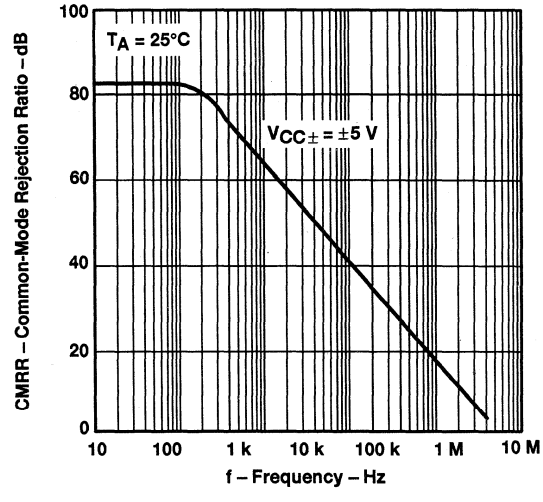


Figure 20

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SUPPLY CURRENT vs SUPPLY VOLTAGE

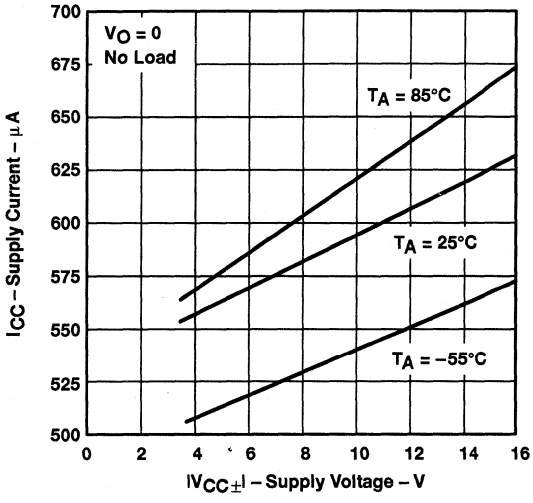


Figure 21

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

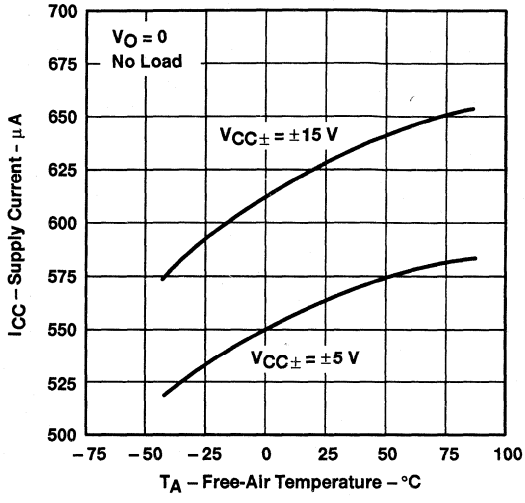


Figure 22

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

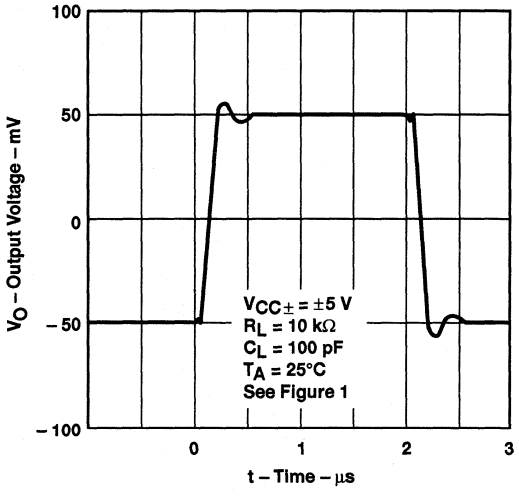


Figure 23

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

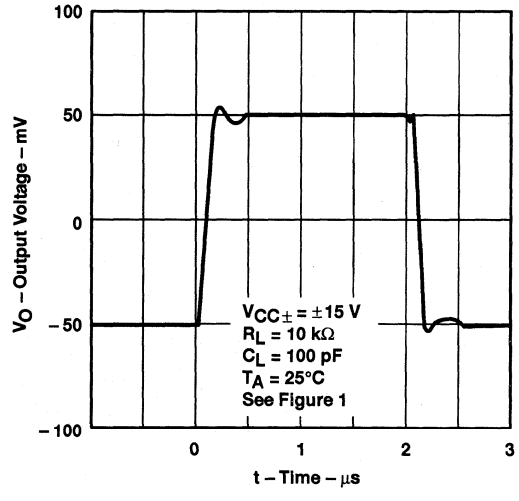


Figure 24

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE

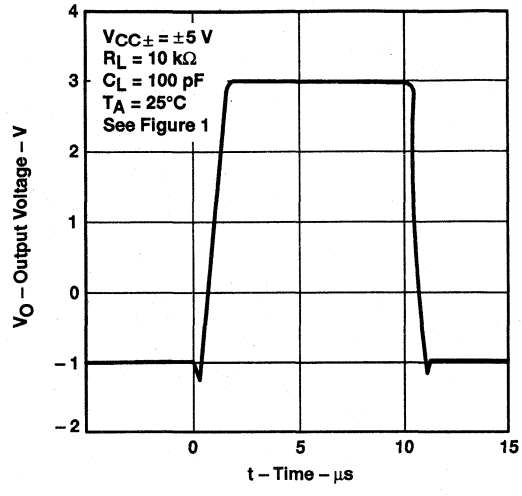


Figure 25

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE

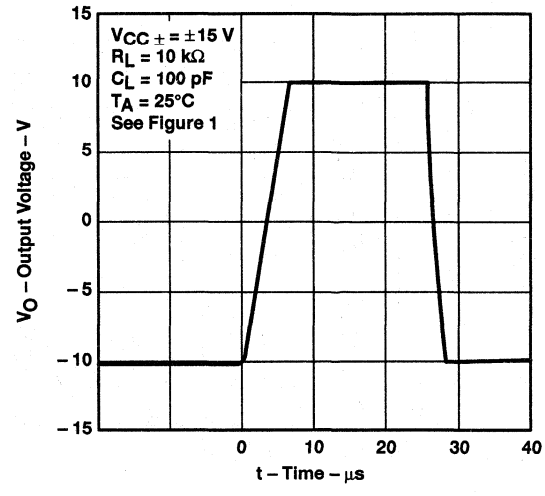


Figure 26

NOISE VOLTAGE
(REFERRED TO INPUT)
0.1 TO 10 Hz

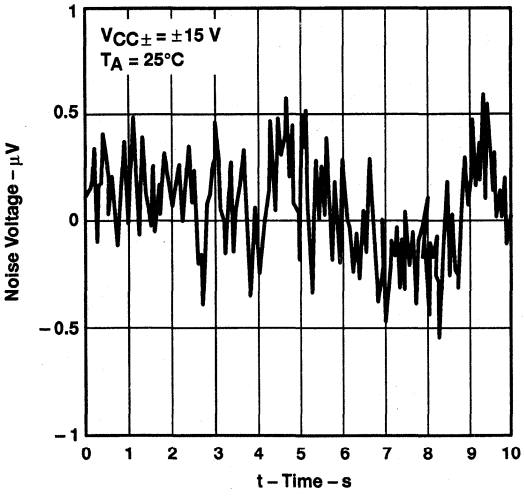


Figure 27

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

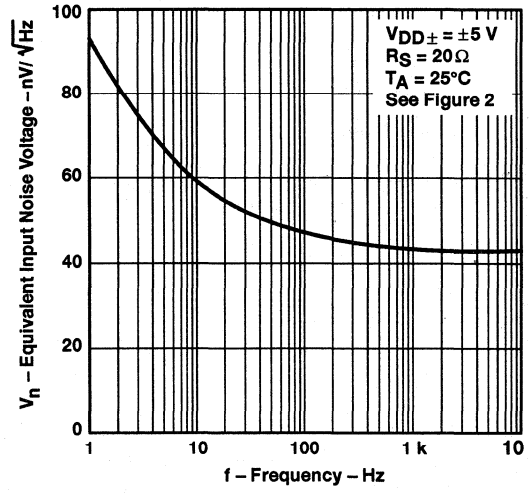


Figure 28

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

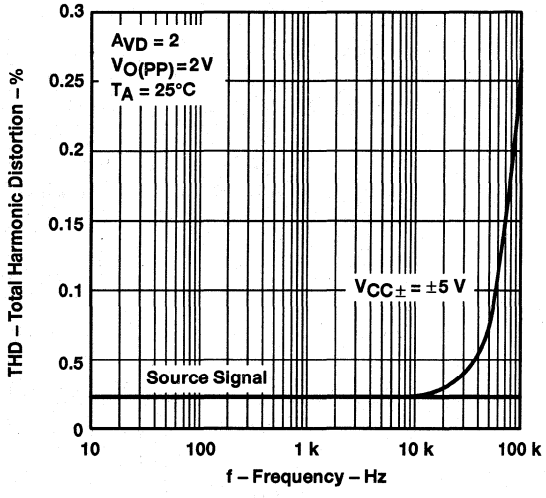


Figure 29

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

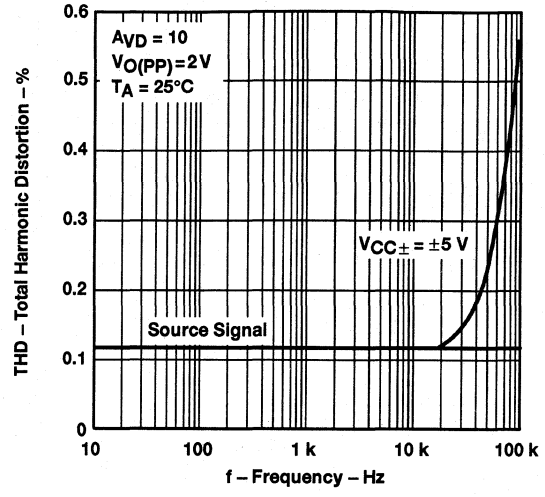


Figure 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

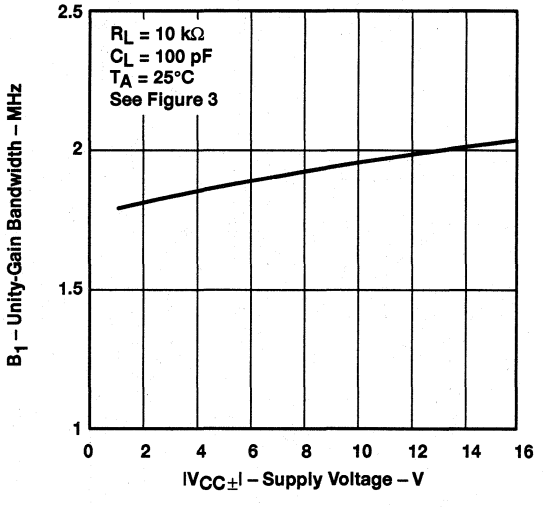


Figure 31

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

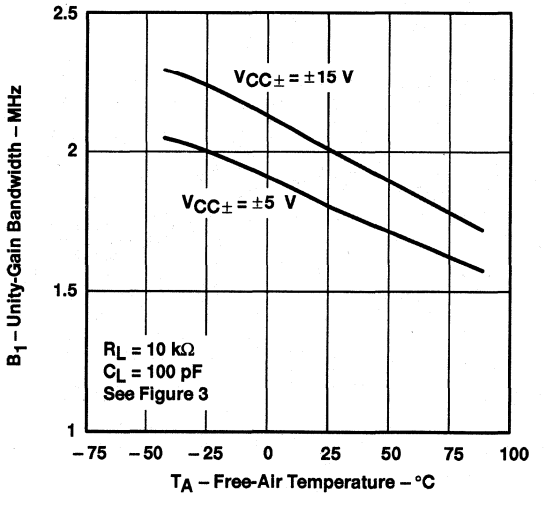


Figure 32

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

PHASE MARGIN
vs
SUPPLY VOLTAGE

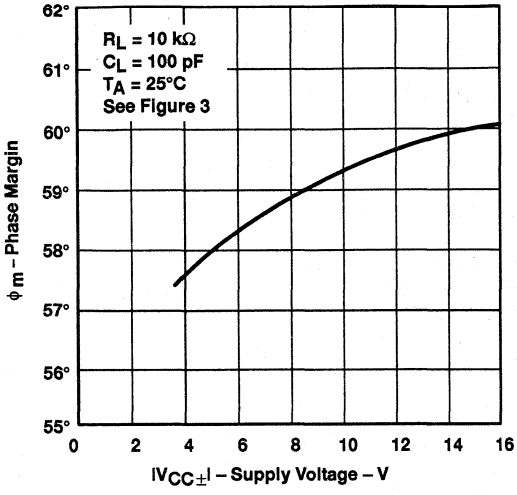


Figure 33

PHASE MARGIN
vs
LOAD CAPACITANCE

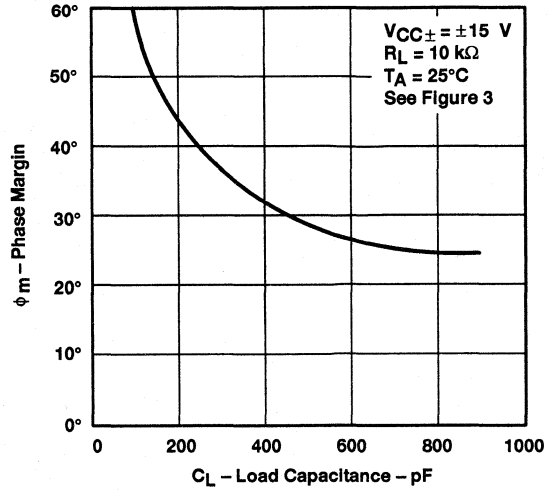


Figure 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

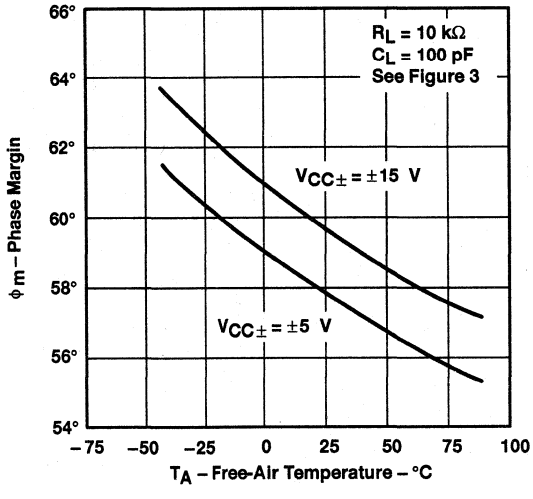


Figure 35

† Data applies for the amplifier block only; the switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

SHUTDOWN THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

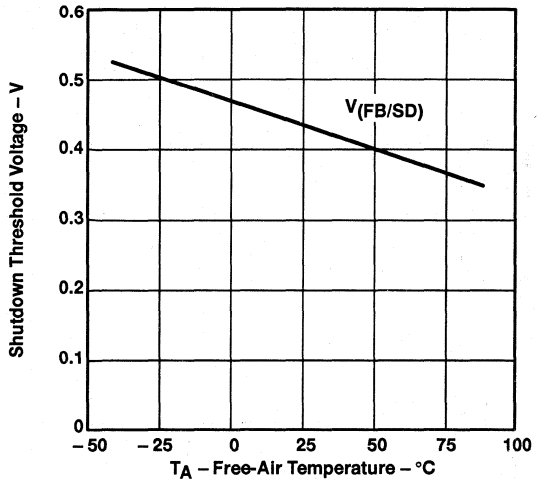


Figure 36

SUPPLY CURRENT vs INPUT VOLTAGE

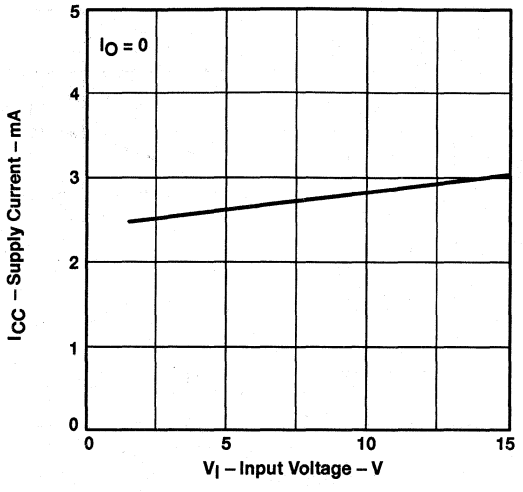


Figure 37

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

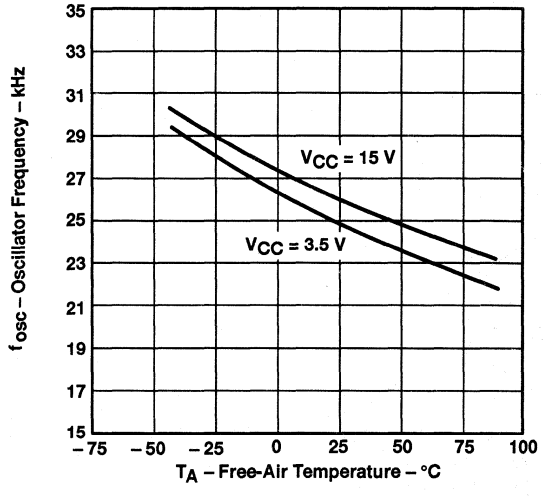


Figure 38

SUPPLY CURRENT IN SHUTDOWN vs INPUT VOLTAGE

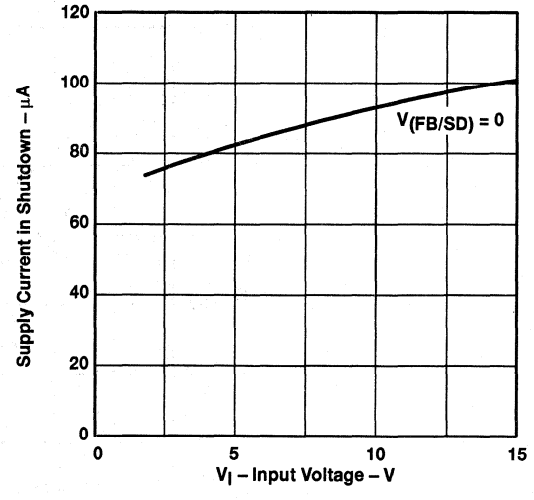


Figure 39

† Data applies for the switched-capacitor block only. Amplifier block is not connected.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

AVERAGE SUPPLY CURRENT vs OUTPUT CURRENT

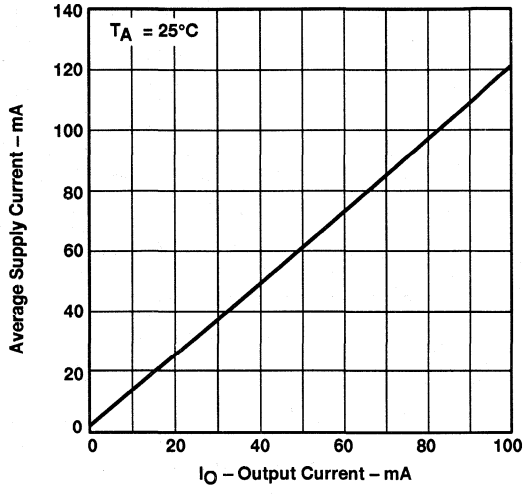


Figure 40

OUTPUT VOLTAGE LOSS vs INPUT CAPACITANCE

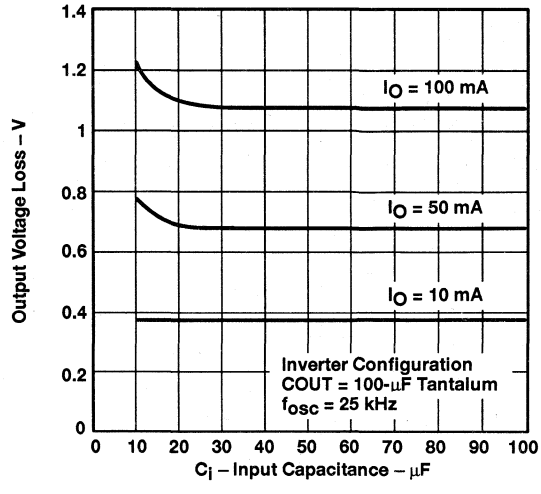


Figure 41

OUTPUT VOLTAGE LOSS vs OSCILLATOR FREQUENCY

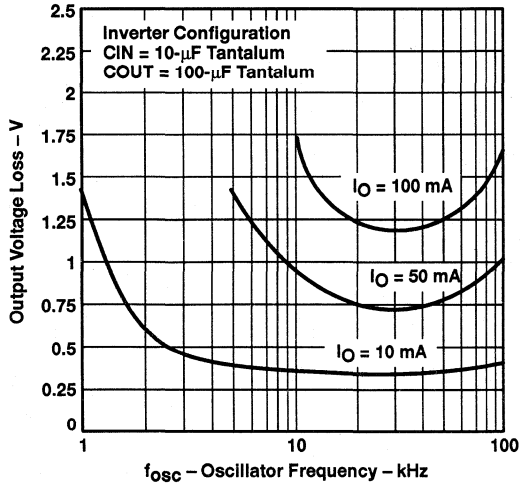


Figure 42

OUTPUT VOLTAGE LOSS vs OSCILLATOR FREQUENCY

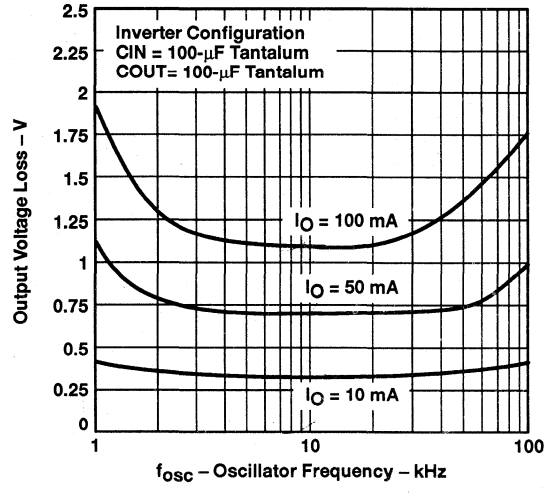


Figure 43

† Data applies for the switched-capacitor block only. Amplifier block is not connected.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

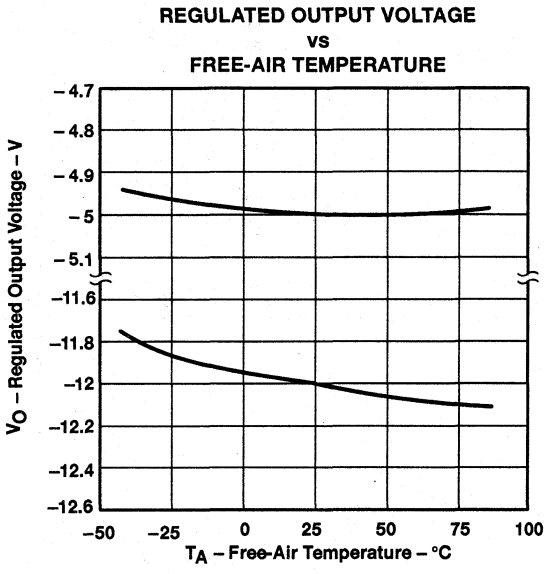


Figure 44

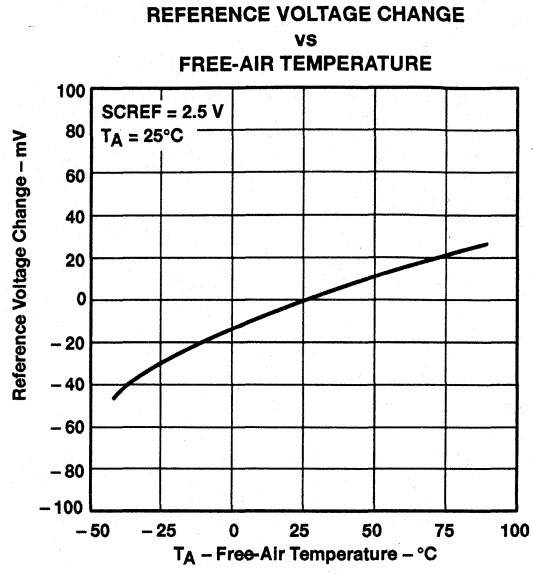


Figure 45

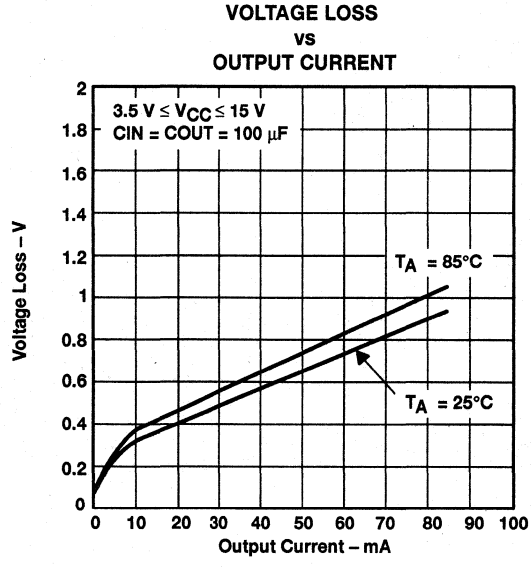


Figure 46

† Data applies for the switched-capacitor block only. Amplifier block is not connected.

APPLICATION INFORMATION

amplifier section

input characteristics

The TLE2662 is specified with a minimum and a maximum input voltage that if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2662 operational amplifier section is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 47). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

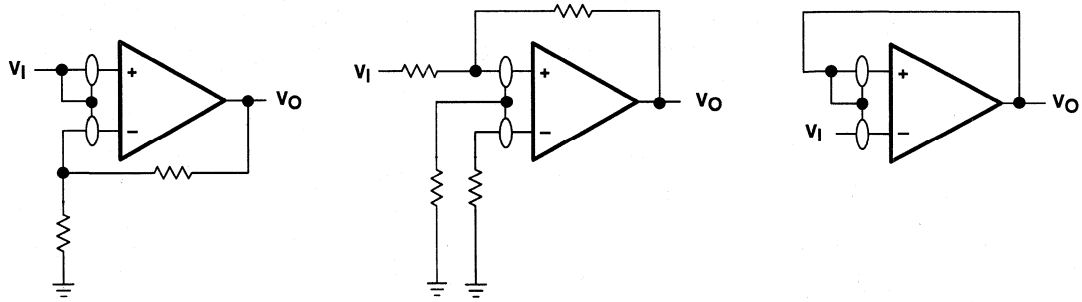
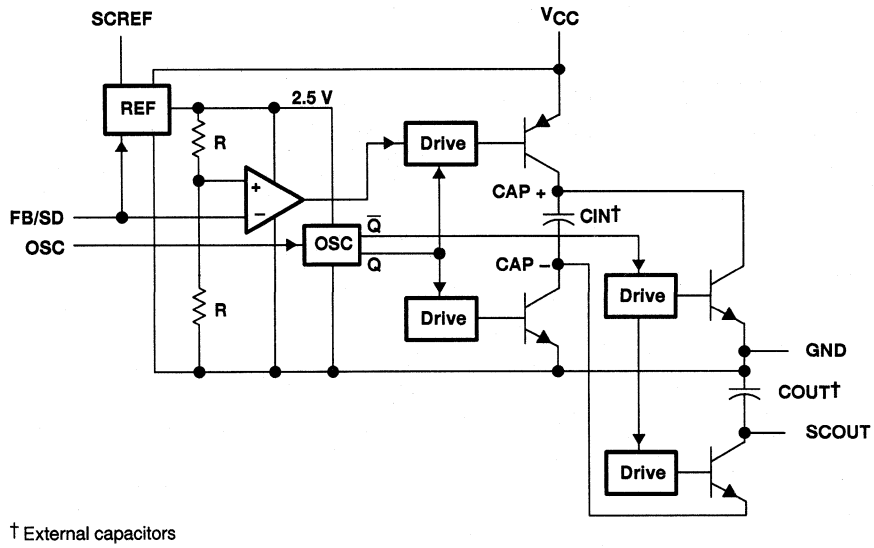


Figure 47. Use of Guard Rings

switched-capacitor section



† External capacitors

Figure 48. Functional Block Diagram for Switched-Capacitor Block Only

APPLICATION INFORMATION

switched-capacitor section (continued)

The TLE2662, with its high-output-drive amplifiers and switched-capacitor voltage converter, readily lends itself to applications like headphone drivers where large signal swing into heavy loads is paramount. Another application is analog-to-digital interfacing when only a single rail is available to the system, but maximization of the ADC dynamic range is key. See Figure 48 for the functional block diagram of the switched-capacitor block.

typical application

In its most basic configuration, the TLE2662 switched-capacitor section is used as a voltage inverter to provide the negative rail for the amplifiers in a single-supply system. As shown in Figure 49, the positive 5-V supply is connected to both V_{CC+} and SCIN. V_{CC-} is connected to the output of the charge pump, SCOUT. Only three external components (excluding the resistors used with the amplifiers) are necessary: the storage capacitors, CIN and COUT, and a fast-recovery Schottky diode to clamp SCOUT during start up. The diode is necessary because the amplifiers present a load referenced to the positive rail and tends to pull SCOUT above ground, which can cause the device to fail to start up (see pin functions section in APPLICATION INFORMATION). As shown in Figure 50, one amplifier is shown driving a resistive load; the other is interfacing to an analog-to-digital converter (ADC).

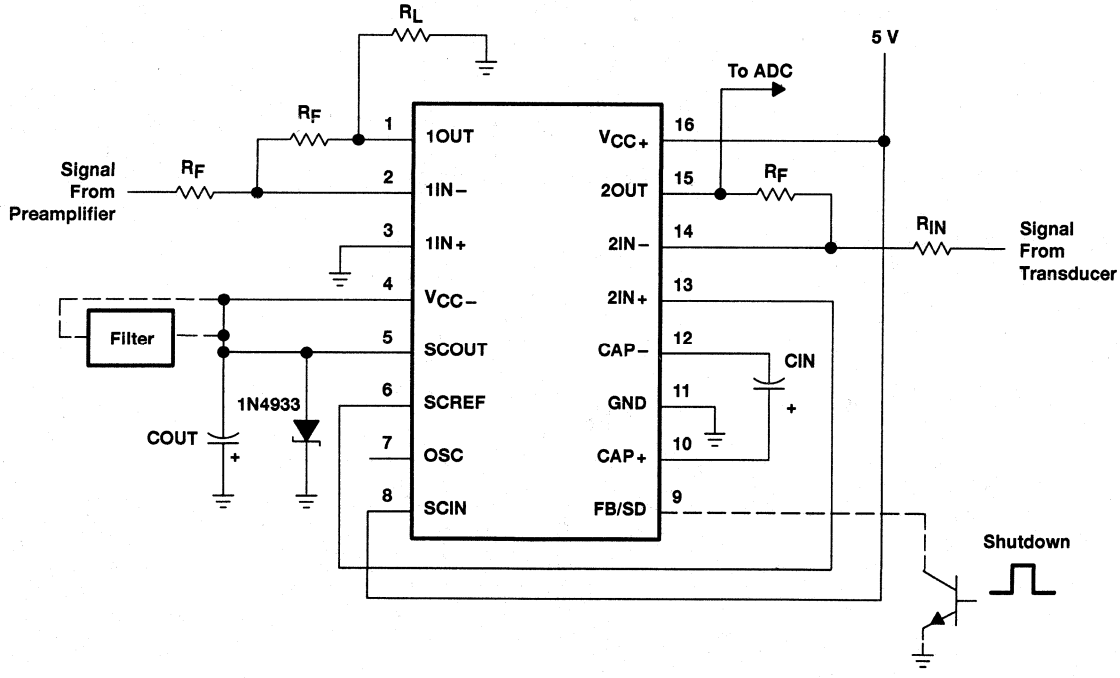


Figure 49. Switched-Capacitor Block Supplying Negative Rail for Amplifiers

APPLICATION INFORMATION

typical application (continued)

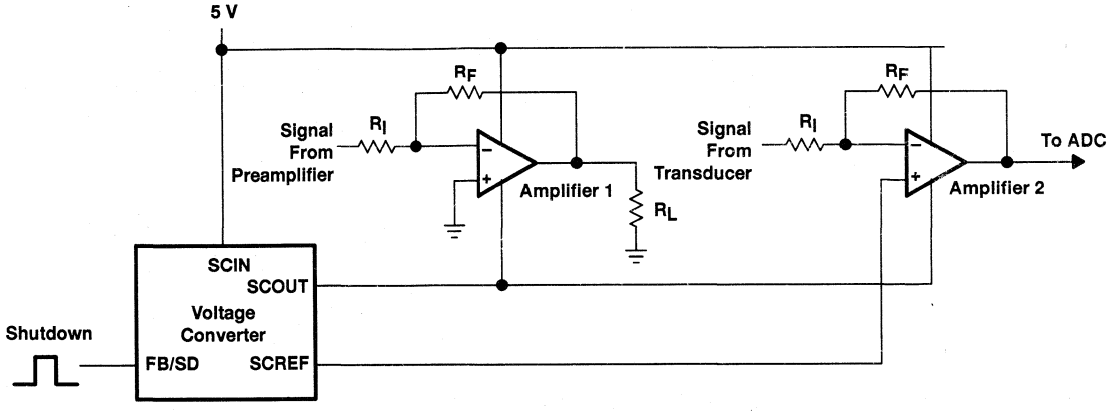


Figure 50. Equivalent Schematic: Amplifier 1 Driving Resistive Load, Amplifier 2 Interfacing to an ADC

Though simple, this configuration has the inherent disadvantage of having ripple and switching-noise components on SCOUT. These are coupled into the amplifier's signal path, effectively introducing distortion into the output waveform. The effect is most pronounced when the outputs are driven low, loading the negative rail generated by the charge pump. A first approach to minimizing these effects is to increase the size of COUT using a low-ESR type capacitor (refer to the switched-capacitor selection section under capacitor selection and output ripple). Figures 51 and 52 compare the ripple and noise present at the amplifier output with COUT = 10 μF and COUT = 100 μF, respectively, with the outputs driven low into a 600-Ω load.

RIPPLE AND SWITCHING NOISE ON AMPLIFIER OUTPUT vs TIME

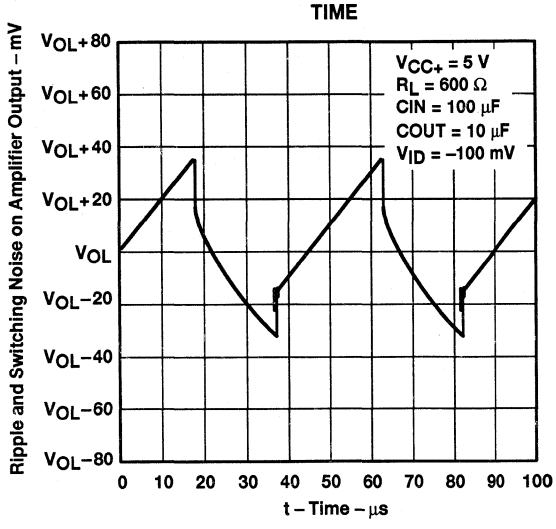


Figure 51

RIPPLE AND SWITCHING NOISE ON AMPLIFIER OUTPUT vs TIME

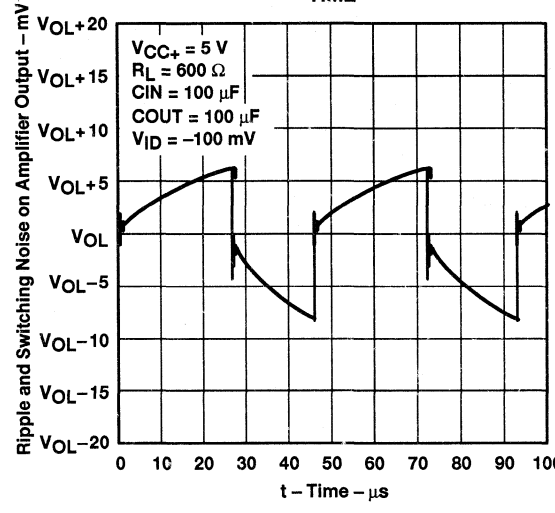


Figure 52

APPLICATION INFORMATION

typical application (continued)

Additional filtering can be added between SCOUT and V_{CC-} to further reduce ripple and noise. For example, adding the simple low-pass LC filter shown in Figure 53, implemented using a 50-μH inductor and 220-μF capacitor (available in surface mount), results in the reduced levels of ripple and switching noise at the amplifier's outputs (see Figures 54 and 55). Larger values of L or C can be used for even better attenuation.

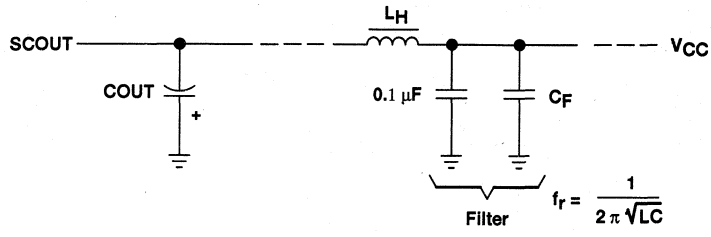


Figure 53. LC Filter Used to Reduce Ripple and Switching Noise, $f_r = 1/2\pi\sqrt{LC}$, A = –40 dB Per Decade

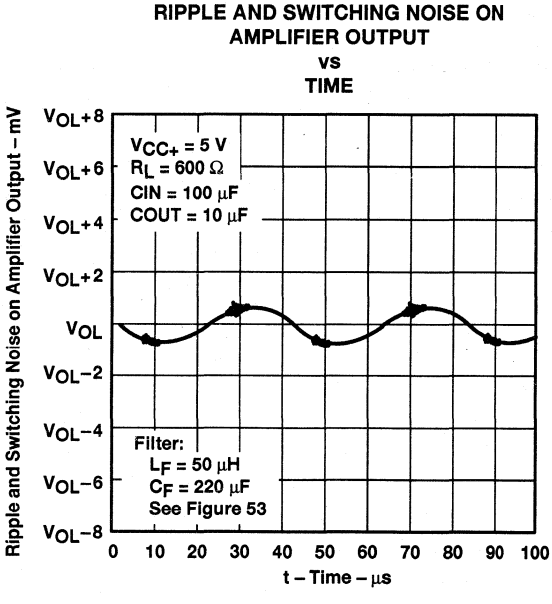


Figure 54

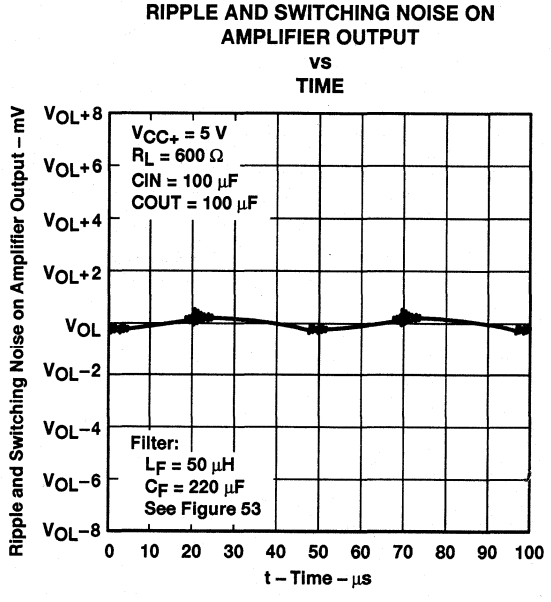


Figure 55

APPLICATION INFORMATION

precision measurement techniques

In systems where the amplifier outputs are being sampled by an analog-to-digital converter (ADC), the switched-capacitor network can be temporarily disabled by applying a voltage of less then 0.45 V to FB/SD. This is easily accomplished using any open-collector gate (shown by dashed lines in Figure 49). When disabled, the internal switches are set to dump any remaining charge onto COUT. The voltage at SCOUT decays to zero at a rate dependent on both the size of COUT and loading. During this time, the amplifier's outputs are free of any switching-induced ripple and noise. Figure 56 shows the relationship of the output voltage decay time to the size of the output storage capacitor when one channel of the amplifier is driving a 100-Ω load to ground. SCOUT rises again when the external gate is turned off (see Figure 57).

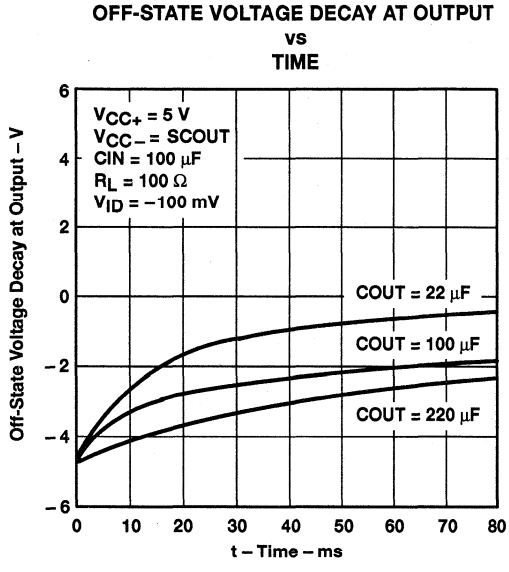


Figure 56

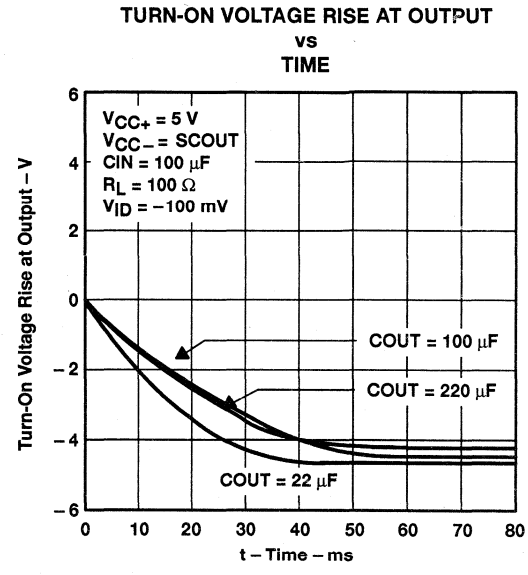


Figure 57

The amplifier's negative input common-mode voltage limit (V_{ICR-}) is specified as an offset from the negative rail. Care should be taken to ensure that the input signal does not violate this limit as SCOUT decays. The negative output voltage swing is similarly affected by the gradual loss of the negative rail.

This application takes advantage of the otherwise unused SCREF output of the switched-capacitor block to bias one amplifier to 2.5 V. This is especially useful when the amplifier is followed by an ADC, keeping the signal centered in the middle of the converter dynamic range. Other biasing methods may be necessary in precision systems.

In Figure 58, SCREF, R1, and R2 are used to generate a feedback voltage to the TLE2662 error amplifier. This voltage, fed into FB/SD, is used to regulate the voltage at SCOUT. When used this way, there is higher voltage loss (SCIN – ISCOUTI) associated with the regulation. For example, the inverter generates an unregulated voltage of approximately –4.5 V from a positive 5-V source; it can achieve a regulated output voltage of only about –3.5 V. Though this reduces the amplifier input and output dynamic range, both V_{ICR-} and V_{OL} still extend to below ground.

APPLICATION INFORMATION

precision measurement techniques (continued)

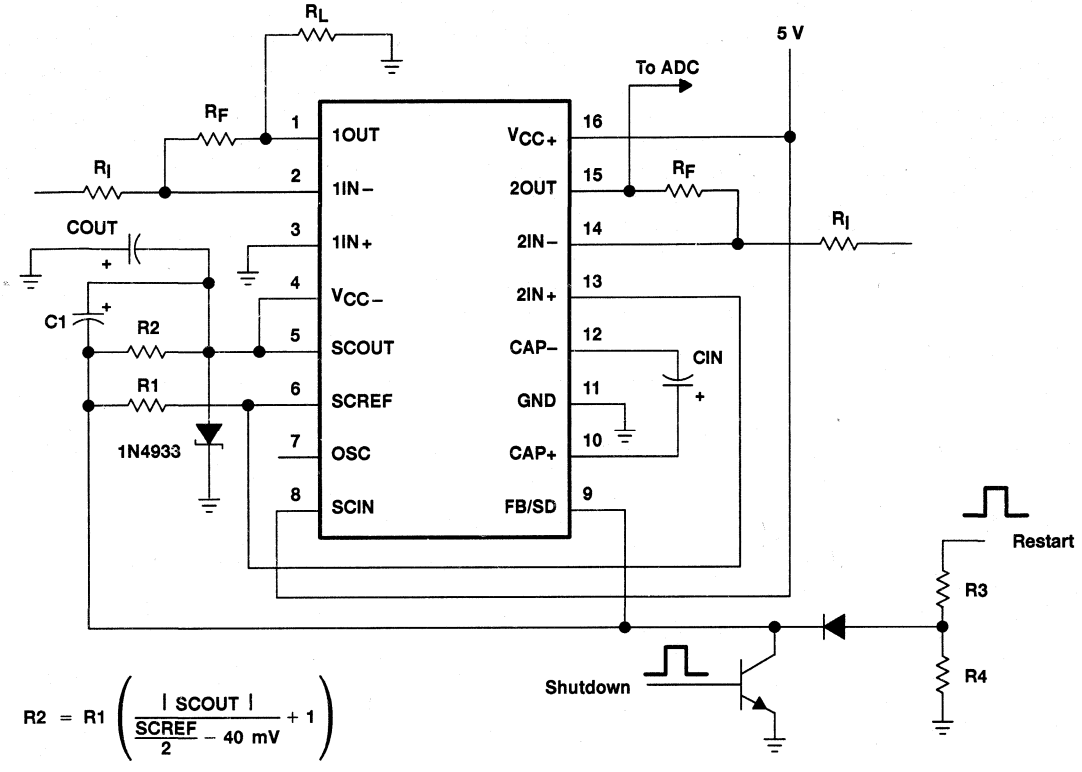


Figure 58. Voltage Inverter With Regulated Output

The reference voltage, though being used as part of the regulation circuitry, is still available for other uses if total current drawn from it is limited to under 60 μA. The shutdown feature also remains available, though a restart pulse may be necessary to start the switched-capacitor if the voltage on COUT is not fully discharged. This restart pulse is isolated from the feedback loop using a blocking diode in the regulation section.

The circuit designer should be aware that the TLE2662 amplifier and switched-capacitor sections are tested and specified separately. Performance may differ from that shown in the typical characteristics section when used together. This is evident, for example, in the dependence of V_{ICR-} and V_{OL} on V_{CC-}. The impact of supplying the amplifier negative rail using the switched-capacitor block in each design should be considered and carefully evaluated.

The more esoteric features of the switched-capacitor building block, including external synchronization of the internal oscillator and power dissipation considerations, are covered in detail in the following section.

APPLICATION INFORMATION

switched-capacitor function

A review of a basic switched-capacitor building block is helpful in understanding the operation of the TLE2662. When the switch shown in Figure 59 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is q1 = C1V1. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is q2 = C1V2. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is as shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \quad (1)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is shown in equation 2.

$$I = f \times \Delta q = f \times C1(V1 - V2) \quad (2)$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}} \quad (3)$$

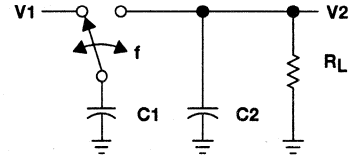


Figure 59. Switched-Capacitor Block

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div fC1$. The equivalent circuit for the switched-capacitor network is as shown in Figure 60. The TLE2662 has the same switching action as the basic switched-capacitor voltage converter. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 43). As oscillator frequency is decreased, the output impedance is eventually dominated by the 1/fC1 term and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise. The oscillator of the TLE2662 switched-capacitor section is designed to run in the frequency band where voltage losses are at a minimum.

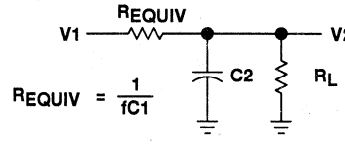


Figure 60. Switched-Capacitor Equivalent Circuit

APPLICATION INFORMATION

pin functions (see functional block diagram – converter)

Supply voltage (SCIN) alternately charges CIN to the input voltage when CIN is switched in parallel with the input supply, and then transfers charge to COUT when CIN is switched in parallel with COUT. Switching occurs at the oscillator frequency. During the time that CIN is charging, the peak supply current is approximately 2.2 times the output current. During the time that CIN is delivering a charge to COUT, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the TLE2662 switched-capacitor section and averages out the current drawn from the supply. A minimum input supply bypass capacitor of 2 μF, preferably tantalum or some other low-ESR type, is recommended. A larger capacitor is desirable in some cases. An example is when the actual input supply is connected to the TLE2662 through long leads or when the pulse currents drawn by the TLE2662 might affect other circuits through supply coupling.

In addition to being the output pin, SCOUT is tied to the substrate of the device. Special care must be taken in TLE2662 circuits to avoid making SCOUT positive with respect to any of the other pins. For circuits with the output load connected from V_{CC+} to SCOUT or from some external positive supply voltage to SCOUT, an external Schottky diode must be added (see Figure 61). This diode prevents SCOUT from being pulled above the GND during start up. A fast-recovery diode such as IN4933 with low forward voltage ($V_f \approx 0.2$ V) can be used.

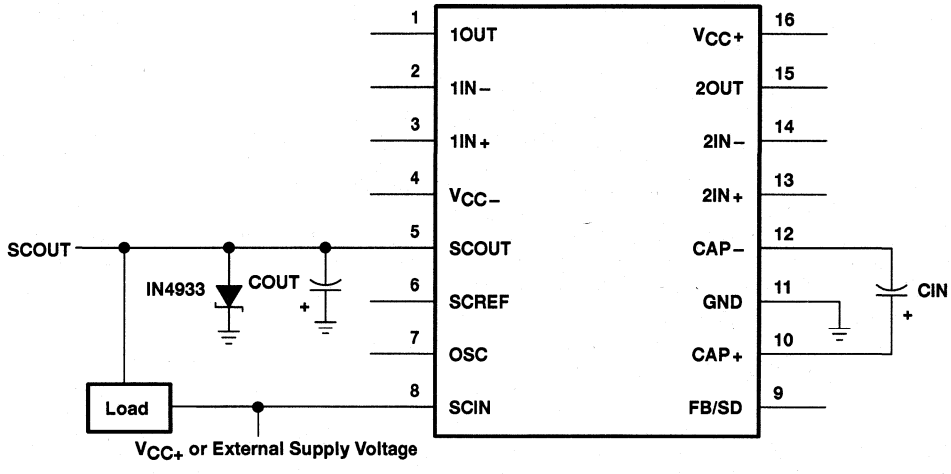


Figure 61. Circuit With Load Connected From V_{CC} to SCOUT

The voltage reference (SCREF) output provides a 2.5-V reference point for use in TLE2662-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator-feedback networks, reference output current should be limited to approximately 60 μA. SCREF draws approximately 100 μA when shorted to ground and does not affect the internal reference/regulator. This pin can also be used as a pullup for TLE2662 circuits that require synchronization.

APPLICATION INFORMATION

pin functions (continued)

CAP+ is the positive side of input capacitor (CIN) and is alternately driven between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP– is the negative side of the input capacitor and is driven alternately between ground and SCOUT. When driven to ground, CAP– sinks current to ground. When driven to SCOUT, CAP– sources current from COUT. In all cases, current flow in the switches is unidirectional as should be expected when using bipolar switches.

OSC can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is alternately charged and discharged by current sources of ±7 μA, so that the duty cycle is approximately 50%. The TLE2662 switched-capacitor section oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 62) in the range of 5 pF–20 pF from CAP+ to OSC. This capacitor couples a charge into C_t at the switch transitions. This shortens the charge and discharge time and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to SCREF. A 20-kΩ pullup resistor is recommended. An open-collector gate or an npn transistor can then be used to drive OSC at the external clock frequency as shown in Figure 62. The frequency can be lowered by adding an external capacitor (C_1 in Figure 62) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.

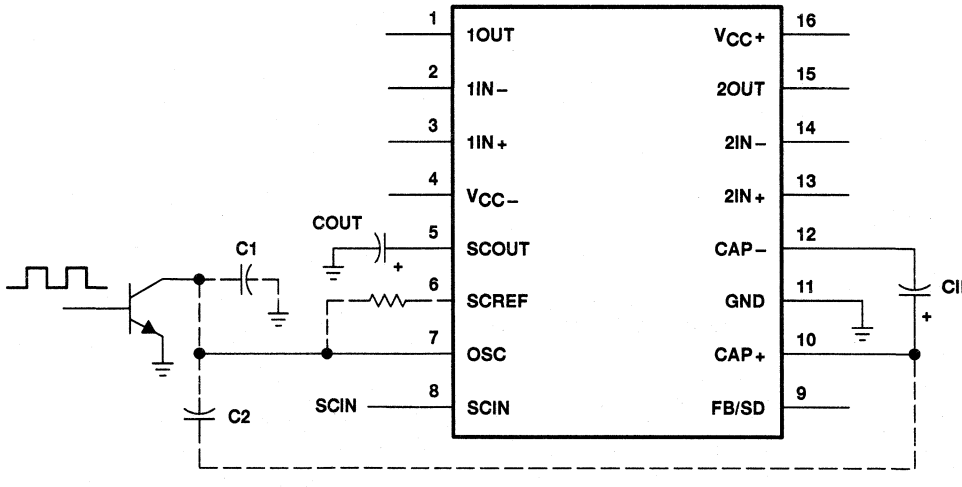


Figure 62. External Clock System

The feedback/shutdown (FB/SD) pin has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both CIN and COUT are discharged through the output load. Quiescent current in shutdown drops to approximately 100 μA . Any open-collector gate can be used to put the TLE2662 into shutdown. For normal (unregulated) operation, the device restarts when the external gate is shut off. In TLE2662 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (COUT) has fully discharged. For most applications where the TLE2662 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start-up before the output capacitor (COUT) has fully discharged, a restart pulse must be applied to FB/SD of the TLE2662.

APPLICATION INFORMATION

pin functions (continued)

Using the circuit shown in Figure 63, the restart signal can be either a pulse (t_p > 100 μs) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 63 should be chosen to provide a signal level at FB/SD of 0.7 V–1.1 V. FB/SD is also the inverting input of the TLE2662 switched-capacitor section error amplifier, and as such can be used to obtain a regulated output voltage.

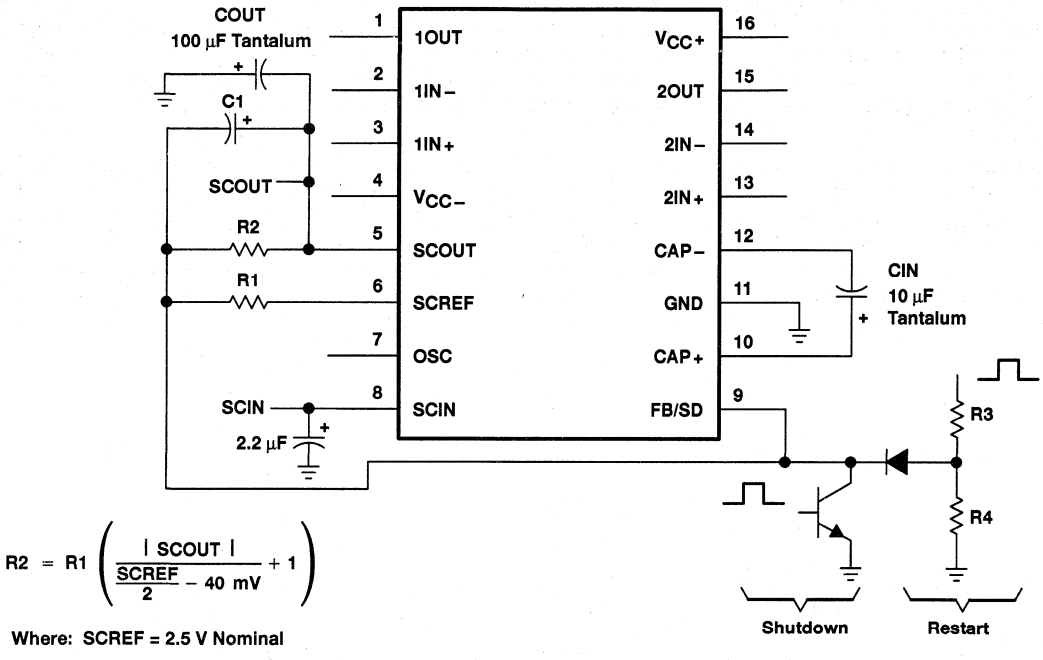


Figure 63. Basic Regulation Configuration

regulation

The error amplifier of the TLE2662 switched-capacitor section drives the npn switch to control the voltage across the input capacitor (CIN), which determines the output voltage. When the reference and error amplifier of the TLE2662 is used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 63 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 μA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of CIN to COUT. For best results, this ratio should be approximately 1 to 10. Capacitor C1, required for good load regulation, should be 0.002 μF for all output voltages.

APPLICATION INFORMATION

regulation (continued)

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, | SCOUT | referenced to GND of the TLE2662 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves.

capacitor selection

While the exact values of CIN and COUT are noncritical, good-quality low-ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For CIN, the effect of the equivalent series resistance (ESR) of the capacitor is multiplied by four, since switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for CIN has the same effect as increasing the output impedance of the switched-capacitor section by 4 Ω. This represents a significant increase in the voltage losses. COUT is alternately charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as shown in equation 4:

$$\Delta V = \frac{I_O}{2\ fC_O} \tag{4}$$

where:

ΔV = peak-to-peak ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to equation 5:

$$\left(2I_O\right)\left(\text{ESR of } C_O\right) \tag{5}$$

power dissipation (switched-capacitor section only)

The power dissipation of any TLE2662 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation is calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the TLE2662 is calculated as shown in equation 6:

$$P \approx (V_{CC} - |V_O|)\ I_O + (V_{CC})\ (I_O)\ (0.2) \tag{6}$$

where both V_{CC} and SCOUT refer to GND. The power dissipation is equivalent to that of a linear regulator. Due to limitations of the DW package, steps must be taken to dissipate power externally for large input or output differentials. This is accomplished by placing a resistor in series with CIN as shown in Figure 64. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when CIN is both charging and discharging, the resistor chosen is as shown in equation 7.

APPLICATION INFORMATION

power dissipation (continued)

$$R_X = V_X/(4.4\ I_O) \quad (7)$$

where:

$$V_X \approx V_{CC} - \left[(\text{TLE2662 voltage loss})\ (1.3) + |\ V_O\ |\right]$$

and I_{OUT} = maximum required output current. The factor of 1.3 allows some operating margin for the TLE2662. When using a 12-V to −5-V converter at 100-mA output current, calculate the power dissipation without an external resistor as shown in equation 8.

$$P = (12\ V - |\ -5\ V\ |)\ (100\ mA) + (12\ V)\ (100\ mA)\ (0.2) \quad (8)$$

$$P = 700\ mW + 240\ mW = 940\ mW$$

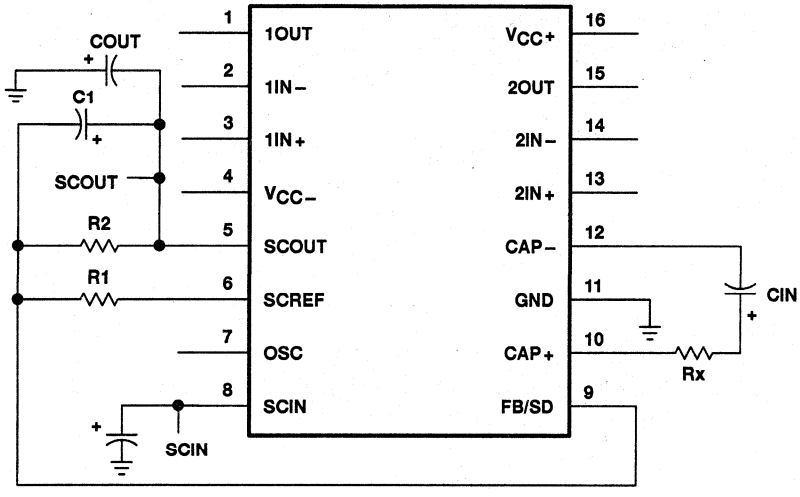


Figure 64. Power-Dissipation-Limiting Resistor in Series With CIN

At θ_{JA} of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C is seen. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external-resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the TLE2662 in the standard regulator configuration at 100 mA output current is 1.6 V (see equation 9).

$$V_X = 12\ V - \left[(1.6\ V)\ (1.3) + |\ -5\ V\ |\right] = 4.9\ V \quad (9)$$

and

$$R_X = 4.9\ V/(4.4)\ (100\ mA) = 11\ \Omega$$

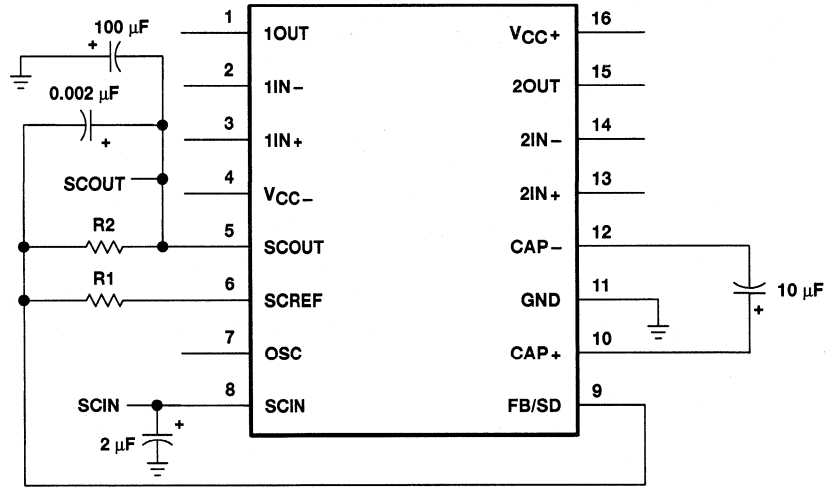
APPLICATION INFORMATION

power dissipation (continued)

The resistor reduces the power dissipated by the TLE2662 by (4.9 V) (100 mA) = 490 mW. The total power dissipated by the TLE2662 is equal to (940 mW – 490 mW) = 450 mW. The junction temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the TLE2662 packages represent worst-case numbers with no heat sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the TLE2662 package. Airflow in some systems helps to lower the thermal resistance. Wide PC board traces from the TLE2662 leads helps to remove heat from the device. This is especially true for plastic packages.

basic voltage inverter

The switched-capacitor block is connected as a basic voltage inverter with regulation as shown in Figure 65. The magnitude of SCIN must exceed that of the desired SCOUT to accommodate voltage losses due to switching and regulation. Losses of 1 V to 2 V are typical.



$$R2 = R1\left(\frac{|\,SCOUT\,|}{\frac{SCREF}{2} - 40\ mV} + 1\right) = R1\left(\frac{|\,SCOUT\,|}{1.121\ V} + 1\right)$$

Figure 65. Basic Voltage Inverter/Regulator

APPLICATION INFORMATION

positive voltage doubler

In this configuration, the voltage converter is configured as a positive voltage doubler providing a higher positive rail, approximately 9 V for the amplifiers or other external circuitry. Filtering (not shown) of the output of the doubler may be necessary.

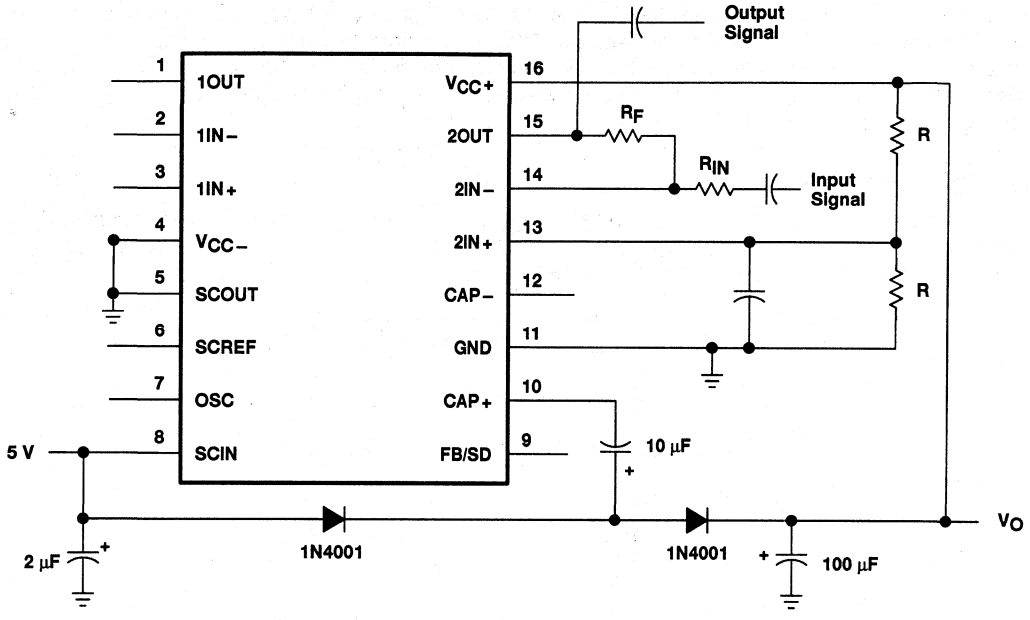


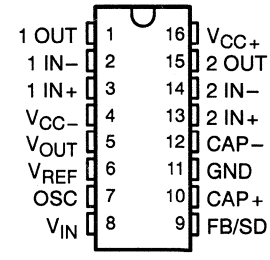
Figure 66. Voltage Converter Configured as Positive Doubler

HIGH-SPEED JFET-INPUT DUAL OPERATIONAL AMPLIFIER WITH SWITCHED-CAPACITOR VOLTAGE CONVERTER

SLOS127 – D4089, JUNE 1993

- **Single-Supply Operation With Rail-to-Rail Inputs**
- **± 30-mA Min Short-Circuit Output Current**
- **Wide V_{CC} Range . . . 3.5 V to 15 V**
- **V_{OUT} Supplies up to 100 mA for External Loads**
- **Shutdown Mode**
- **External 2.5-V Voltage Reference Available**
- **40-V/μs Slew Rate Typ**
- **High Gain-Bandwidth Product . . . 10 MHz**

DW PACKAGE
(TOP VIEW)



description

The TLE2682 offers the advantages of JFET-input operational amplifiers and rail-to-rail common-mode input voltage range with the convenience of single-supply operation. By combining a switched-capacitor voltage converter with a dual operational amplifier in a single package, Texas Instruments now gives circuit designers new options for conditioning low-level signals in single-supply systems.

The TLE2682 features two high-speed, high-output drive JFET-input operational amplifiers with a switched-capacitor building block. Using two external capacitors, the switched-capacitor network can be configured as a voltage inverter generating a negative supply voltage capable of sourcing up to 100 mA. This supply functions not only as the amplifier's negative rail but is also available to drive external circuitry. In this configuration, the amplifier common-mode input voltage range extends from the positive rail to below ground, thus providing true rail-to-rail inputs from a single supply. Furthermore, the outputs can swing to and below ground while sinking over 25 mA. This feature was previously unavailable in operational amplifier circuits. The TLE2682 operational amplifier section has output stages that can drive 20-mA loads to 2.3 V with a 5-V rail. With a 2-mA load, the output swing extends to 3.9 V.

This amplifier design features a 25-V/μs minimum slew rate, which results in a high-power bandwidth. Settling time to 0.1% of a 10-V step (1-kΩ/100-pF load) is approximately 400 ns. Gain-bandwidth product is typically 10 MHz with an 8-MHz minimum. The TLE2682 offers significant speed and noise advantages at a low 1.5-mA typical supply current per channel.

The TLE2682 features a shutdown pin (FB/SD), which can be used to disable the switched-capacitor section. When disabled, the switched-capacitor voltage converter block draws less then 150 μA from the power supply, V_{IN}.

The switched-capacitor voltage converter block also provides an on-board regulator; with the addition of an external divider, a well-regulated output voltage is easily obtained. The internal oscillator runs at a nominal frequency of 25 kHz. This can be synchronized to an external clock signal or can be varied using an external capacitor. A 2.5-V reference is brought out to V_{REF} for use with the on-board regulator or external circuitry. Additional filtering can be added to minimize switching noise.

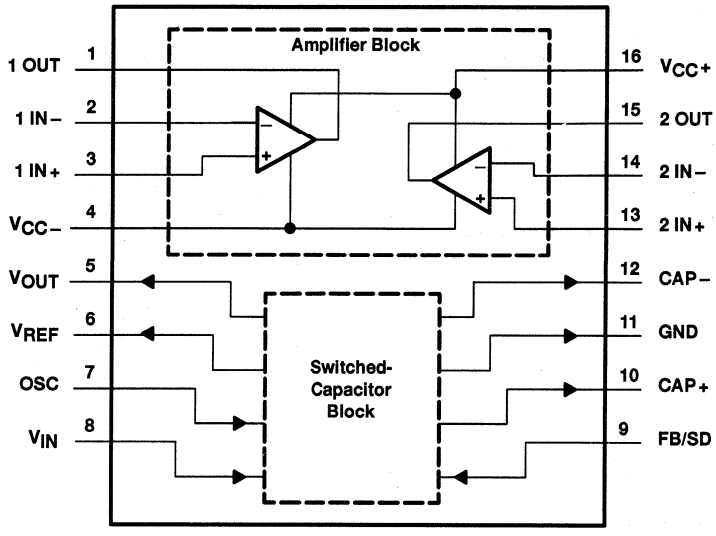
The TLE2682 is characterized for operation over the industrial temperature range of −40°C to 85°C. This device is available in a 16-pin wide-body surface-mount package.

AVAILABLE OPTION

T_A	PACKAGE
	SMALL OUTLINE (DW)
−40°C to 85°C	TLE2682IDW

The DW package is available taped and reeled. Add the suffix R to the device type, (i.e., TLE2682IDWR).

functional block diagram



ACTUAL DEVICE
COMPONENT COUNT

AMPLIFIER BLOCK		SWITCHED-CAPACITOR BLOCK	
Transistors	57	Transistors	71
Resistors	37	Resistors	44
Diodes	5	Diodes	2
Capacitors	11	Capacitors	5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{IN} (see Note 1) ..... 16 V
Supply voltage, V_{CC+} (see Note 2) ..... 16 V
Supply voltage, V_{CC-} (see Note 2) ..... −16 V
Differential input voltage, V_{ID} (see Note 3) ..... 32 V
Input voltage, V_I (any input of amplifier) (see Note 2) ..... $V_{CC\pm}$
Input voltage range, V_I (FB/SD) (see Note 1) ..... 0 V to V_{IN}
Input voltage range, V_I (OSC) (see Note 1) ..... 0 V to V_{REF}
Input current, I_I (each input of amplifier) ..... ± 1 mA
Output current, I_O (each output of amplifier) ..... ± 80 mA
Total current into V_{CC+} ..... 160 mA
Total current out of V_{CC-} ..... 160 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 4) (each amplifier) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Junction temperature (see Note 5) ..... 150°C
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the switched-capacitor block GND pin.
2. Voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
3. Differential voltages are at IN+ with respect to IN−.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
5. The devices are functional up to the absolute maximum junction temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	533 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC+}/V_{IN}		3.5	15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	−1	5	V
	$V_{CC\pm}$ = ±15 V	−11	15	
Output current at V_{OUT}, I_O		0	100	mA
Operating free-air temperature, T_A		−40	85	°C

OPERATIONAL AMPLIFIER SECTION

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.9	7.5	mV
				Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		5	100	pA
				Full range			950	
I_{IB}	Input bias current			25°C		15	175	pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	5 to −1	5 to −1.9		V
				Full range	5 to −0.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	3.8	4.1		V
				Full range	3.7			
		I_O = −2 mA		25°C	3.5	3.9		
				Full range	3.4			
		I_O = −20 mA		25°C	1.5	2.3		
				Full range	1.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−3.8	−4.2		V
				Full range	−3.7			
		I_O = 2 mA		25°C	−3.5	−4.1		
				Full range	−3.4			
		I_O = 20 mA		25°C	−1.5	−2.4		
				Full range	−1.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±2.3 V	R_L = 600 Ω	25°C	75	91		dB
				Full range	74			
			R_L = 2 kΩ	25°C	85	100		
				Full range	84			
			R_L = 10 kΩ	25°C	90	106		
				Full range	89			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		11		pF
			Differential	25°C		2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	70	89		dB
				Full range	68			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		dB
				Full range	80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	2.9	3.6	mA
				Full range			3.6	
a_x	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C		−35		mA
			V_{ID} = −1 V			45		

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_{O(PP)}$ = ±2.3 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C		35		V/μs
				Full range	20			
SR−	Negative slew rate			25°C		38		V/μs
				Full range	20			
	Settling time	A_{VD} = −1, 2-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.25		μs
			To 1 mV			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28		nV/√Hz
			f = 10 kHz			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6		μV
			f = 0.1 Hz to 10 Hz			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 5 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.013%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		9.4		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C		2.8		MHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		56°		

† Full range is 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		1.1	7.5	mV
				Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2.4	25	μV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, See Figure 4		25°C		6	100	pA
				Full range			950	
I_{IB}	Input bias current			25°C		20	175	pA
				Full range			2.5	nA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	15 to −11	15 to −11.9		V
				Full range	15 to −10.8			
V_{OM+}	Maximum positive peak output voltage swing	I_O = −200 μA		25°C	13.8	14.1		V
				Full range	13.7			
		I_O = −2 mA		25°C	13.5	13.9		
				Full range	13.4			
		I_O = −20 mA		25°C	11.5	12.3		
				Full range	11.5			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 200 μA		25°C	−13.8	−14.2		V
				Full range	−13.7			
		I_O = 2 mA		25°C	−13.5	−14		
				Full range	−13.4			
		I_O = 20 mA		25°C	−11.5	−12.4		
				Full range	−11.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V	R_L = 600 Ω	25°C	75	96		dB
				Full range	74			
			R_L = 2 kΩ	25°C	90	109		
				Full range	89			
			R_L = 10 kΩ	25°C	90	118		
				Full range	89			
r_i	Input resistance	V_{IC} = 0		25°C		10^{12}		Ω
c_i	Input capacitance	V_{IC} = 0, See Figure 5	Common mode	25°C		7.5		pF
			Differential	25°C		2.5		
z_o	Open-loop output impedance	f = 1 MHz		25°C		80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω		25°C	80	98		dB
				Full range	79			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	82	99		dB
				Full range	80			
I_{CC}	Supply current (both channels)	V_O = 0, No load		25°C	2.7	3.1	3.6	mA
				Full range			3.6	
a_X	Crosstalk attenuation	V_{IC} = 0, R_L = 2 kΩ		25°C		120		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−30	−45		mA
			V_{ID} = −1 V		30	48		

† Full range is −40°C to 85°C.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_{O(PP)}$ = ±10 V, A_{VD} = −1, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	25°C	25	40		V/μs
				Full range	20			
SR−	Negative slew rate			25°C	25	45		V/μs
				Full range	20			
	Settling time	A_{VD} = −1, 10-V step, R_L = 1 kΩ, C_L = 100 pF	To 10 mV	25°C		0.4		μs
			To 1 mV			1.5		
V_n	Equivalent input noise voltage	R_S = 20 Ω, See Figure 3	f = 10 Hz	25°C		28		nV/√Hz
			f = 10 kHz			11.6		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		6		μV
			f = 0.1 Hz to 10 Hz			0.6		
I_n	Equivalent input noise current	V_{IC} = 0,	f = 10 kHz	25°C		2.8		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, f = 1 kHz, R_S = 25 Ω	A_{VD} = 10, R_L = 2 kΩ,	25°C		0.008%		
B_1	Unity-gain bandwidth	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C	8	10		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ,	A_{VD} = −1, C_L = 25 pF	25°C	478	637		kHz
ϕ_m	Phase margin at unity gain	V_I = 10 mV, C_L = 25 pF,	R_L = 2 kΩ, See Figure 2	25°C		57°		

† Full range is −40°C to 85°C.

SWITCHED-CAPACITOR SECTION

electrical characteristics over recommended supply voltage range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
Regulated output voltage, V_{OUT}	V_{CC} = 5 V, T_J = 25°C, $R_L(V_{OUT})$ = 500 Ω, See Note 6		25°C	−3.75	−4	−4.25	V
	V_{CC} = 7 V, T_J = 25°C, $R_L(V_{OUT})$ = 500 Ω, See Note 7		25°C	−4.7	−5	−5.2	
Input regulation	V_{CC} = 5 V to 15 V, $R_L(V_{OUT})$ = 500 Ω, See Note 6		Full range		7	27	mV
	V_{CC} = 7 V to 12 V, $R_L(V_{OUT})$ = 500 Ω, See Note 7		Full range		5	25	
Output regulation	V_{CC} = 5 V, $R_L(V_{OUT})$ = 100 Ω to 500 Ω		Full range		20	140	mV
	V_{CC} = 7 V, $R_L(V_{OUT})$ = 100 Ω to 500 Ω		Full range		20	70	
Voltage loss, $V_{CC} - \lvert V_{OUT} \rvert$ (see Note 8)	V_{CC} = 7 V, $C_{IN} = C_{OUT}$ = 100-μF tantalum	I_O = 10 mA	Full range		0.35	0.55	V
		I_O = 100 mA	Full range		1.1	1.8	
Output resistance	ΔI_O = 10 mA to 100 mA, See Note 9		Full range		10	15	Ω
Oscillator frequency			Full range	15	25	35	kHz
Reference voltage, V_{ref}	V_{CC} = 5 V, I_{ref} = 50 μA		25°C	2.35	2.5	2.65	V
			Full range	2.25		2.75	
	V_{CC} = 7 V, I_{ref} = 60 μA		25°C	2.35	2.5	2.65	
			Full range	2.25		2.75	
Maximum switch current			25°C		300		mA

† Data applies for the switched-capacitor block only. Amplifier block is not connected.
‡ Full range is −40°C to 85°C.

NOTES: 6. Regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator (see Figure 105) with R1 = 23.7 kΩ, R2 = 102.2 kΩ, C_{IN} = 10 μF (tantalum), C_{OUT} = 100 μF (tantalum), and C1 = 0.002 μF.
7. Regulation specifications are for the switched-capacitor section connected as a positive to negative converter/regulator (see Figure 105) with R1 = 20 kΩ, R2 = 102.5 kΩ, C_{IN} = 10 μF (tantalum), C_{OUT} = 100 μF (tantalum) and C1 = 0.002 μF.
8. For voltage-loss tests, the switched-capacitor section is connected as a voltage inverter, with V_{REF}, OSC, and FB/SD (pins 6, 7, and 9) unconnected. The voltage losses may be higher in other configurations.
9. Output resistance is defined as the slope of the curve (ΔV_O vs ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve are higher at currents less than 10 mA due to the characteristics of the switch transistors.

AMPLIFIER AND SWITCHED-CAPACITOR SECTIONS CONNECTED

electrical characteristics, $V_{IN} = V_{CC+}$ = 5 V, T_A = 25°C (see Figure 6)

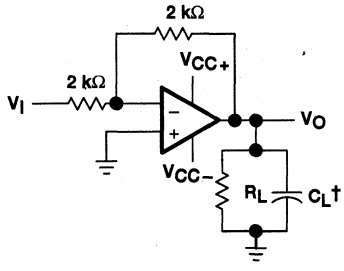
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ			4.1		V
		R_L = 600 Ω			3.6		
		R_L = 100 Ω			2.3		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ			−3.9		V
		R_L = 600 Ω			−3.3		
		R_L = 100 Ω			−1.9		
	Voltage loss, $V_{IN} - \lvert V_{OUT} \rvert$ (see Note 8)	V_{ID} = −100 mV, $C_{IN} = C_{OUT}$ = 100-μF tantalum	R_L = 10 kΩ		0.55		V
			R_L = 600 Ω		0.65		
			R_L = 100 Ω		0.9		

NOTE 8: For voltage-loss tests, the switched-capacitor section is connected as a voltage inverter, with V_{REF}, OSC, and FB/SD (pins 6, 7, and 9) unconnected. The voltage losses may be higher in other configurations.

supply current (no load), T_A = 25°C

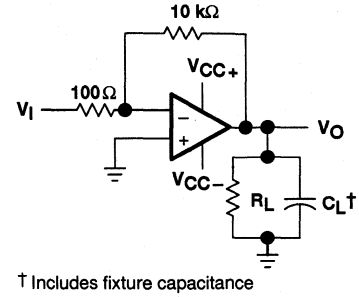
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	V_{CC+} = 5 V, V_{IN} = 5 V, $V_{FB/SD}$ = 2.5 V, V_O = 0		8.9		mA
Supply current in shutdown	V_{CC+} = 5 V, V_{IN} = 5 V, $V_{FB/SD}$ = 0 V		2.5		mA

PARAMETER MEASUREMENT INFORMATION



† Includes fixture capacitance

Figure 1. Slew-Rate Test Circuit



† Includes fixture capacitance

Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

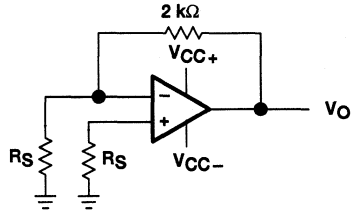


Figure 3. Noise-Voltage Test Circuit

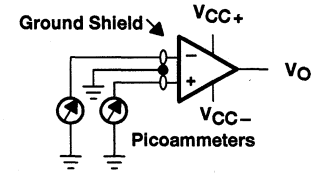


Figure 4. Input-Bias and Offset-Current Test Circuit

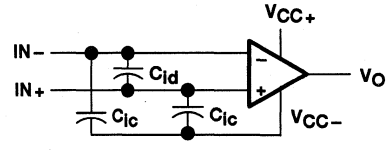


Figure 5. Internal Input Capacitance

PARAMETER MEASUREMENT INFORMATION

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias-current level typical of the TLE2682, accurate measurement of the bias currents becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket, and a second test is performed that measures both the socket leakage and the device input bias current (see Figure 6). The two measurements are then subtracted algebraically to determine the bias current of the device.

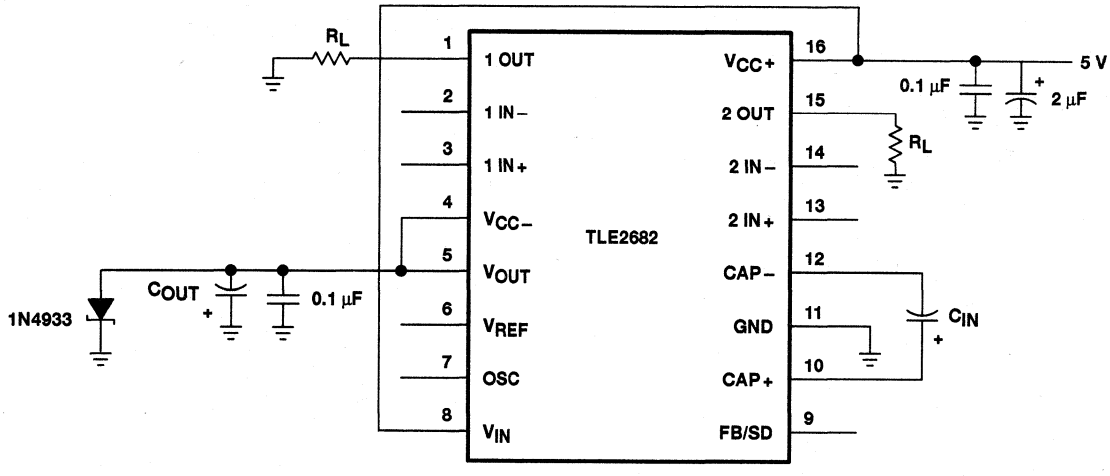


Figure 6. Bias-Current Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs for Operational Amplifier Section

			FIGURE
V_{IO}	Input offset voltage	Distribution	7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8
I_{IO}	Input offset current	vs Free-air temperature	9, 10
I_{IB}	Input bias current	vs Free-air temperature vs Supply voltage	9, 10 11
V_{IC}	Common-mode input voltage range	vs Free-air temperature	12
V_{ID}	Differential input voltage	vs Output voltage	13, 14
V_{OM+}	Maximum positive peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	15 17, 18 19
V_{OM-}	Maximum negative peak output voltage	vs Output current vs Free-air temperature vs Supply voltage	16 17, 18 19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
V_O	Output voltage	vs Settling time	21
A_{VD}	Large-signal differential voltage amplification	vs Load resistance vs Free-air temperature vs Frequency	22 23, 24 25, 26
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	27 28
k_{SVR}	Supply voltage rejection ratio	vs Frequency vs Free-air temperature	29 30
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature vs Differential input voltage	31 32 33, 34
I_{OS}	Short-circuit output current	vs Supply voltage vs Time vs Free-air temperature	35 36 37
SR	Slew rate	vs Free-air temperature vs Load resistance vs Differential input voltage	38, 39 40 41
V_n	Equivalent input noise voltage	vs Frequency	42
V_n	Input-referred noise voltage	vs Noise bandwidth Over a 10-second time interval	43 44
	Third-octave spectral noise density	vs Frequency	45
THD + N	Total harmonic distortion plus noise	vs Frequency	46, 47
B_1	Unity-gain bandwidth	vs Load capacitance	48
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	49 50
A_m	Gain margin	vs Load capacitance	51
ϕ_m	Phase margin	vs Free-air temperature vs Supply voltage vs Load capacitance	52 53 54
	Phase shift	vs Frequency	25, 26

TYPICAL CHARACTERISTICS

Table of Graphs for Operational Amplifier Section (Continued)

			FIGURE
	Large-signal pulse response, noninverting	vs Time	55
	Small-signal pulse response	vs Time	56
z_o	Output impedance	vs Frequency	57
a_x	Crosstalk attenuation	vs Frequency	58

Table of Graphs for Switched-Capacitor Section

			FIGURE
	Shutdown threshold voltage	vs Free-air temperature	59
I_{CC}	Supply current	vs Input voltage	60
f_{osc}	Oscillator frequency	vs Free-air temperature	61
	Supply current in shutdown	vs Input voltage	62
I_{avg}	Average supply current	vs Output current	63
	Output voltage loss	vs Input capacitance	64
	Output voltage loss	vs Oscillator frequency	65, 66
V_O	Regulated output voltage	vs Free-air temperature	67
ΔV_{REF}	Reference voltage change	vs Free-air temperature	68
	Voltage loss	vs Output current	69

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

DISTRIBUTION OF TLE2682 INPUT OFFSET VOLTAGE

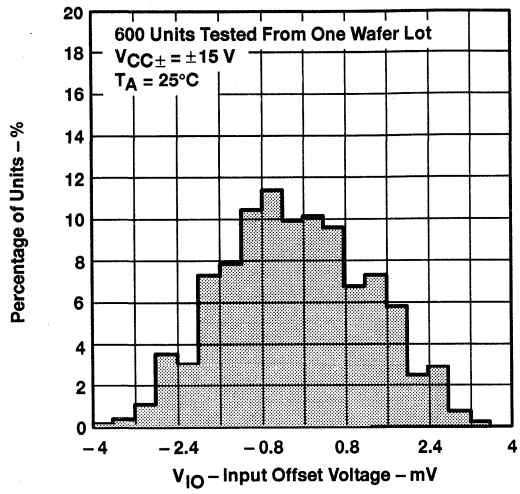


Figure 7

DISTRIBUTION OF TLE2682 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

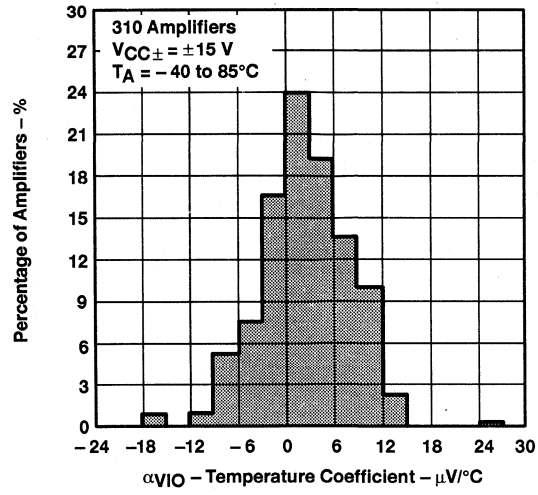


Figure 8

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

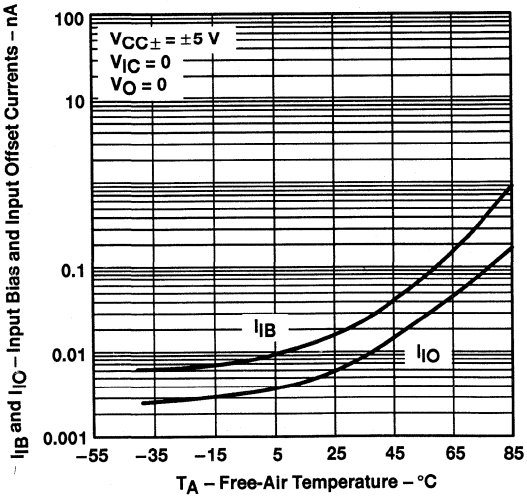


Figure 9

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

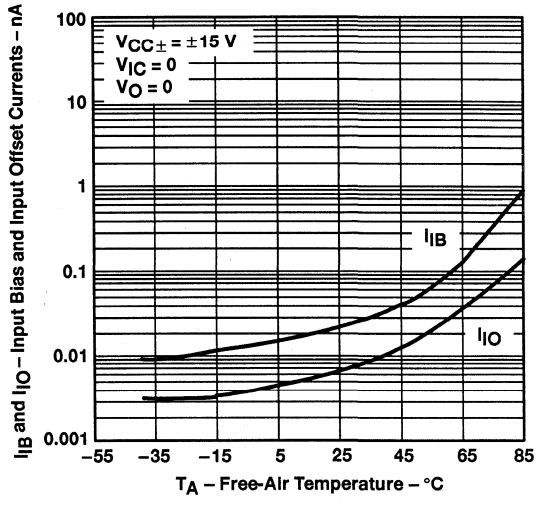


Figure 10

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

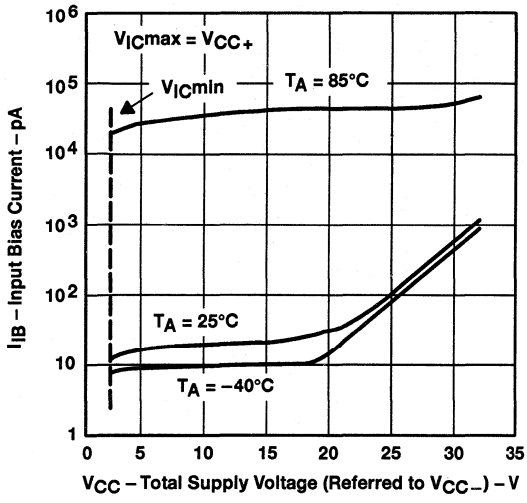


Figure 11

COMMON-MODE INPUT VOLTAGE RANGE
vs
TEMPERATURE

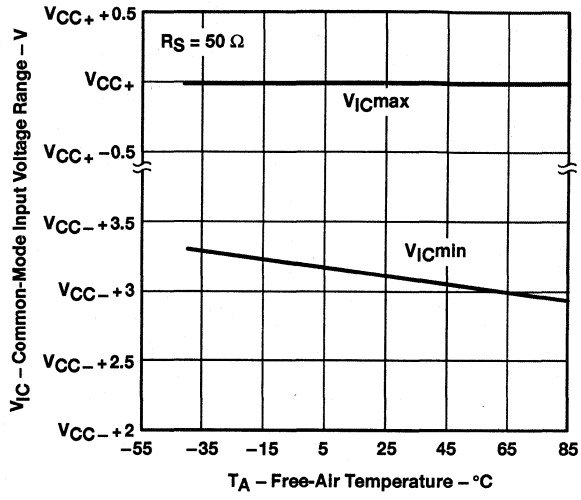


Figure 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

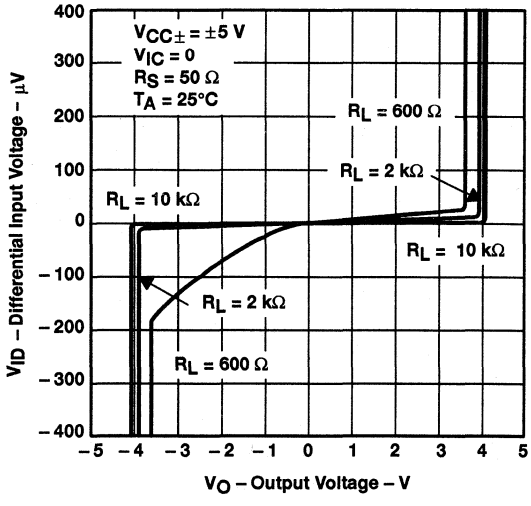


Figure 13

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

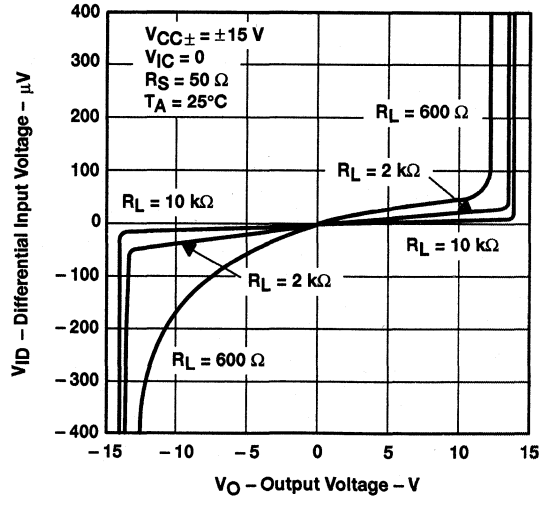


Figure 14

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

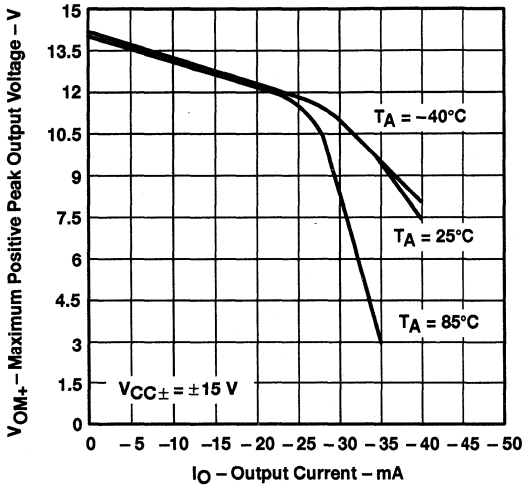


Figure 15

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

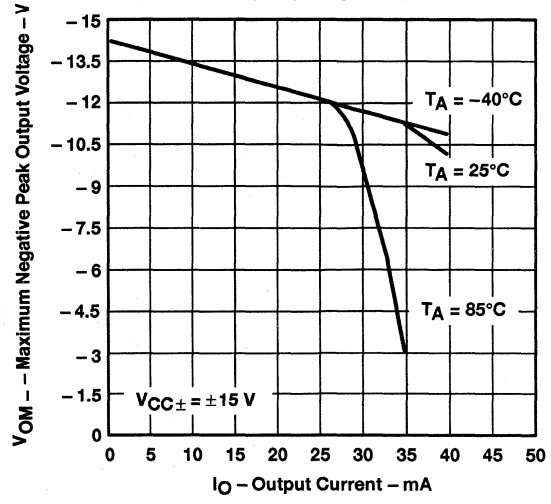


Figure 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

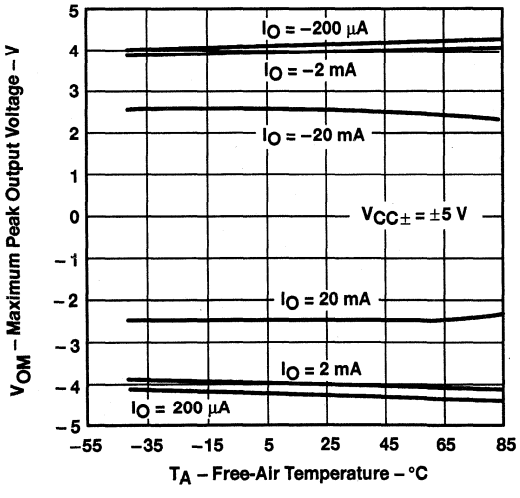


Figure 17

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

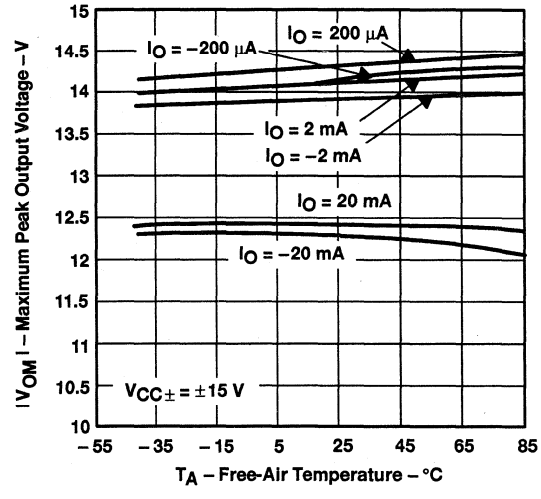


Figure 18

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

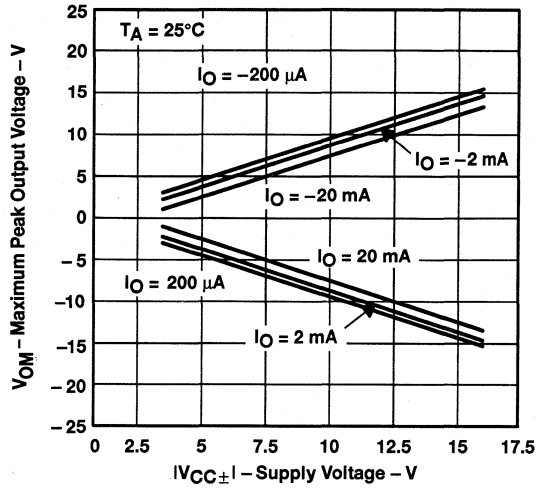


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

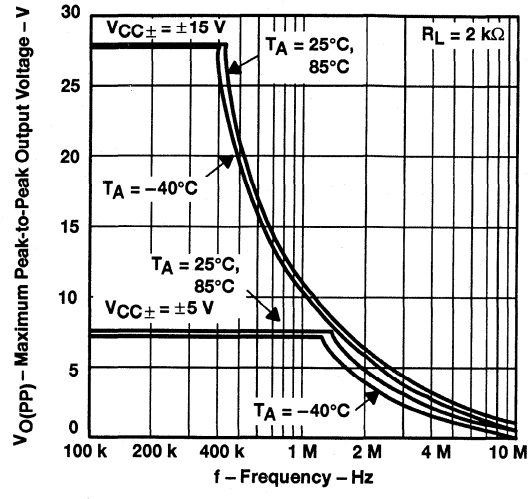


Figure 20

OUTPUT VOLTAGE
vs
SETTLING TIME

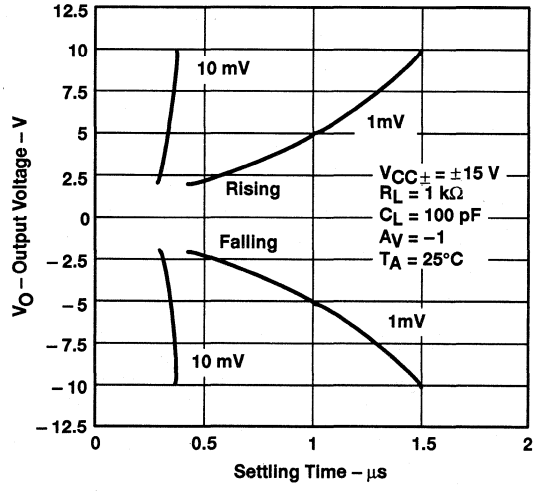


Figure 21

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

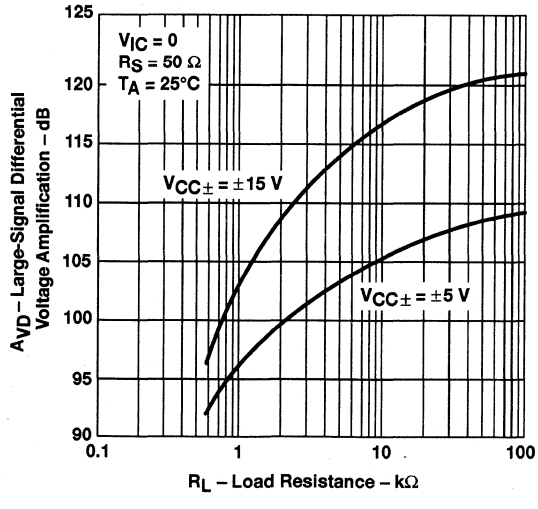


Figure 22

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying $V_{CC–}$ supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

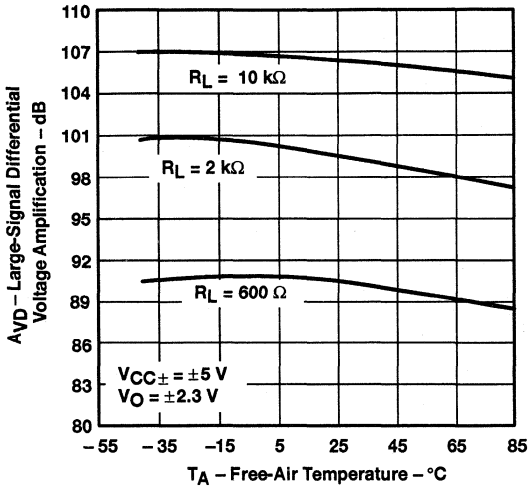


Figure 23

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

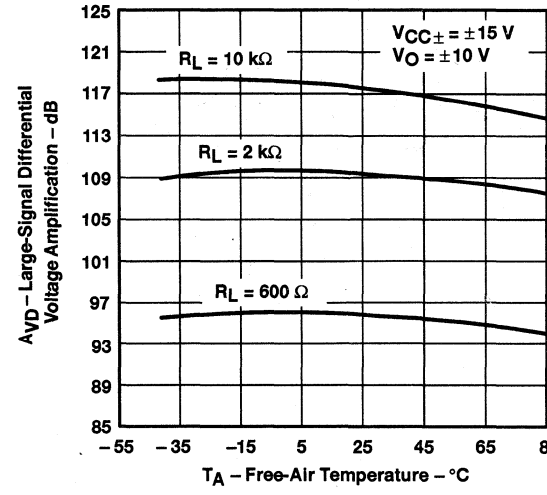


Figure 24

SMALL-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

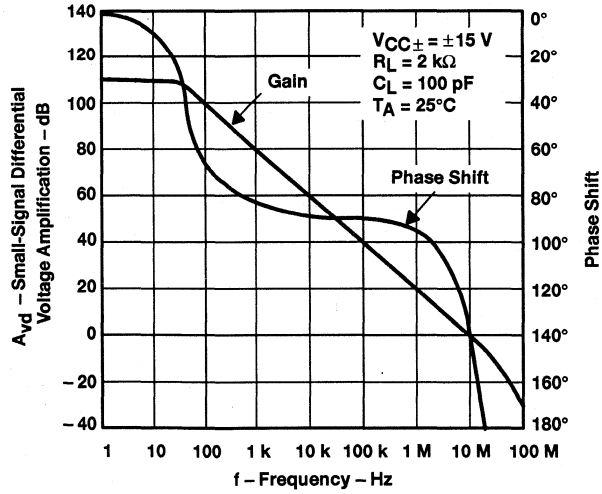


Figure 25

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS† OPERATIONAL AMPLIFIER SECTION

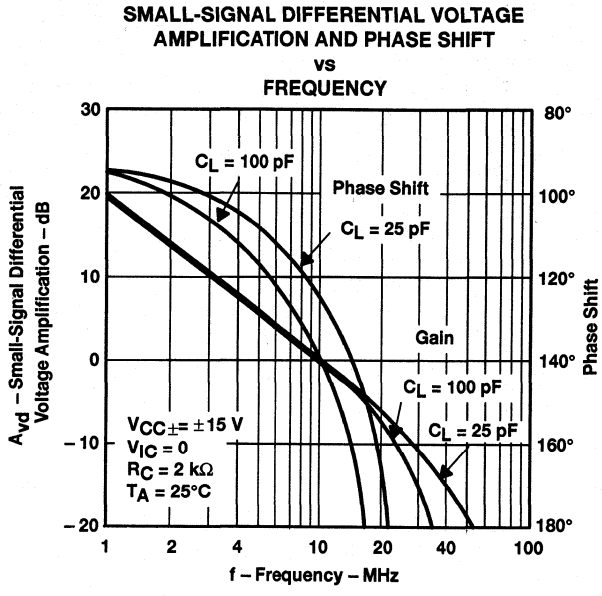


Figure 26

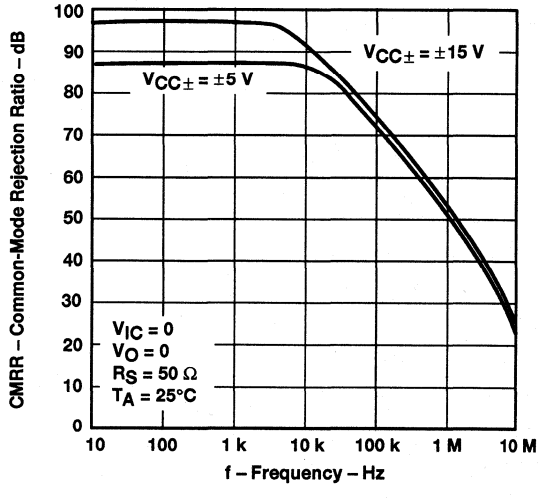


Figure 27

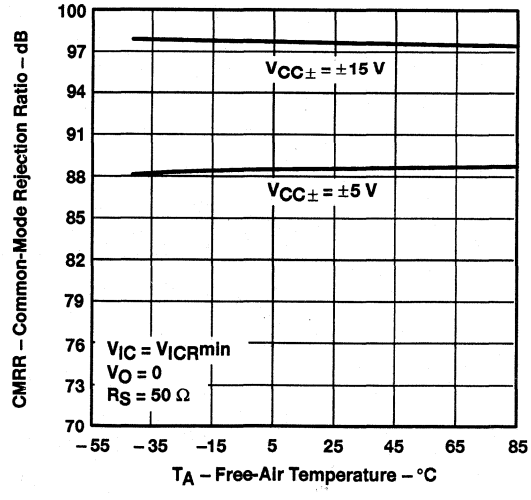


Figure 28

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

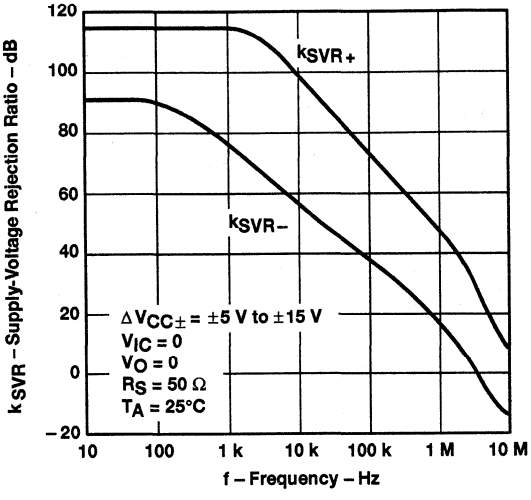


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

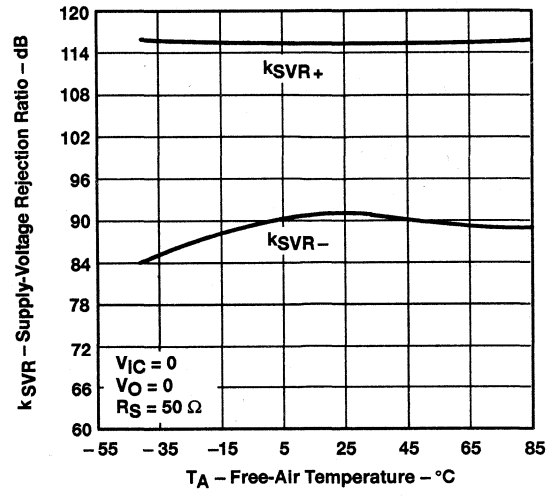


Figure 30

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

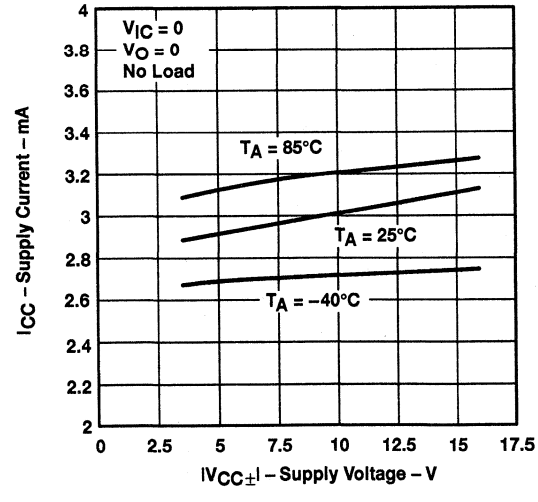


Figure 31

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

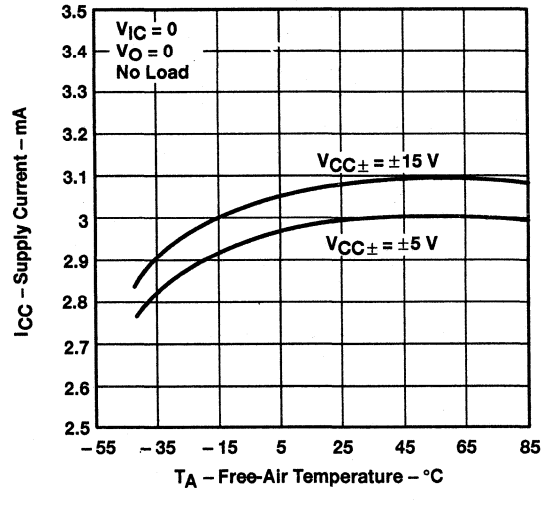


Figure 32

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

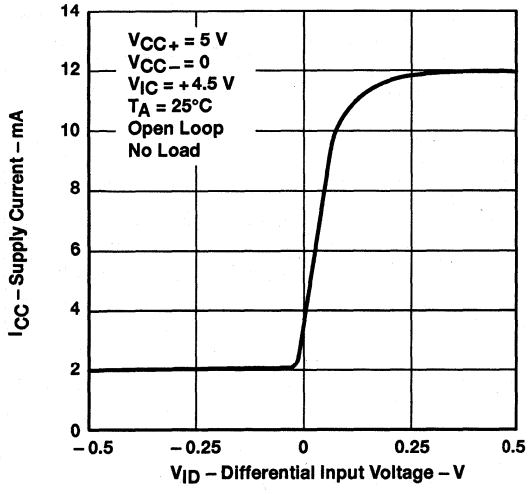


Figure 33

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

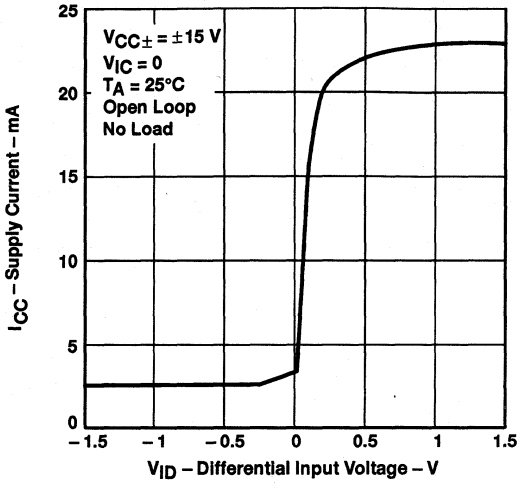


Figure 34

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

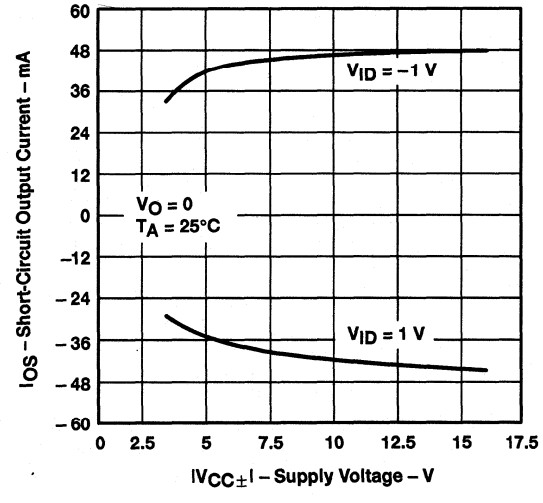


Figure 35

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

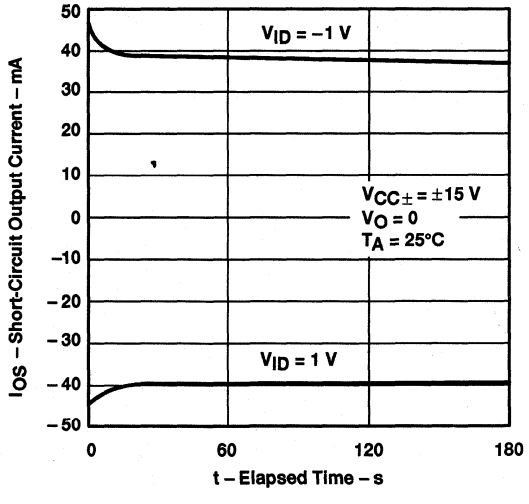


Figure 36

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

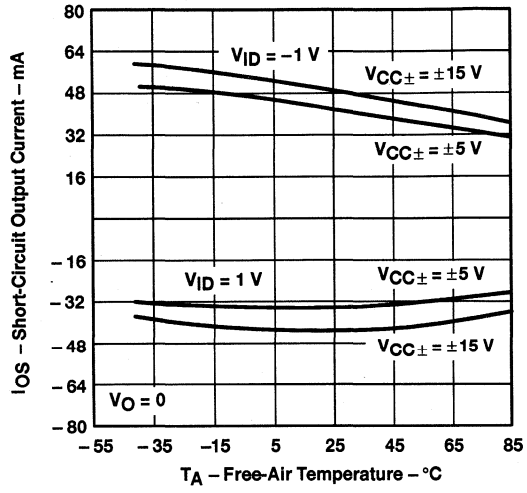


Figure 37

SLEW RATE vs FREE-AIR TEMPERATURE

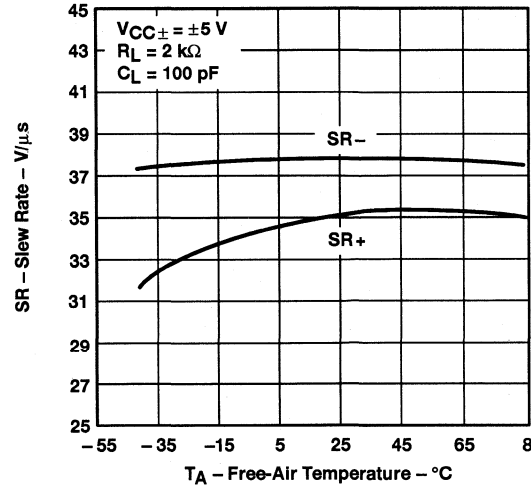


Figure 38

SLEW RATE vs FREE-AIR TEMPERATURE

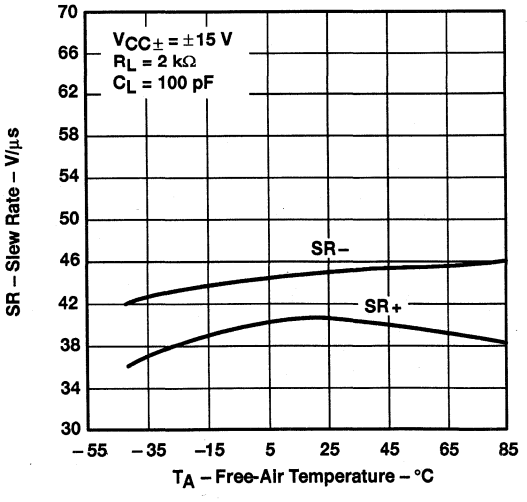


Figure 39

SLEW RATE vs LOAD RESISTANCE

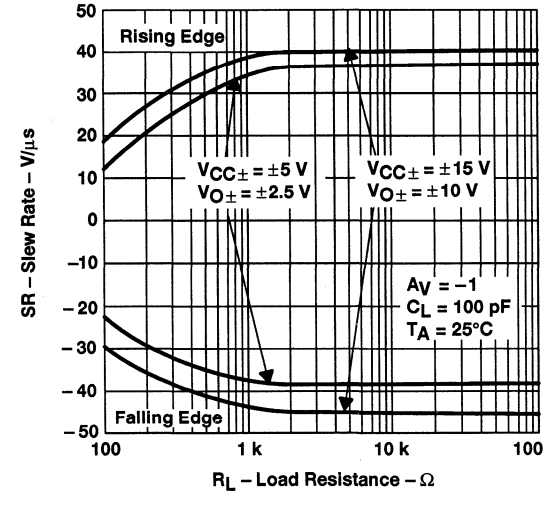


Figure 40

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE

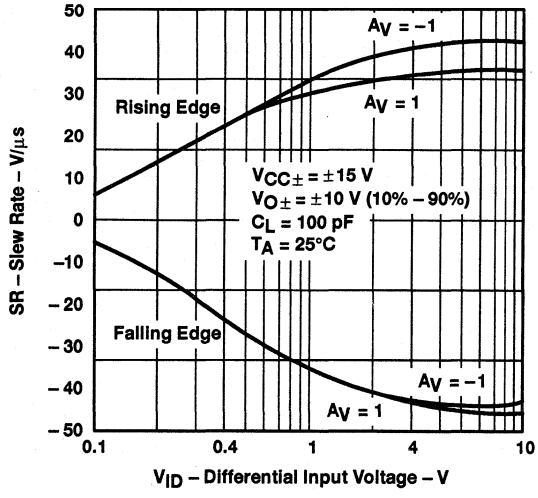


Figure 41

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

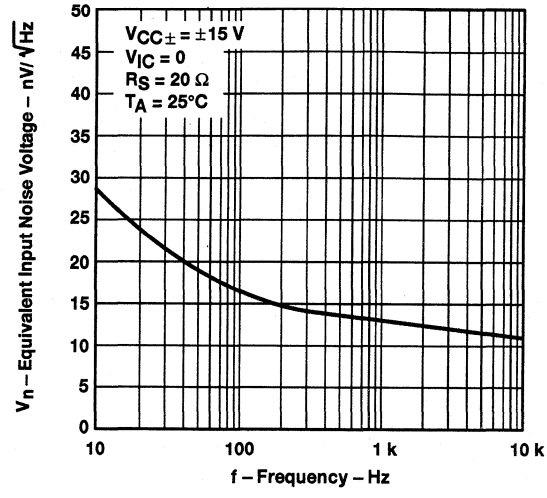


Figure 42

INPUT-REFERRED NOISE VOLTAGE vs NOISE BANDWIDTH

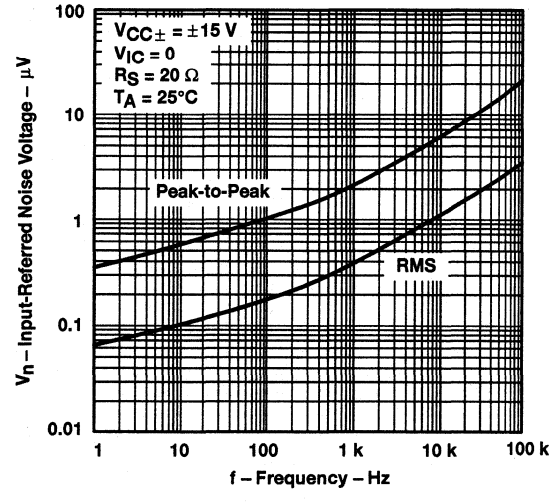


Figure 43

INPUT-REFERRED NOISE VOLTAGE OVER A 10-SECOND TIME INTERVAL

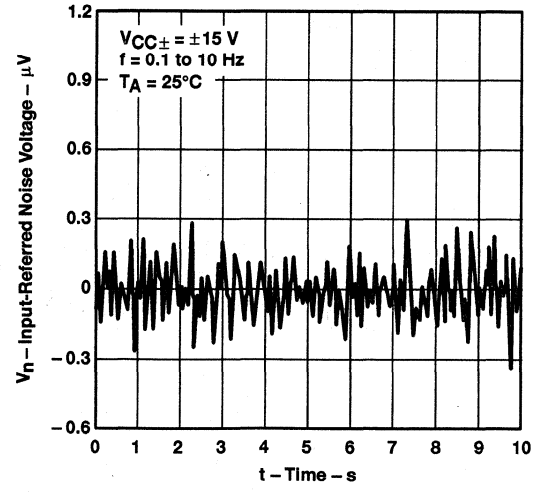


Figure 44

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS† OPERATIONAL AMPLIFIER SECTION

THIRD-OCTAVE SPECTRAL NOISE DENSITY
vs
FREQUENCY

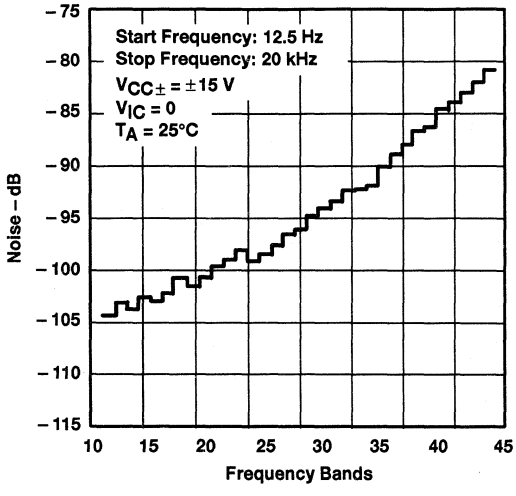


Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

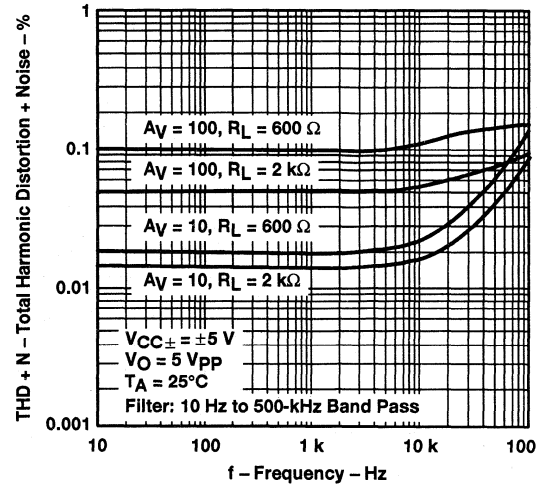


Figure 46

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

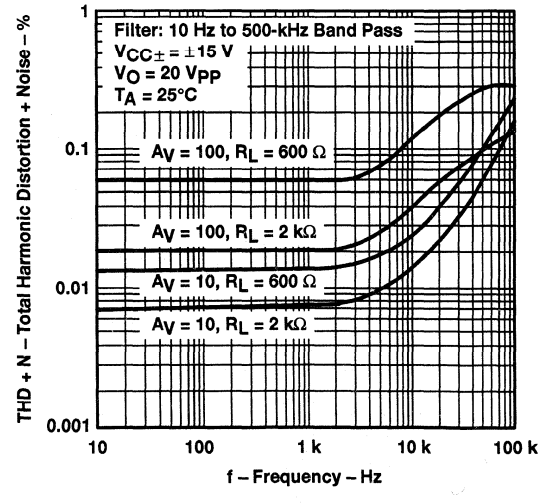


Figure 47

UNITY GAIN BANDWIDTH
vs
LOAD CAPACITANCE

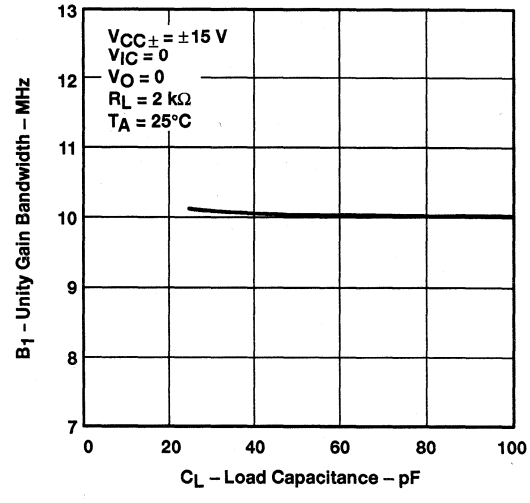


Figure 48

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS† OPERATIONAL AMPLIFIER SECTION

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

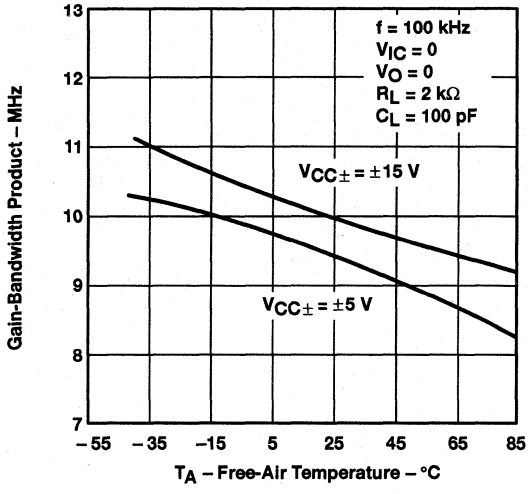


Figure 49

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

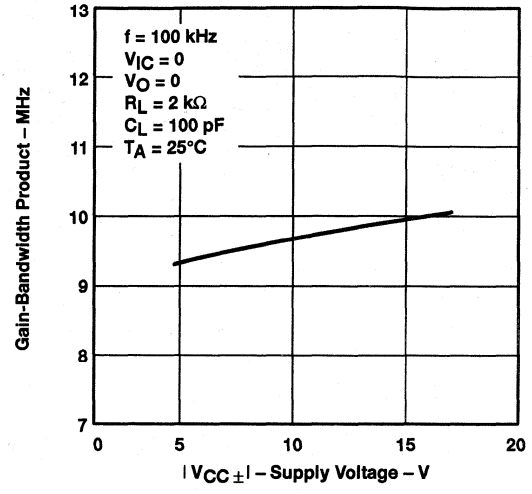


Figure 50

GAIN MARGIN vs LOAD CAPACITANCE

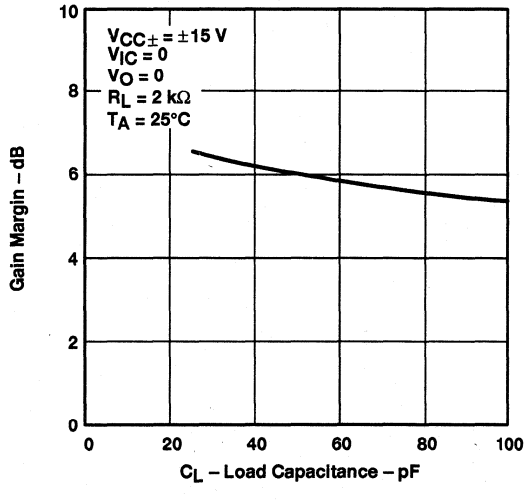


Figure 51

PHASE MARGIN vs TEMPERATURE

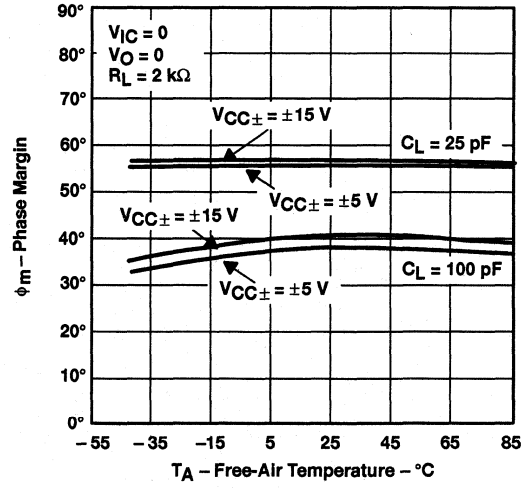


Figure 52

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

PHASE MARGIN vs SUPPLY VOLTAGE

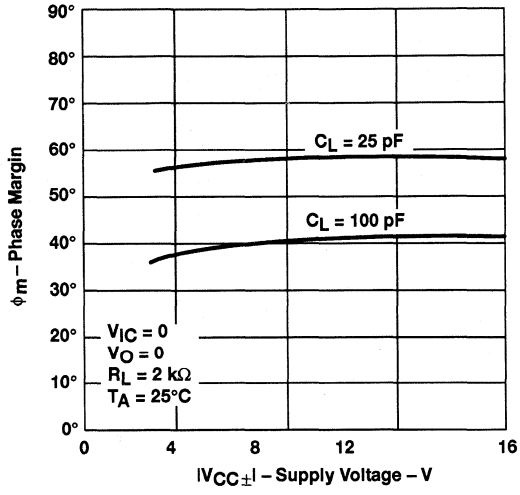


Figure 53

PHASE MARGIN vs LOAD CAPACITANCE

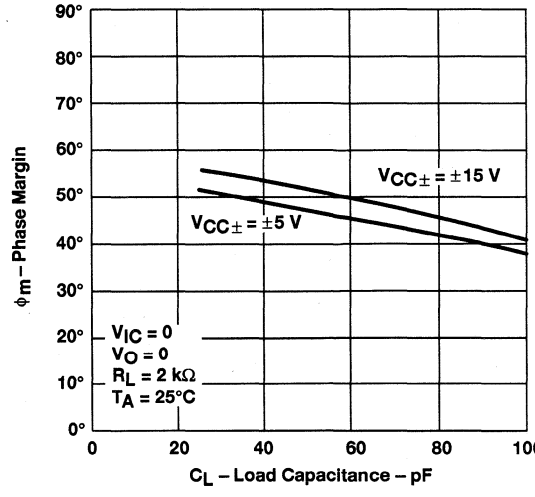


Figure 54

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

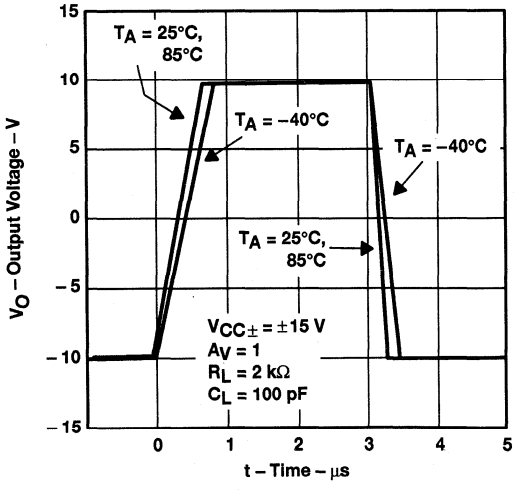


Figure 55

SMALL-SIGNAL PULSE RESPONSE

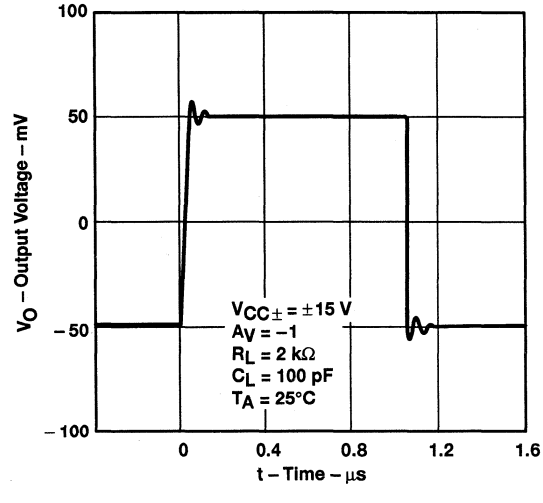


Figure 56

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS†
OPERATIONAL AMPLIFIER SECTION

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

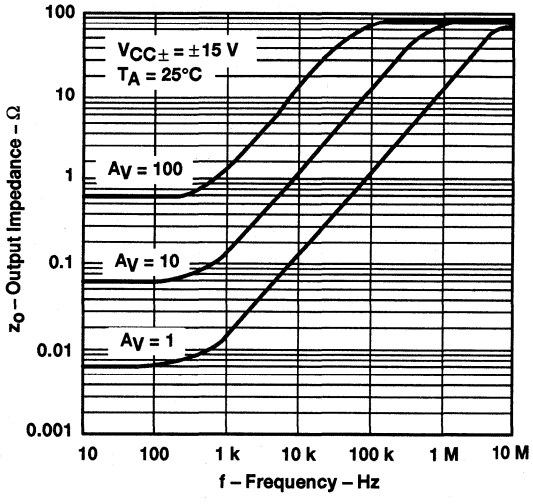


Figure 57

CROSSTALK ATTENUATION vs FREQUENCY

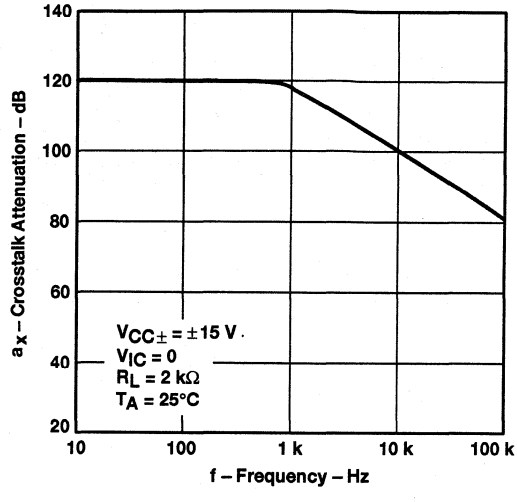


Figure 58

† Data applies to the operational amplifier block only. Switched-capacitor block is not supplying V_{CC-} supply.

TYPICAL CHARACTERISTICS† SWITCHED-CAPACITOR SECTION

SHUTDOWN THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

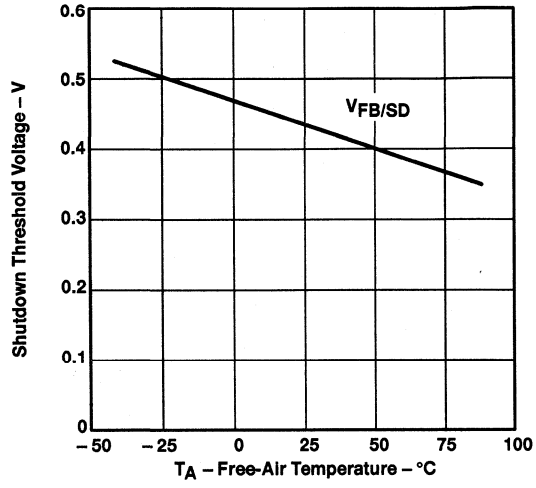


Figure 59

SUPPLY CURRENT
vs
INPUT VOLTAGE

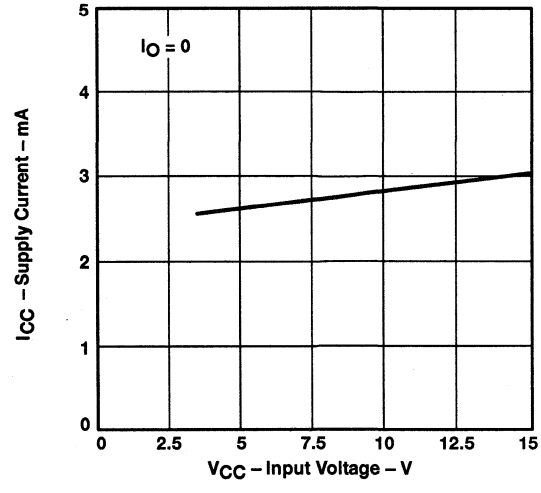


Figure 60

OSCILLATOR FREQUENCY
vs
FREE-AIR TEMPERATURE

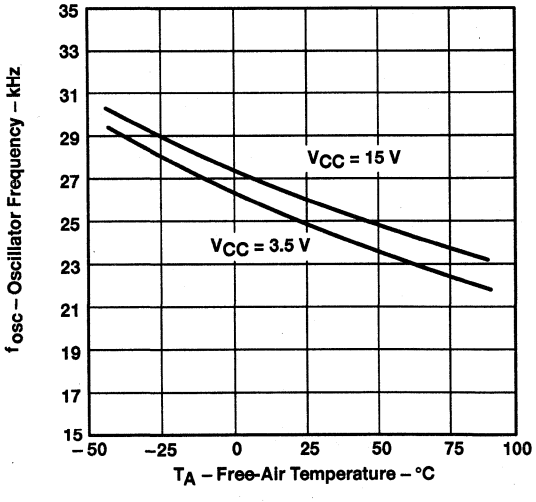


Figure 61

SUPPLY CURRENT IN SHUTDOWN
vs
INPUT VOLTAGE

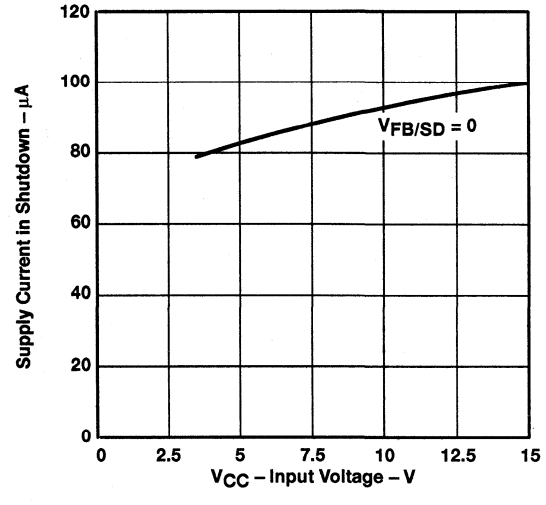


Figure 62

† Data applies to the switched-capacitor block only. Amplifier block is not connected.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

AVERAGE SUPPLY CURRENT
vs
OUTPUT CURRENT

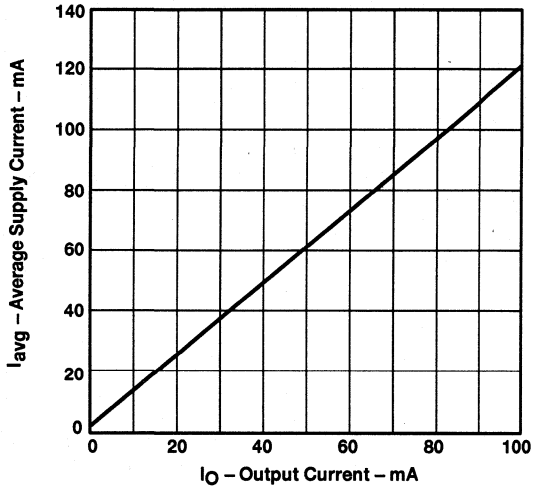


Figure 63

OUTPUT VOLTAGE LOSS
vs
INPUT CAPACITANCE

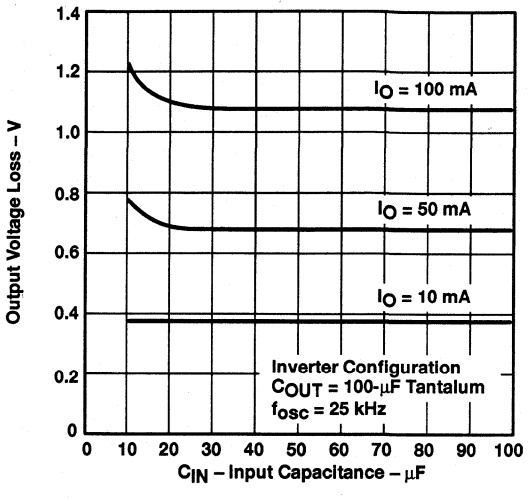


Figure 64

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

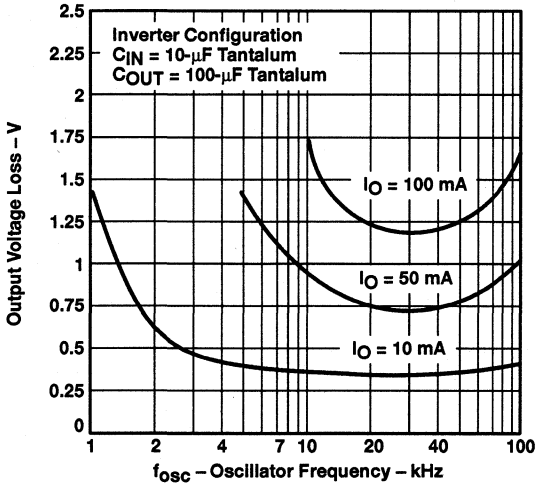


Figure 65

OUTPUT VOLTAGE LOSS
vs
OSCILLATOR FREQUENCY

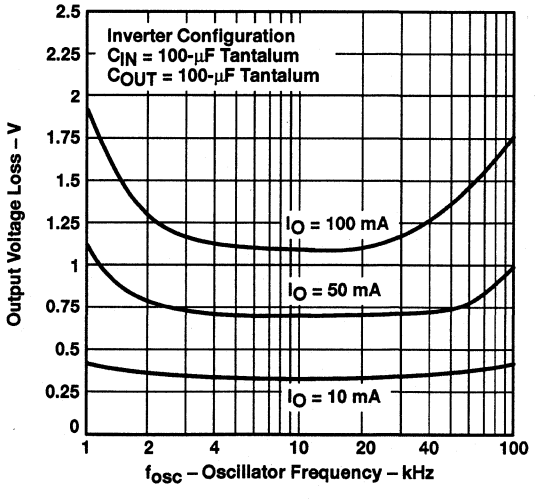


Figure 66

† Data applies to the switched-capacitor block only. Amplifier block is not connected.

TYPICAL CHARACTERISTICS†
SWITCHED-CAPACITOR SECTION

REGULATED OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

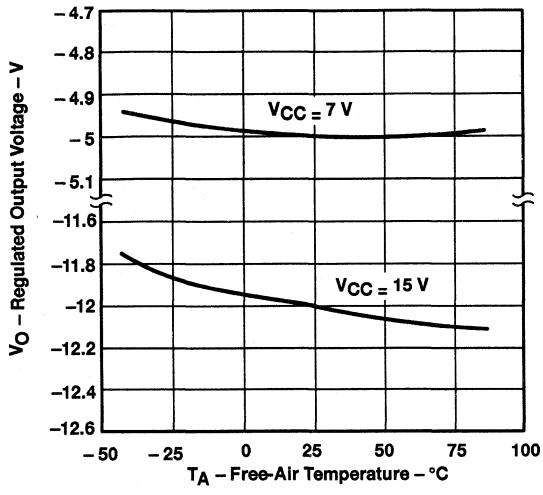


Figure 67

REFERENCE VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

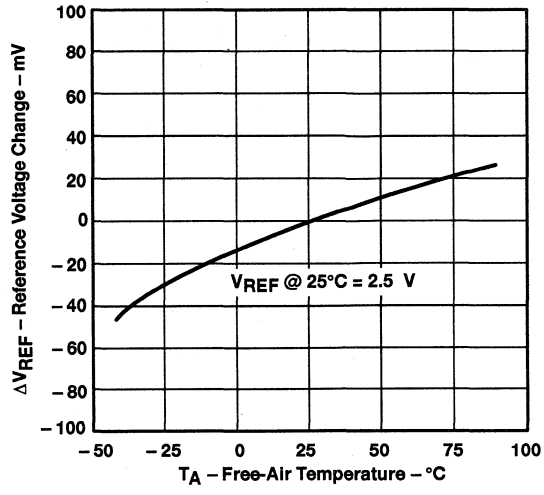


Figure 68

VOLTAGE LOSS
vs
OUTPUT CURRENT

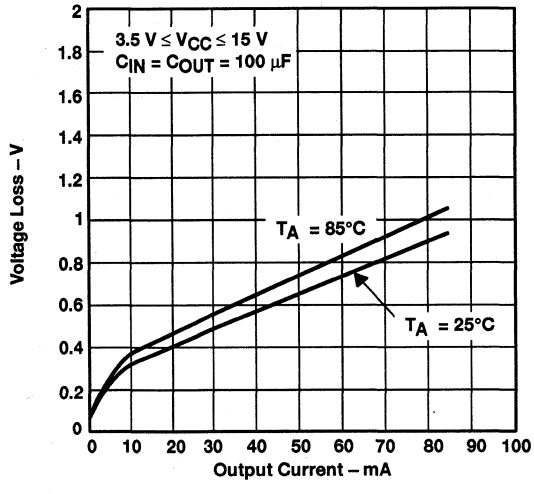


Figure 69

† Data applies to the switched-capacitor block only. Amplifier block is not connected.

APPLICATION INFORMATION

amplifier section

input characteristics

The TLE2682 is specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2682 operational amplifier section is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 70). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded voltage followers to avoid potential oscillation.

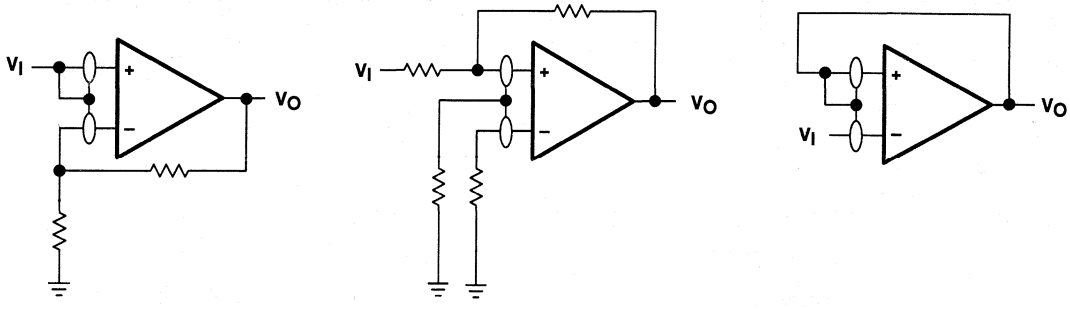
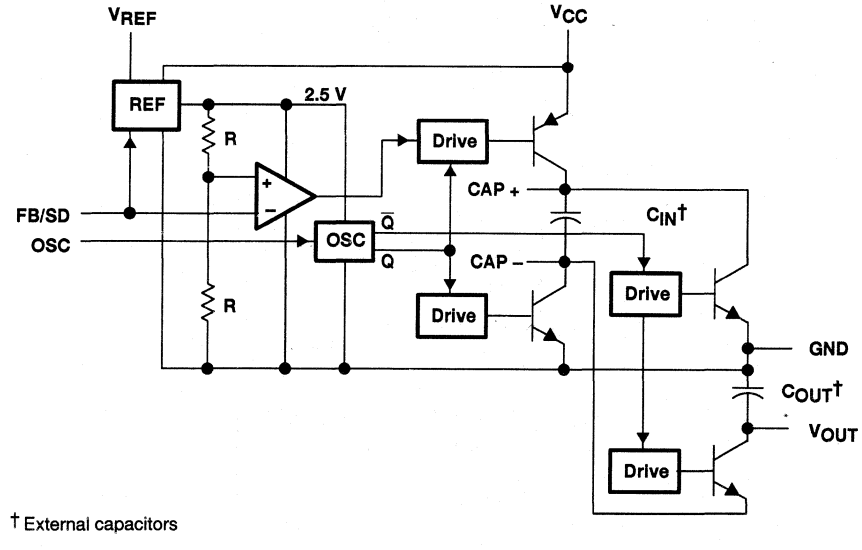


Figure 70. Use of Guard Rings

switched-capacitor section

Figure 71 shows the functional block diagram for the switched-capacitor block only.



† External capacitors

Figure 71. Functional Block Diagram for Switched-Capacitor Block Only

APPLICATION INFORMATION

The TLE2682 high-speed JFET-input amplifiers are ideal for conditioning fast signals from high-impedance sources. When interfacing with ADCs in single-supply 5-V systems, its on board charge pump provides the negative rail necessary for reliable operation of the JFET inputs and delivers a common-mode input voltage range that includes ground and the positive rail. The amplifiers can also drive resistive loads to 0.000 V while sinking 25 mA.

Figure 72 shows the switched-capacitor section configured as a voltage inverter generating approximately –5-V supply voltage from the single 5-V supply available. Three external components are necessary: the storage capacitors, C_{IN} and C_{OUT}, and a fast recovery Schottky diode to clamp V_{OUT} during start-up. The diode is necessary because the amplifiers present a load referenced to the positive rail and tend to pull V_{OUT} above ground, which may prevent the switched-capacitor section from starting (see section on pin functions). The amplifiers use the 5-V supply for V_{CC+} (pin 16) and the derived –5-V supply for V_{CC-} (pin 4). One amplifier is shown driving an ADC; the other is driving a resistive load (see Figure 73).

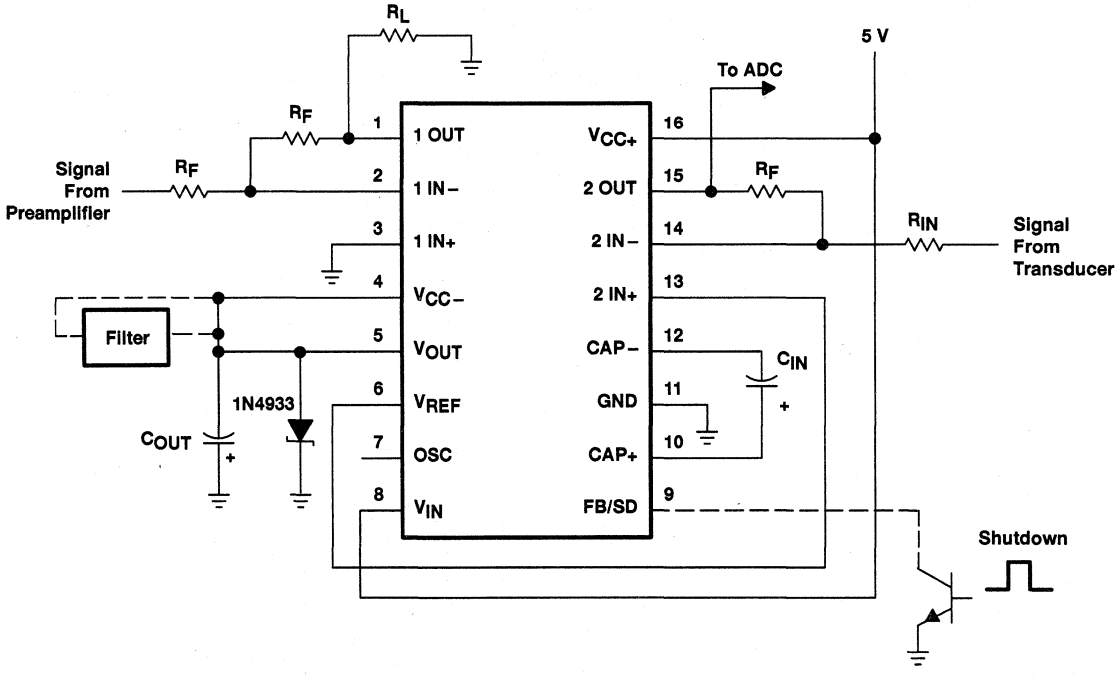


Figure 72. Switched-Capacitor Block Supplying Negative Rail for Amplifiers

APPLICATION INFORMATION

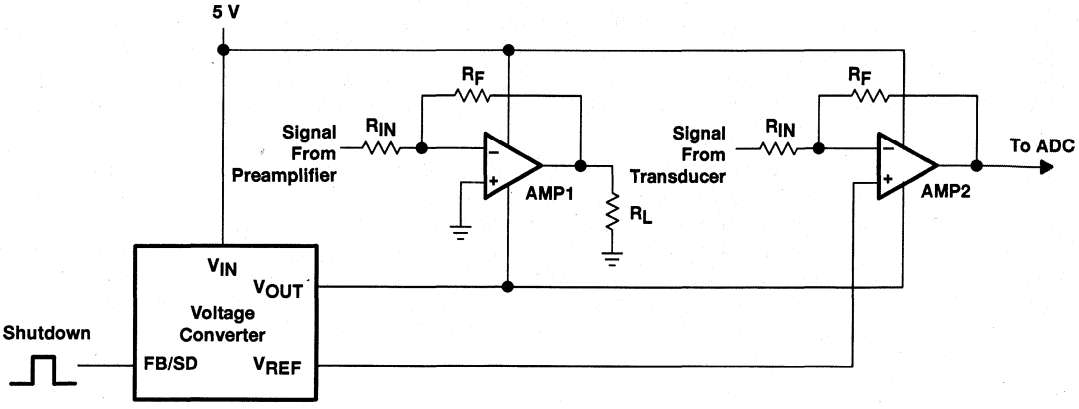


Figure 73. Equivalent Schematic: Amplifier 1 Driving Resistive Load, Amplifier 2 Interfacing to an ADC

Using the switched-capacitor network to generate the negative rail for the amplifiers (or other circuitry) requires special design considerations to minimize the effects of ripple and switching noise. Using larger values for C_{OUT} and selecting low-ESR capacitors reduces the ripple and noise present on V_{OUT}, the – 5-V rail (refer to the capacitor section and the output ripple discussion in the switched-capacitor section). Figure 74 and Figure 75 show the smoothing effect of changing C_{OUT} from 10 µF to 100 µF when V_{OUT} is supplying 1 mA. Figure 76 and Figure 77 demonstrate that at heavier loads the ripple and noise are more pronounced and while increasing the size of C_{OUT} helps, other steps may be necessary.

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

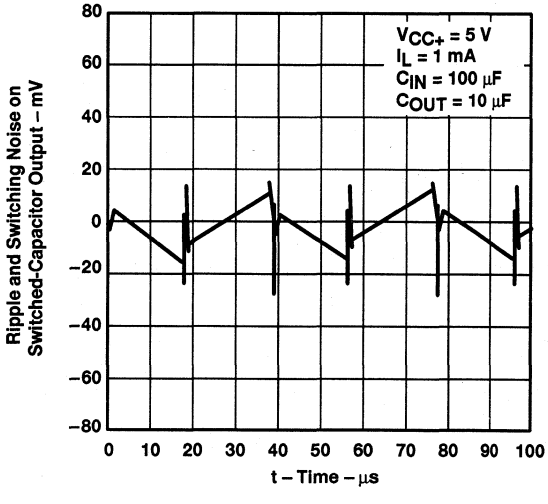


Figure 74

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

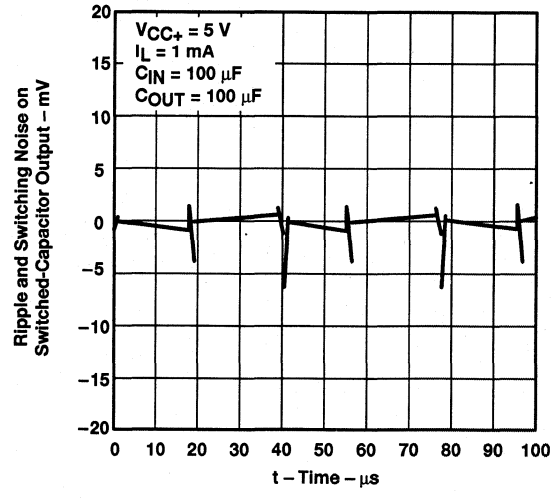


Figure 75

APPLICATION INFORMATION

typical application (continued)

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT VS TIME

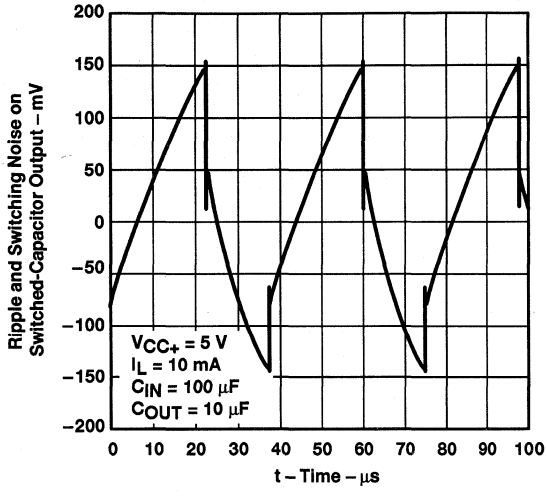


Figure 76

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT VS TIME

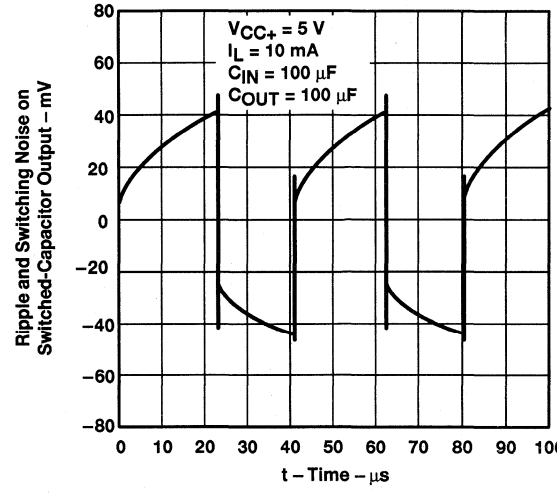


Figure 77

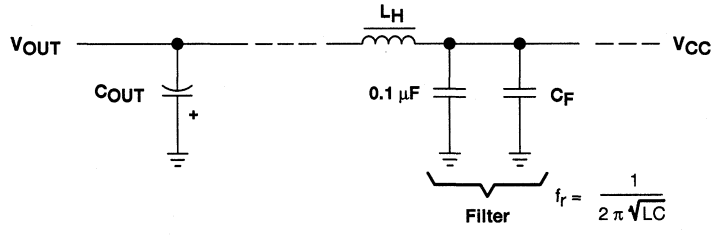


Figure 78. LC Filter Used to Reduce Ripple and Switching Noise, $f_r = 1/2\pi\sqrt{LC}$, A = −40 dB per Decade

A low-pass LC filter can be added to the circuit to further reduce ripple and noise. For example, adding a filter as shown in Figure 78, implemented using a 50-μH inductor and 200-μF capacitor (available in surface mount), achieves the following results (see Figure 79 through Figure 82).

APPLICATION INFORMATION

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

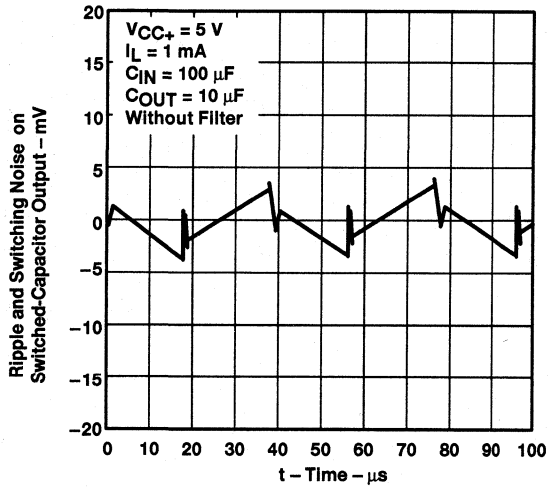


Figure 79

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

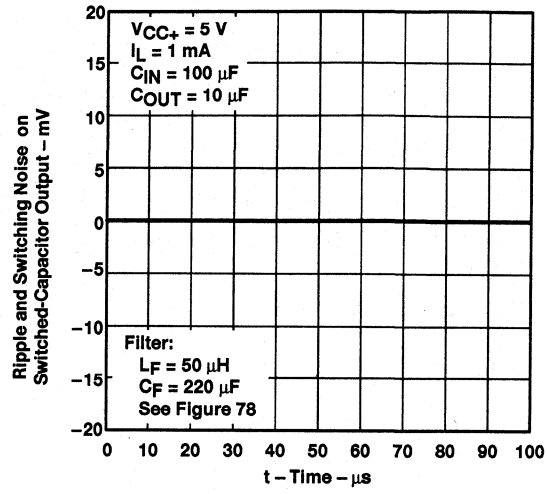


Figure 80

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

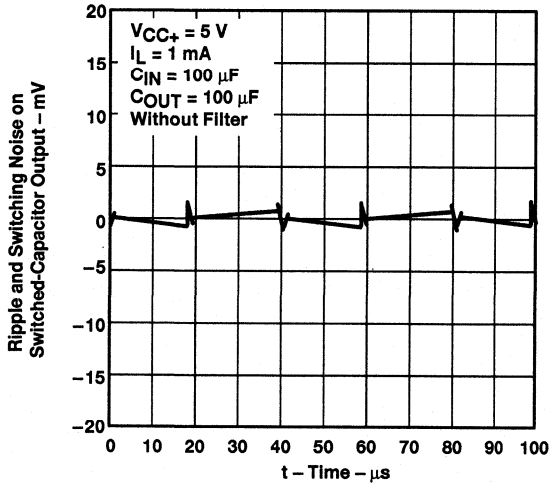


Figure 81

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

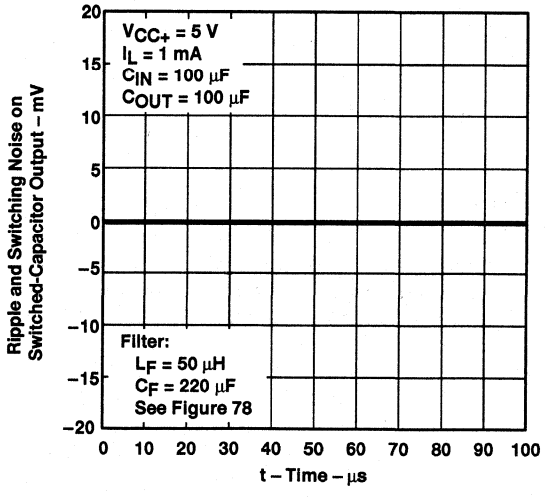


Figure 82

APPLICATION INFORMATION

As the load increases, filtering is still effective, but noise and ripple become more prominent (see Figure 83 through Figure 86):

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

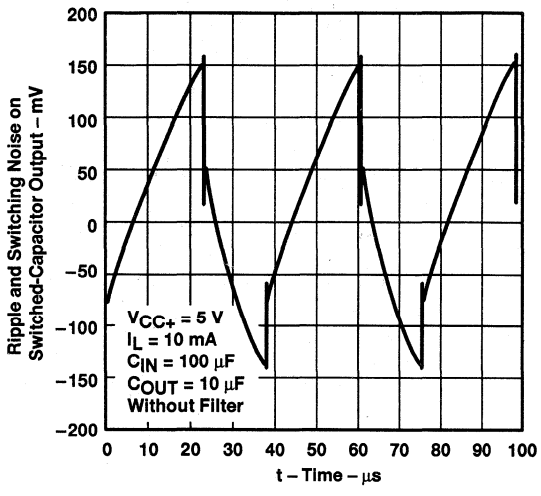


Figure 83

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

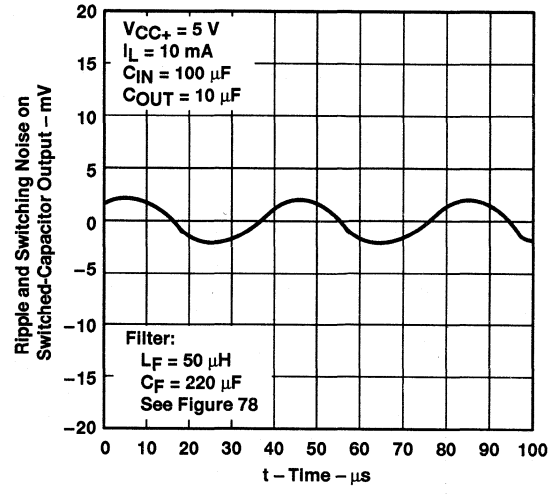


Figure 84

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

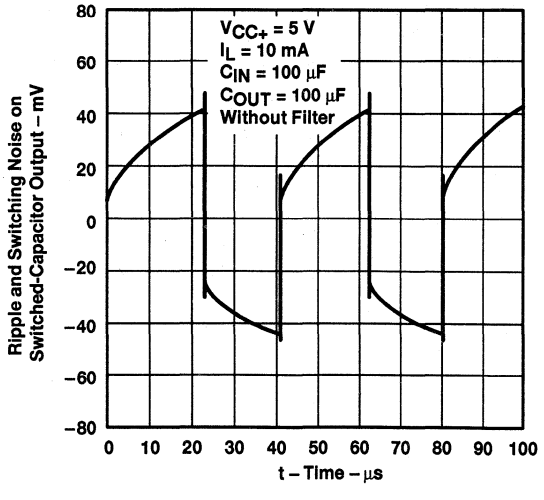


Figure 85

RIPPLE AND SWITCHING NOISE ON SWITCHED-CAPACITOR OUTPUT vs TIME

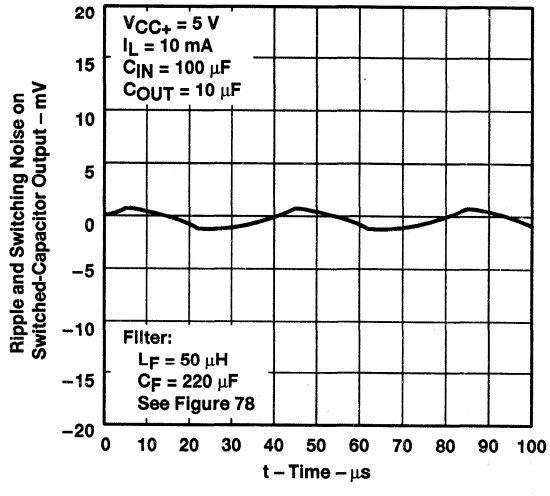


Figure 86

APPLICATION INFORMATION

Even with filtering, switching noise is coupled into the amplifier's signal path through ground. An example of this is shown in Figure 87 and Figure 88. This cannot be avoided. In systems where high-precision measurement is necessary, the shutdown pin, FB/SD, can be used to temporarily disable the switched-capacitor section while a measurement is being taken.

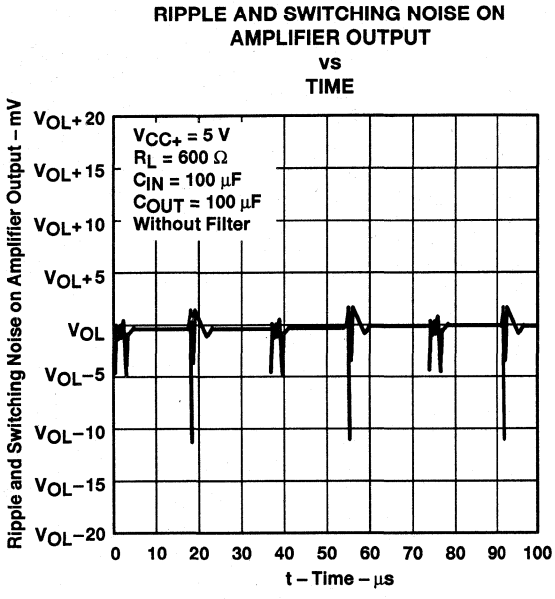


Figure 87

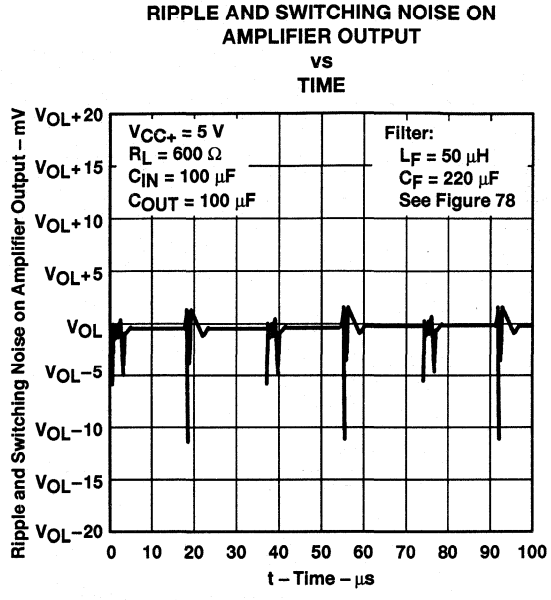


Figure 88

By applying a voltage of less than 0.45 V to FB/SD , the internal switches are set to dump any remaining charge onto C_{OUT}. The voltage at V_{OUT} decays to zero at a rate dependent on both the size of C_{OUT} and loading. During this time, the amplifier's outputs are free of any switching-induced ripple and noise. Figure 89 and Figure 90 show the decay and charge times of the negative supply when the amplifier is driving a 100-Ω load.

APPLICATION INFORMATION

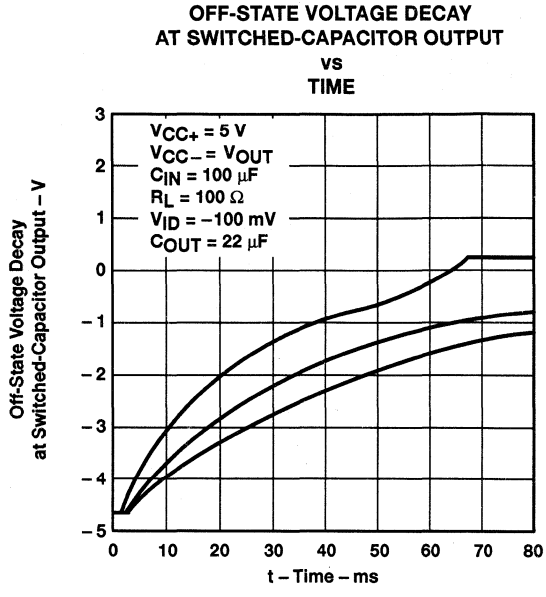


Figure 89

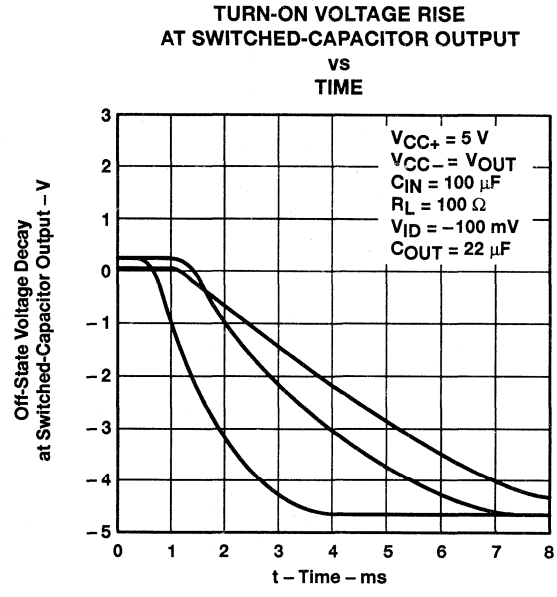


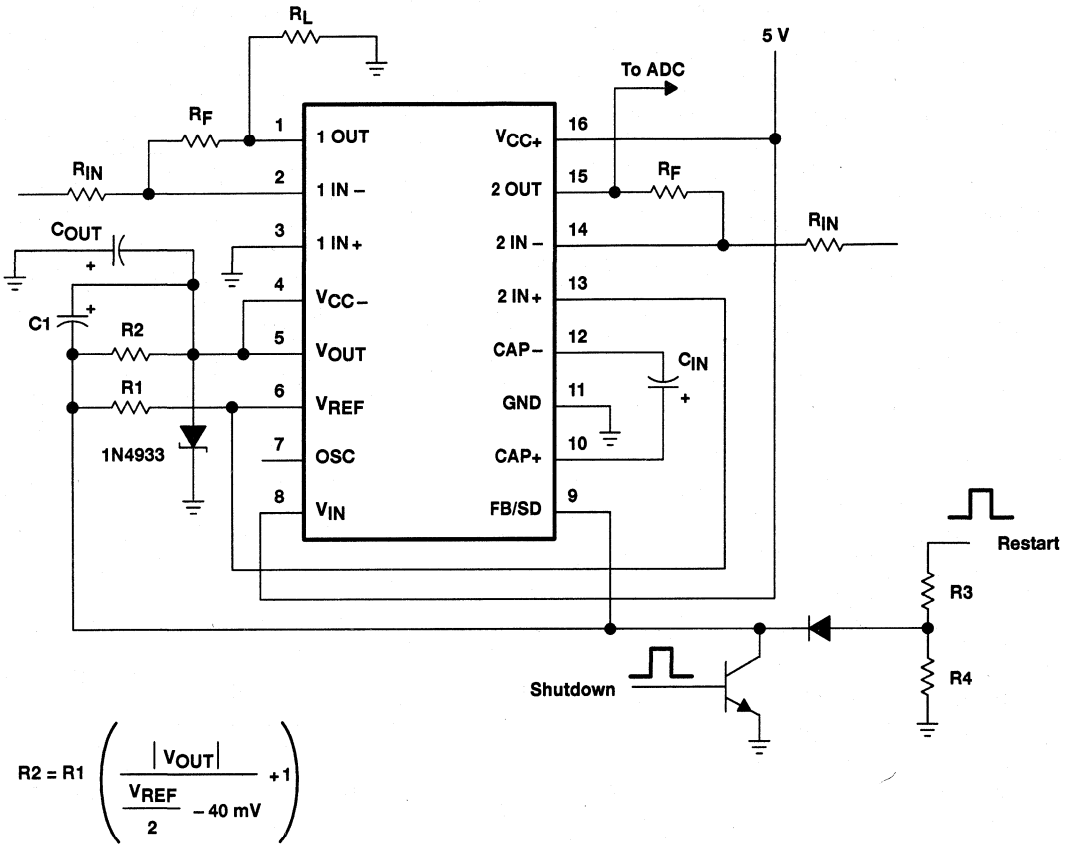
Figure 90

It is important to remember that the amplifier's negative common-mode input voltage limit (V_{ICR-}) is specified as an offset from the negative rail. Care should be taken to ensure that the input signal does not violate this limit as V_{OUT} decays. The negative output voltage swing is similarly affected by the gradual loss of the negative rail.

This application takes advantage of the otherwise unused V_{REF} output of the switched-capacitor block to bias one amplifier to 2.5 V. This is especially useful when the amplifier is followed by an ADC, keeping the signal centered in the middle of the converter's dynamic range. Other biasing methods may be necessary in precision systems.

In Figure 91, V_{REF}, R1, and R2 are used to generate a feedback voltage to the TLE2682's error amplifier. This voltage, fed into FB/SD, is used to regulate the voltage at V_{OUT}, thereby further reducing output ripple. When used this way, there is a higher voltage loss ($V_{IN} - |V_{OUT}|$) associated with the regulation. For example, the inverter generates an unregulated voltage of approximately –4.5 V from a positive 5-V source; it can achieve a regulated output voltage of only about –3.5 V. Though this reduces the amplifier's input and output dynamic range, both V_{ICR-} and V_{OL} still extends to below ground.

APPLICATION INFORMATION



$$R2 = R1 \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1 \right)$$

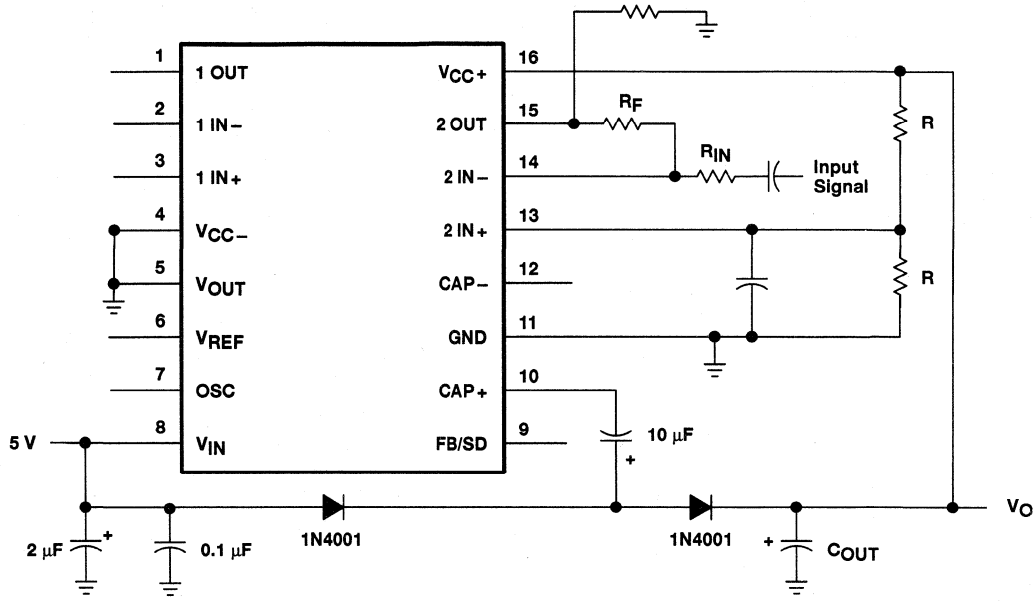
Where: V_{REF} = 2.5 V Nominal

Figure 91. Switched Capacitor Configured as Regulated Inverter

The reference voltage, though being used as part of the regulation circuitry, is still available for other uses if total current drawn from it is limited to under 60 μA. The shutdown feature remains available, though a restart pulse may be necessary to start the switched capacitor if the voltage on C_{OUT} is not fully discharged. This restart pulse is isolated from the feedback loop using a blocking diode. A more detailed discussion of this configuration can be found in the switched-capacitor section.

The TLE2682s switched-capacitor building block can also be configured as a positive doubler, extending the range of single-supply systems. This configuration is shown in Figure 92. As with the inverting configuration, noise and ripple components show up at the doubled output voltage and vary in magnitude with load. As before, filtering can be used to improve the output waveform; but unlike the voltage inverter, changing the size of C_{OUT} has little effect. Figure 93 through Figure 98 illustrate the effects of loading and filtering.

APPLICATION INFORMATION



V_{IN} = 3.5 V through 15 V

$V_O \approx 2\ V_{IN} - (V_L + 2\ V_{Diode})$

V_L = voltage loss switched-capacitor voltage converter

Figure 92. Voltage Converter Configured as Positive Doubler

APPLICATION INFORMATION

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

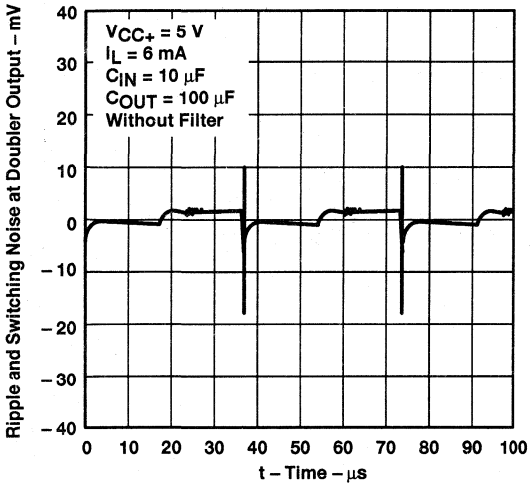


Figure 93

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

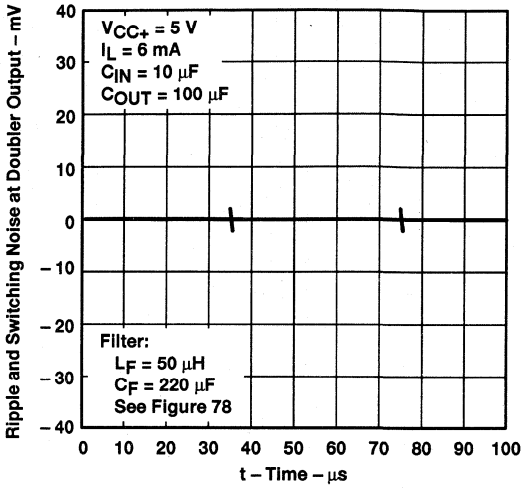


Figure 94

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

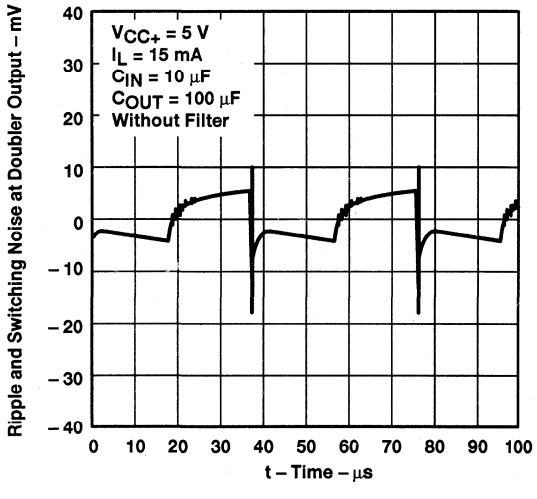


Figure 95

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT vs TIME

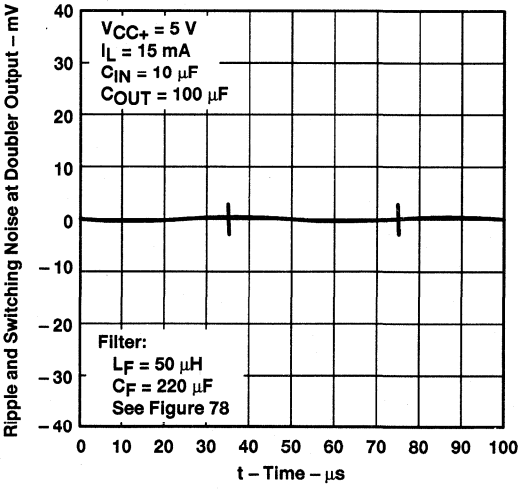


Figure 96

APPLICATION INFORMATION

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT VS TIME

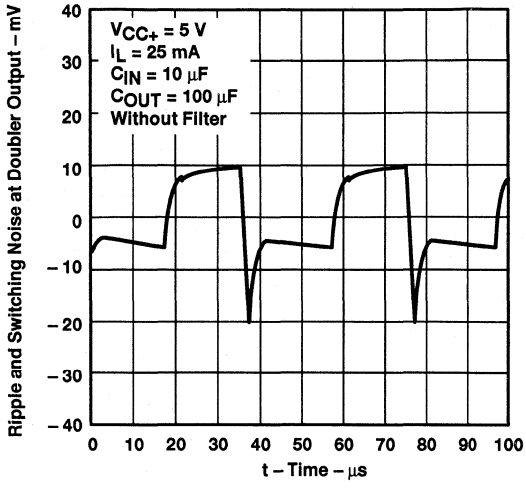


Figure 97

RIPPLE AND SWITCHING NOISE AT DOUBLER OUTPUT VS TIME

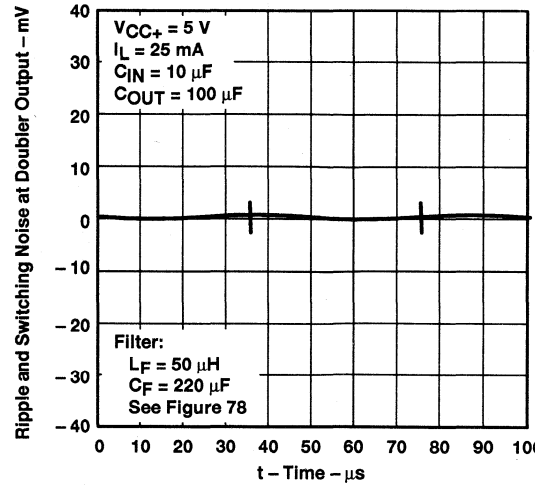


Figure 98

As with the inverter configuration, when the operational amplifiers are supplied using the voltage converter block, switching noise are coupled into the signal path through ground. Using the shutdown pin allows precision measurement of the output signal by an ADC by temporarily disabling the switching mechanism. Figure 99 and Figure 100 show the decay and charge times at the doubler output with the amplifier connected as shown.

APPLICATION INFORMATION

OFF-STATE VOLTAGE DECAY AT DOUBLER OUTPUT vs TIME

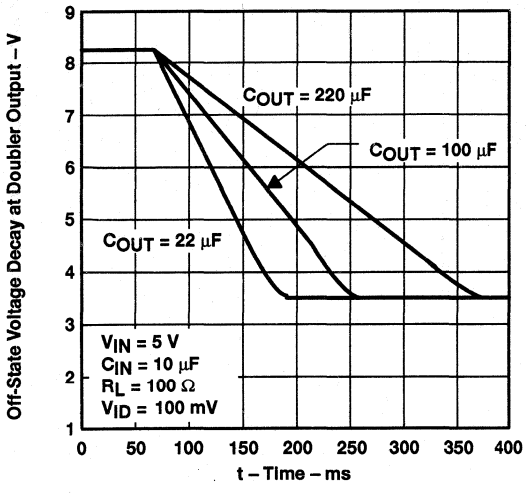


Figure 99

TURN-ON VOLTAGE RISE AT DOUBLER OUTPUT vs TIME

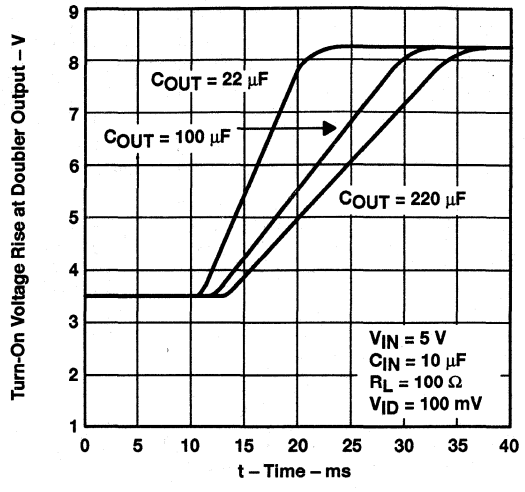


Figure 100

The circuit designer should be aware that the TLE2682 amplifier and switched-capacitor sections are tested and specified separately. Performance may differ from that shown in the Typical Characteristics section of this data sheet when they are used together. This is evident, for example, in the dependence of V_{ICR-} and V_{OL} on V_{CC-} as previously discussed. The impact of supplying the amplifier's negative rail using the switched-capacitor block in each design should be considered and carefully evaluated.

The more esoteric features of the switched-capacitor building block, including external synchronization of the internal oscillator and power dissipation considerations, are covered in detail in the following switched-capacitor building block application information section.

APPLICATION INFORMATION

switched-capacitor section

A review of a basic switched-capacitor building block is helpful in understanding the operation of the TLE2682. When the switch shown in Figure 101 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is $q1 = C1 \times V1$. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is $q2 = C1 \times V2$. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is as shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \quad (1)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is as shown in equation 2.

$$I = f \times \Delta q = f \times C1(V1 - V2) \quad (2)$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/f \times C1)} = \frac{V1 - V2}{R_{EQUIV}} \quad (3)$$

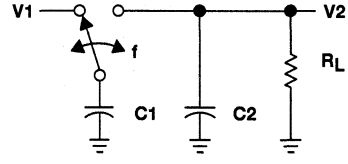


Figure 101. Switched-Capacitor Block

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div f \times C1$. The equivalent circuit for the switched-capacitor network is as shown in Figure 102. The TLE2682 has the same switching action as the basic switched-capacitor voltage converter. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 66). As oscillator frequency is decreased, the output impedance is eventually dominated by the $1/f \times C1$ term and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle when multiplied by the switching frequency becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the TLE2682 switched-capacitor section is designed to run in the frequency band where voltage losses are at a minimum.

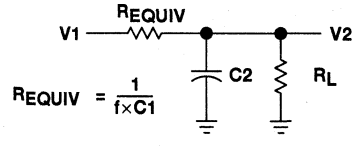


Figure 102. Switched-Capacitor Equivalent Circuit

APPLICATION INFORMATION

pin functions (see functional block diagram – converter)

Supply voltage (V_{IN}) alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current is approximately 2.2 times the output current. During the time that C_{IN} is delivering a charge to C_{OUT}, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the TLE2682 switched-capacitor section and averages out the current drawn from the supply. A minimum input supply bypass capacitor of 2 μF, preferably tantalum or some other low-ESR type, is recommended. A larger capacitor is desirable in some cases. An example is when the actual input supply is connected to the TLE2682 through long leads or when the pulse currents drawn by the TLE2682 might affect other circuits through supply coupling.

In addition to being the output pin, V_{OUT} is tied to the substrate of the device. Special care must be taken in TLE2682 circuits to avoid making V_{OUT} positive with respect to any of the other pins. For circuits with the output load connected from V_{CC+} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external Schottky diode must be added (see Figure 103). This diode prevents V_{OUT} from being pulled above the GND during start up. A fast recovery diode such as IN4933 with low forward voltage ($V_f \approx 0.2$ V) can be used.

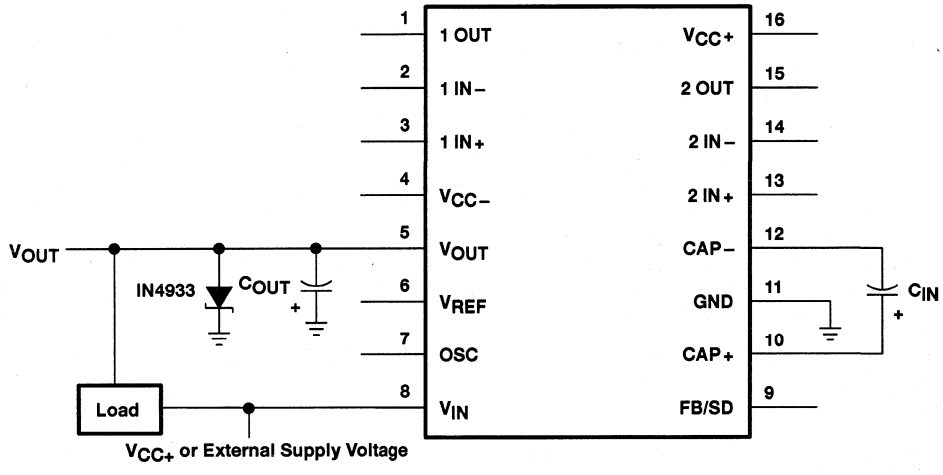


Figure 103. Circuit With Load Connected From V_{CC} to V_{OUT}

The voltage reference (V_{REF}) output provides a 2.5-V reference point for use in TLE2682-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This nonzero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator feedback networks, reference output current should be limited to approximately 60 μA. V_{REF} draws approximately 100 μA when shorted to ground and does not affect the internal reference/regulator. This pin can also be used as a pullup for TLE2682 circuits that require synchronization.

APPLICATION INFORMATION

pin functions (continued)

CAP+ is the positive side of input capacitor C_{IN} and is alternately driven between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP– is the negative side of the input capacitor and is driven alternately between ground and V_{OUT}. When driven to ground, CAP– sinks current to ground. When driven to V_{OUT}, CAP– sources current from C_{OUT}. In all cases, current flow in the switches is unidirectional as should be expected when using bipolar switches.

OSC can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is alternately charged and discharged by current sources of ±7 µA so that the duty cycle is approximately 50%. The TLE2682 switched-capacitor section oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 104) in the range of 5 pF–20 pF from CAP+ to OSC. This capacitor couples a charge into C_t as the switch transitions. This shortens the charge and discharge time and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to V_{REF}. A 20-kΩ pullup resistor is recommended. An open-collector gate or an npn transistor can then be used to drive OSC at the external clock frequency as shown in Figure 104.

The frequency can be lowered by adding an external capacitor (C1 in Figure 104) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.

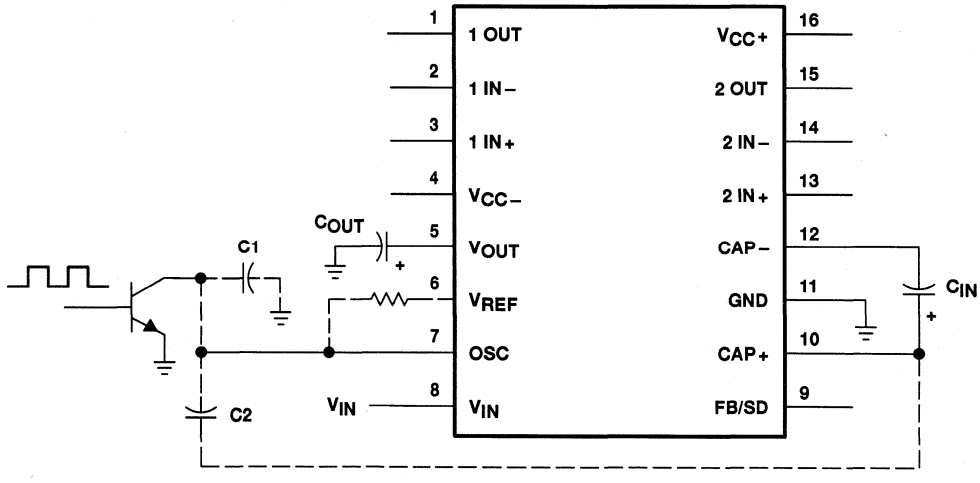


Figure 104. External Clock System

The feedback/shutdown (FB/SD) pin has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 µA. Any open-collector gate can be used to put the TLE2682 into shutdown. For normal (unregulated) operation, the device restarts when the external gate is shut off. In TLE2682 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where

APPLICATION INFORMATION

pin functions (continued)

the TLE2682 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the TLE2682.

Using the circuit shown in Figure 105, the restart signal can be either a pulse ($t_p > 100\ \mu s$) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 105 should be chosen to provide a signal level at FB/SD of 0.7 V–1.1 V. FB/SD is also the inverting input of the TLE2682 switched-capacitor section error amplifier and, as such, can be used to obtain a regulated output voltage.

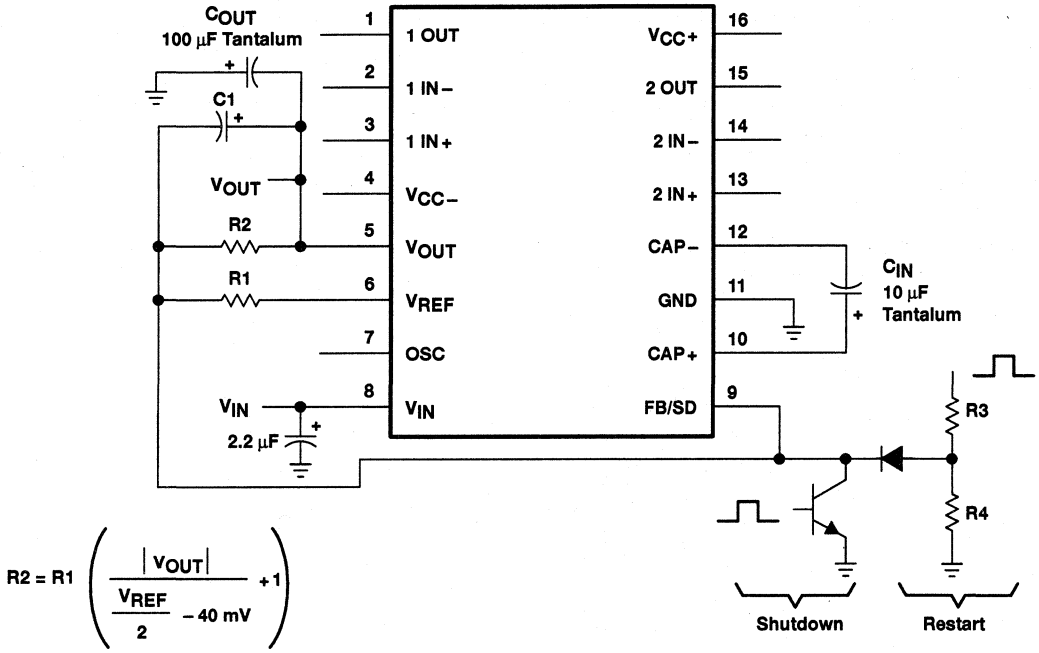


Figure 105. Basic Regulation Configuration

regulation

The error amplifier of the TLE2682 switched-capacitor section drives the npn switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the TLE2682 is used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 105 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 µA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}. For best results, this ratio should be approximately 1 to 10. Capacitor C1, required for good load regulation, should be 0.002 µF for all output voltages.

APPLICATION INFORMATION

regulation (continued)

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referenced to GND of the TLE2682 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves.

capacitor selection

While the exact values of C_{IN} and C_{OUT} are noncritical, good-quality low-ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the equivalent series resistance (ESR) of the capacitor is multiplied by four since switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the switched-capacitor section by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A smaller tantalum capacitor can be connected in parallel with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as shown in equation 4:

$$\Delta V = \frac{I_{OUT}}{2\, f \times C_{OUT}} \tag{4}$$

where:

ΔV = peak-to-peak ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})\ (\text{ESR of } C_{OUT}) \tag{5}$$

power dissipation (switched-capacitor section only)

The power dissipation of any TLE2682 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation is calculated from two components: the power loss due to voltage drops in the switches and the power loss due to drive current losses. The total power dissipated by the TLE2682 is calculated as shown in equation 6:

$$P \approx (V_{CC} - |V_{OUT}|)\, I_{OUT} + (V_{CC})\ (I_{OUT})\ (0.2) \tag{6}$$

where both V_{CC} and V_{OUT} refer to GND. The power dissipation is equivalent to that of a linear regulator. Due to limitations of the DW package, steps must be taken to dissipate power externally for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 106. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor value is calculated as follows:

$$R_X = V_X/(4.4\ I_{OUT})$$

where:

$$V_X \approx V_{CC} - \left[(\text{TLE2682 voltage loss})\ (1.3) + |V_{OUT}|\right] \tag{7}$$

I_{OUT} = maximum required output current

APPLICATION INFORMATION

power dissipation (continued)

The factor of 1.3 allows some operating margin for the TLE2682.

When using a 12-V to −5-V converter at 100-mA output current, calculate the power dissipation without an external resistor:

$$P = (12\ V - |-5\ V|)\ (100\ mA) + (12\ V)\ (100\ mA)\ (0.2) \quad (8)$$

$$P = 700\ mW + 240\ mW = 940\ mW$$

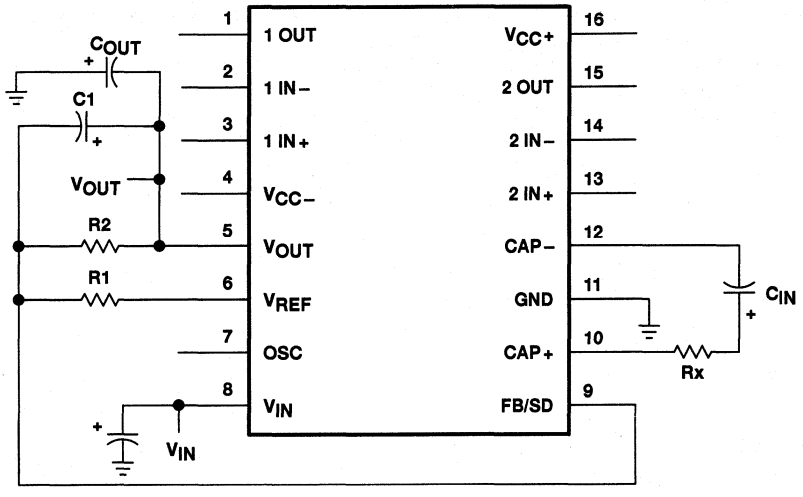


Figure 106. Power-Dissipation-Limiting Resistor in Series With C_{IN}

At θ_{JA} of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C is seen. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the TLE2682 in the standard regulator configuration at 100 mA output current is 1.6 V.

$$V_X = 12\ V - [(1.6\ V)\ (1.3) + |-5\ V|] = 4.9\ V \quad \text{and} \quad (9)$$

$$R_X = 4.9\ V/(4.4)\ (100\ mA) = 11\ \Omega$$

The resistor reduces the power dissipated by the TLE2682 by (4.9 V) (100 mA) = 490 mW. The total power dissipated by the TLE2682 is equal to (940 mW – 490 mW) = 450 mW. The junction temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the TLE2682 packages represent worst-case numbers with no heat-sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the TLE2682 package. Airflow in some systems helps to lower the thermal resistance. Wide PC board traces from the TLE2682 leads help to remove heat from the device. This is especially true for plastic packages.

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C**
- **Wide Supply Voltage Range 2.7 V to 8 V**
- **Macromodel Included**

description

The TLV2262 and TLV2262A are dual operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μpower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2262 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV,allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 μA (typical) of supply current per amplifier, the TLV2262 family can achieve input offset voltage levels as low as 950 μV, outperforming existing CMOS amplifiers. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

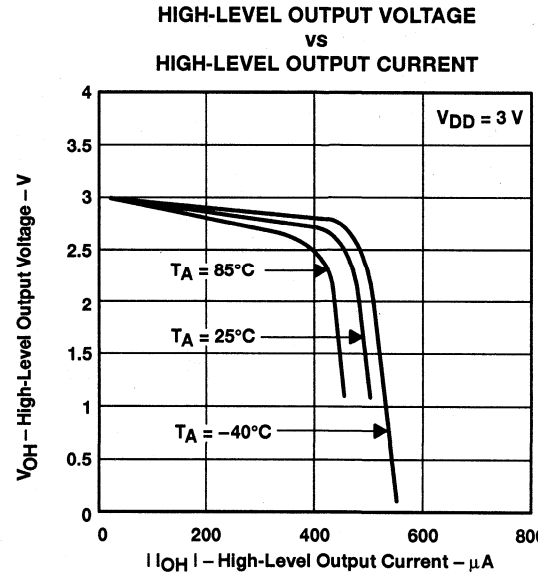


Figure 1

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	950 μV	TLV2262AID	TLV2262AIP	TLV2262AIPWLE	TLV2262Y
	2.5 mV	TLV2262ID	TLV2262IP	—	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2262IDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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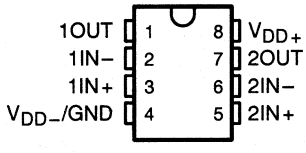
description (continued)

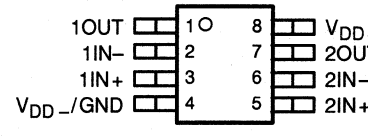
The TLV2262 and TLV2262A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to ADCs. All of these features combined with its temperature performance make the TLV2262 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

D OR P PACKAGE
(TOP VIEW)



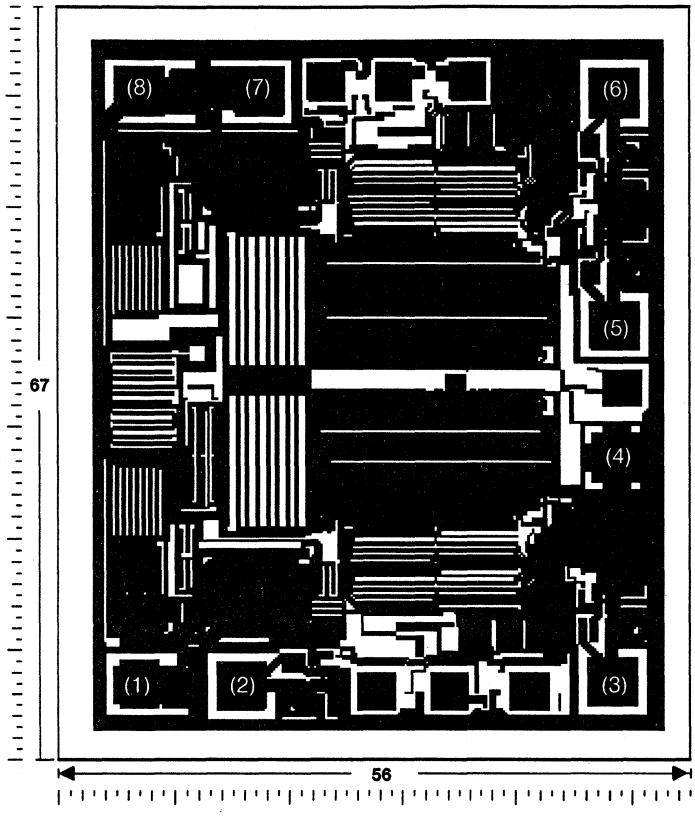
PW PACKAGE
(TOP VIEW)

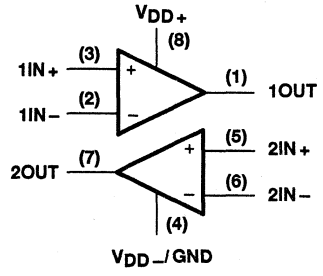


TLV2262Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2262. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

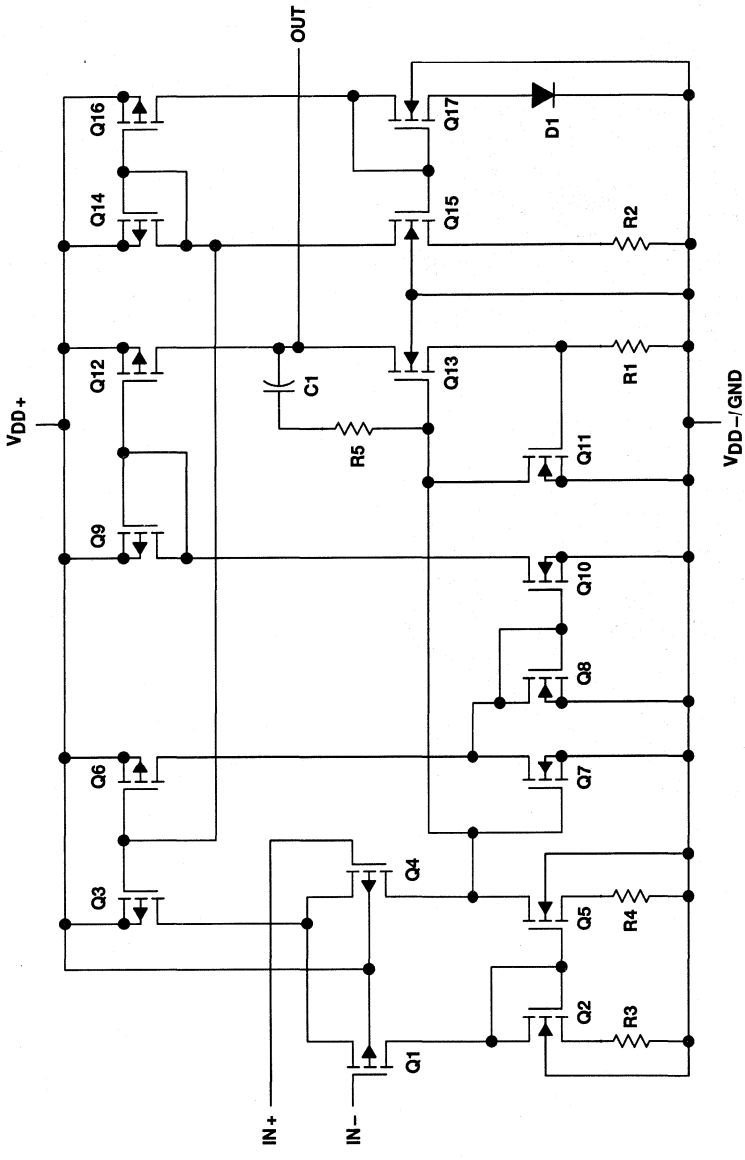
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	38
Diodes	9
Resistors	26
Capacitors	3

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) ..... −0.3 V to V_{DD}
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} ..... ±50 mA
Total current out of V_{DD-} ..... ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD+} (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −200 μA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		300			300		kHz
	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		61°			61°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −200 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ‡	25°C		550			550		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262			TLV2262A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2262Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm$ = ±1.5 V, V_O = 0,	V_{IC} = 0,	R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current					0.5	150	pA
I_{IB}	Input bias current					1	150	pA
V_{ICR}	Common-mode input voltage range	$|V_{IO}|\leq$5 mV,	R_S = 50 Ω		0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				2.99		V
		I_{OH} = −200 μA			2.7	2.75		
V_{OL}	Low-level output voltage	V_{IC} = 0 V,	I_{OL} = 50 μA			10		V
		V_{IC} = 0 V,	I_{OL} = 500 μA			100	125	
		V_{IC} = 0 V,	I_{OL} = 1 mA			200	250	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 50 kΩ†		60	100		V/mV
			R_L = 1 MΩ†			100		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω	65	77		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load	80	100		dB
I_{DD}	Supply current	V_O = 0,	No load			400	500	μA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2262Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current				0.5	150	pA
I_{IB}	Input bias current				1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.99		V
		I_{OH} = −100 μA		4.85	4.94		
		I_{OH} = −200 μA		4.7	4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA		0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†	80	170		V/mV
			R_L = 1 MΩ†		550		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V, R_S = 50 Ω	70	83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, No load	V_{IC} = V_{DD}/2,	80	95		dB
I_{DD}	Supply current	V_O = 2.5 V,	No load		400	500	μA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

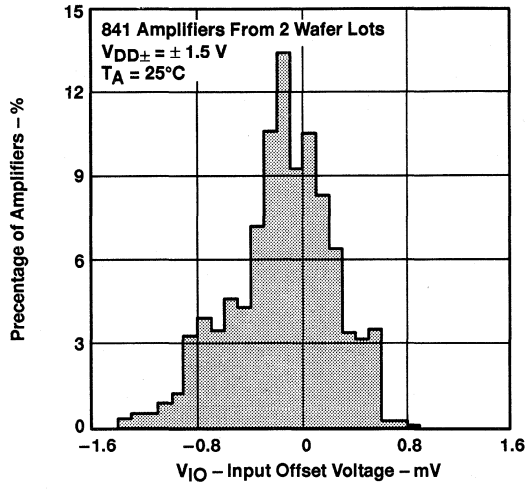


Figure 2

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

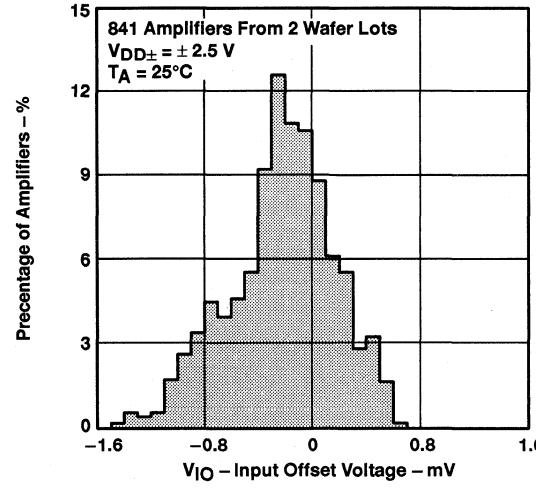


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

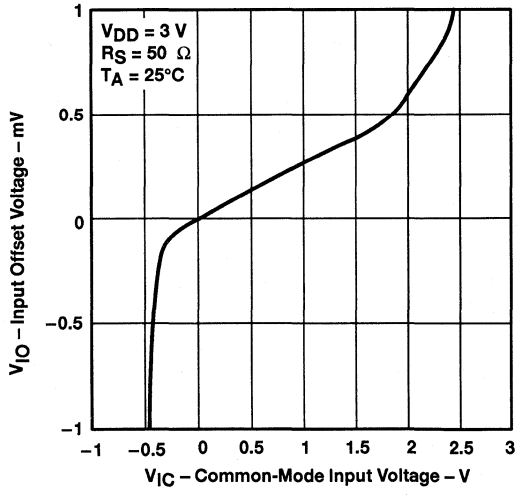


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

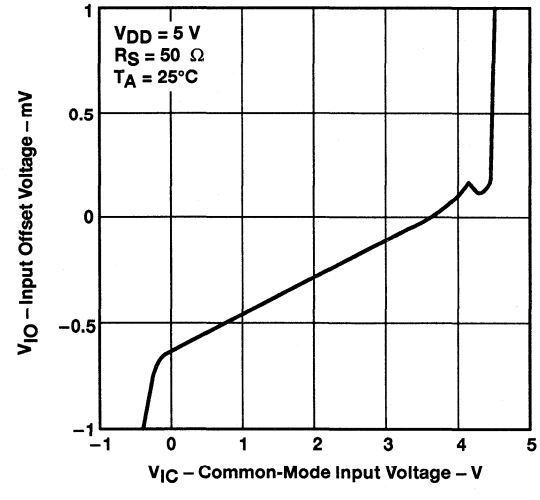


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

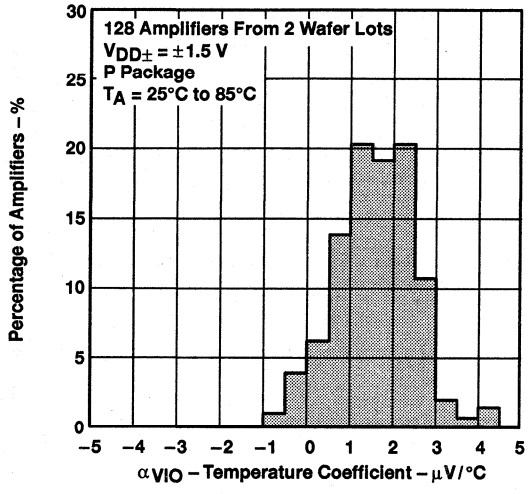


Figure 6

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

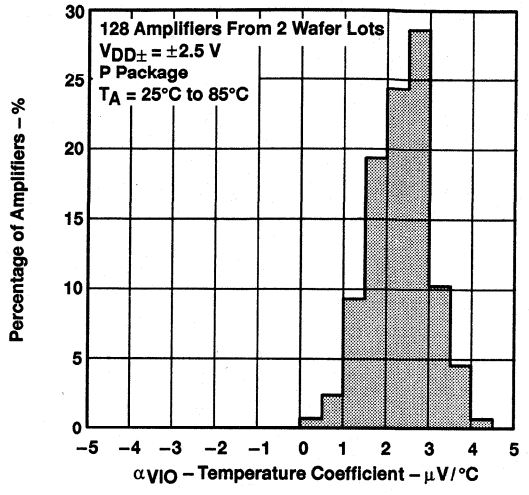


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

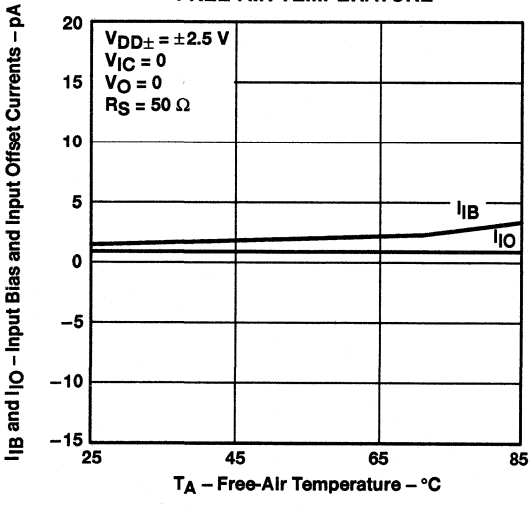


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

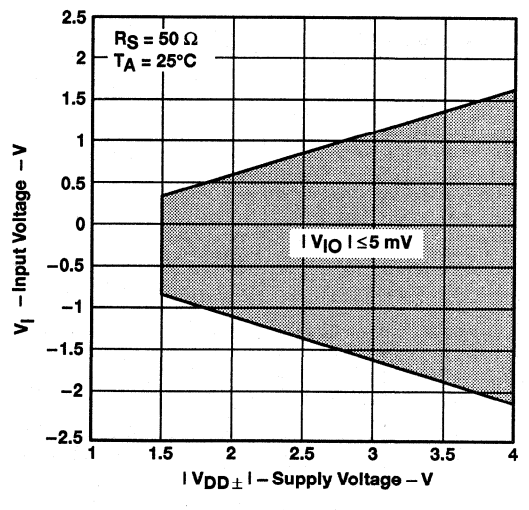


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE vs FREE-AIR TEMPERATURE

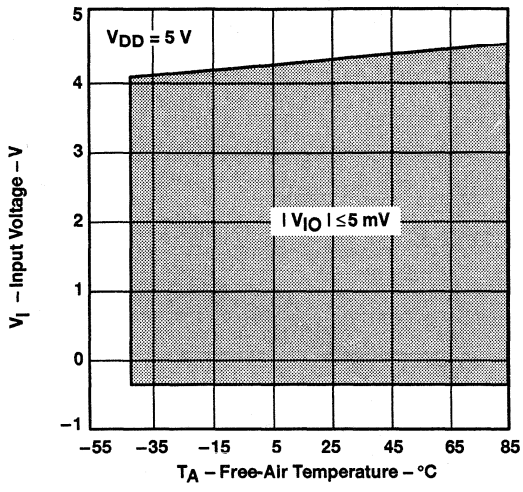


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

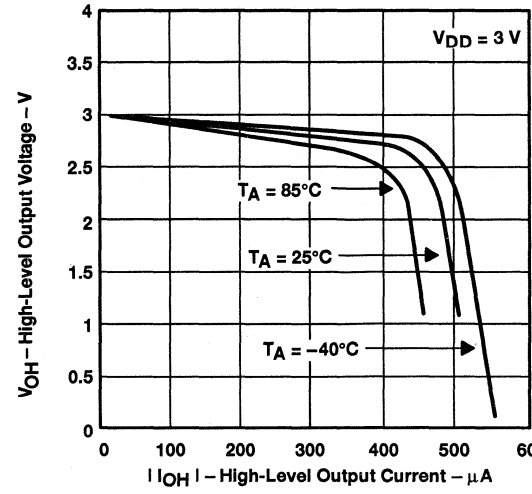


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

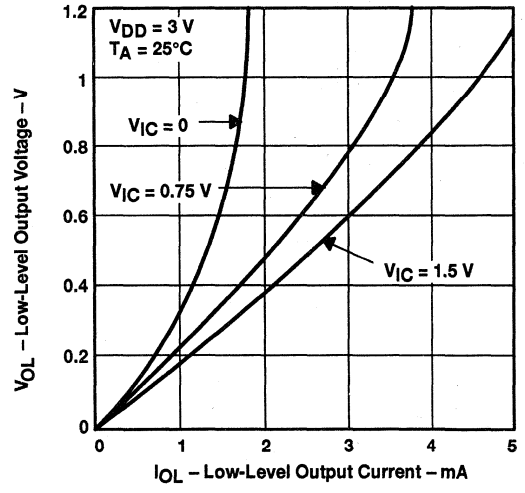


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

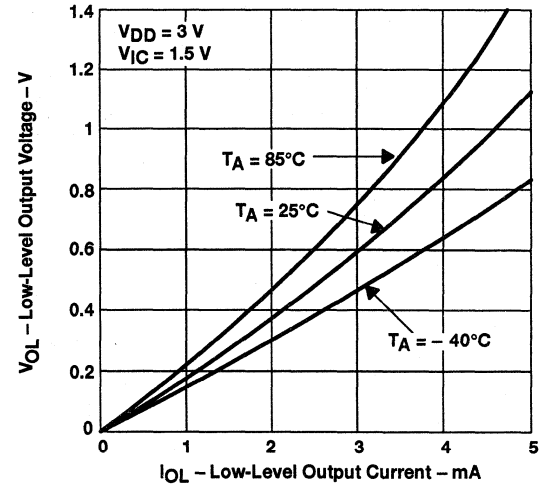


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

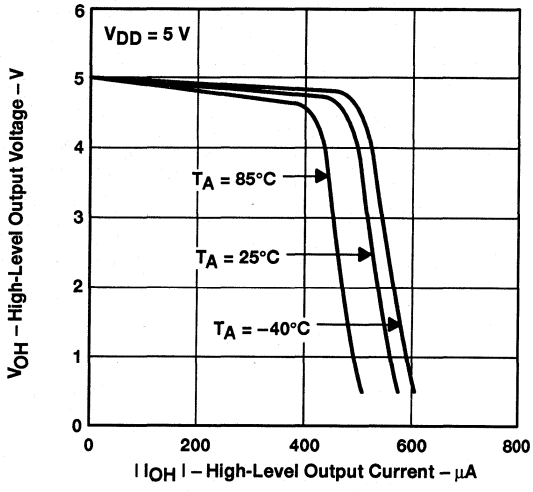


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

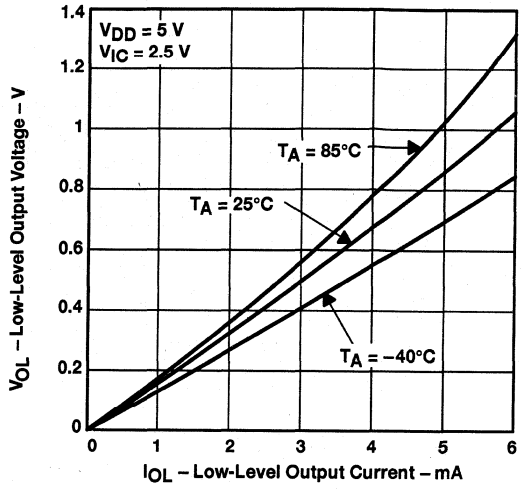


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

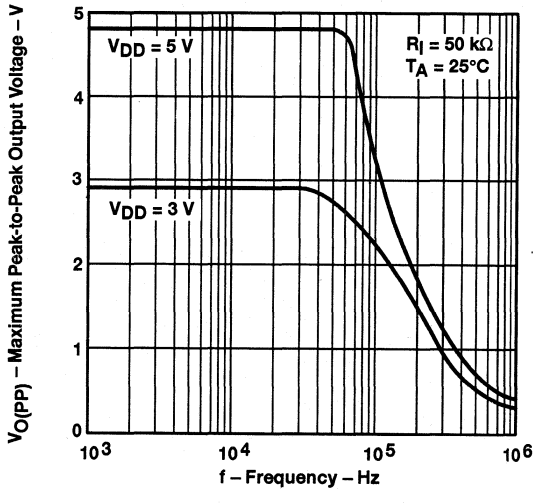


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

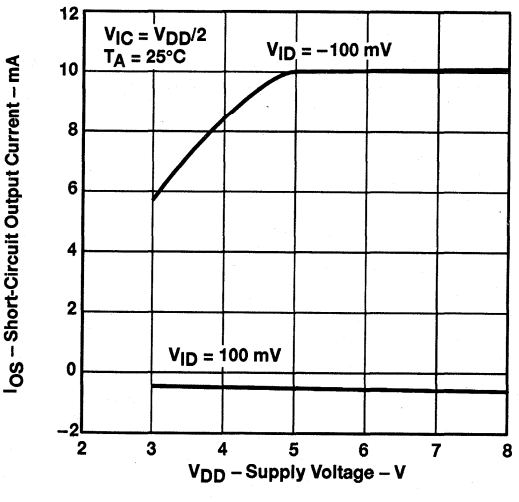


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

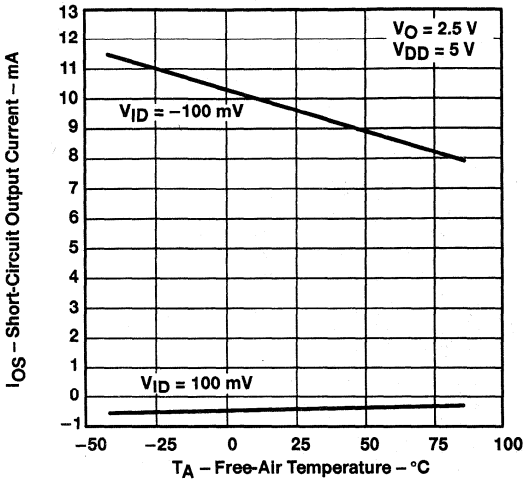


Figure 18

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

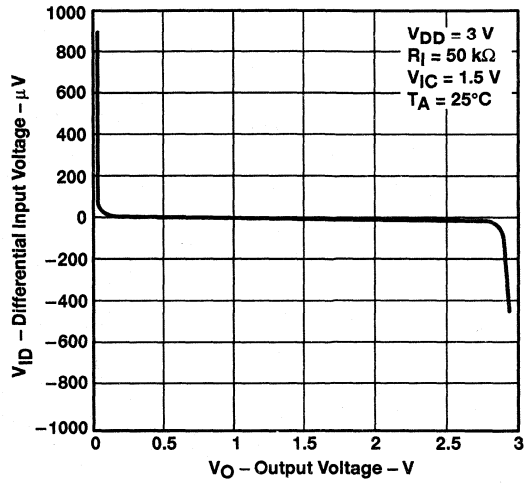


Figure 19

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

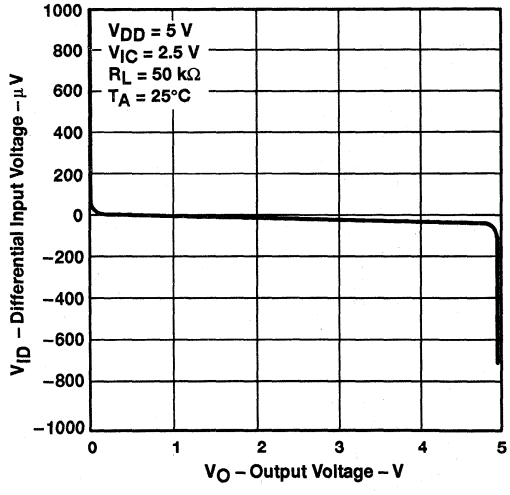


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

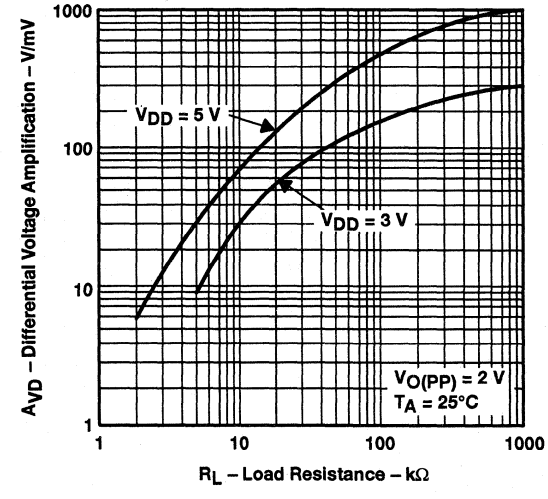


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

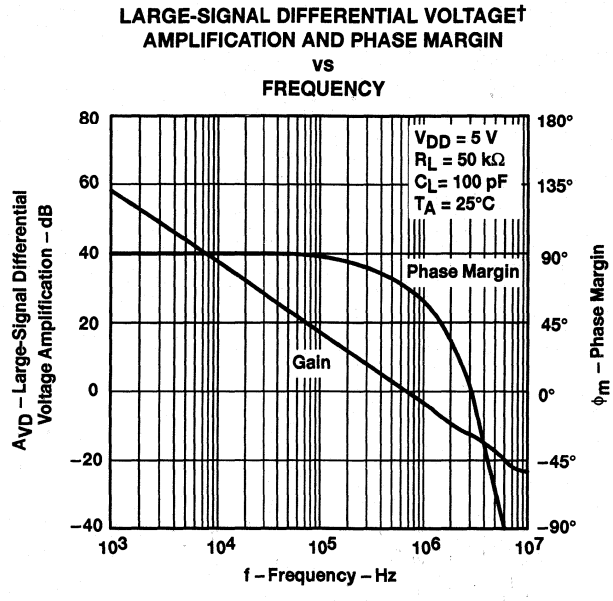


Figure 22

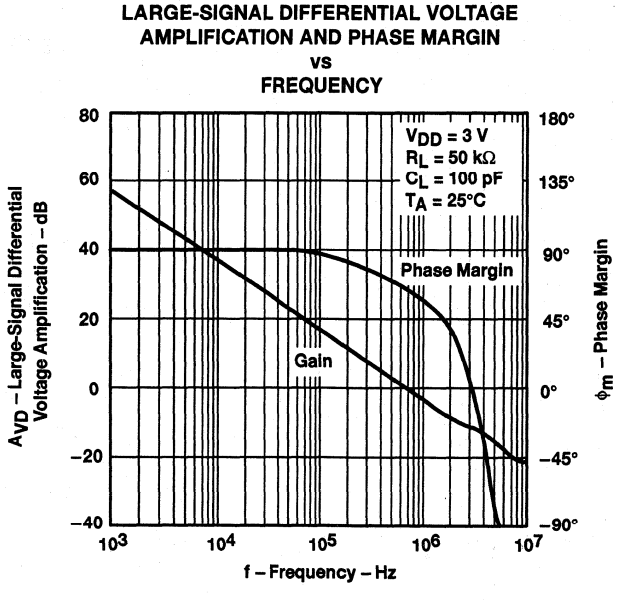


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

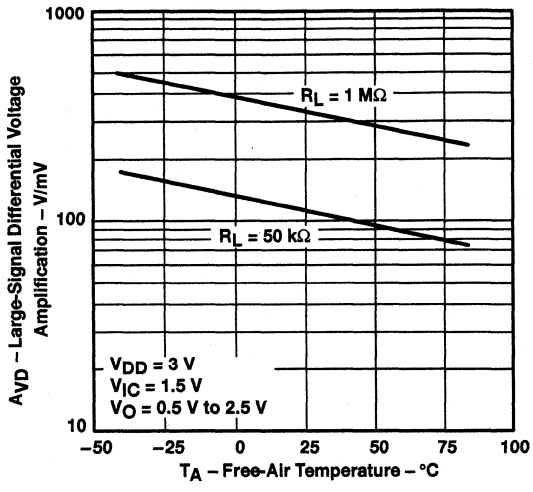


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

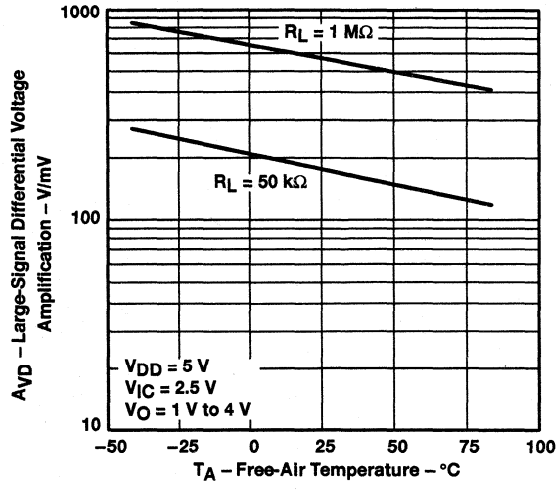


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

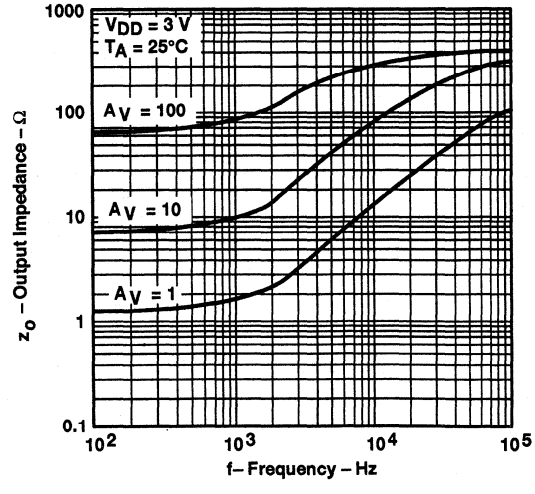


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

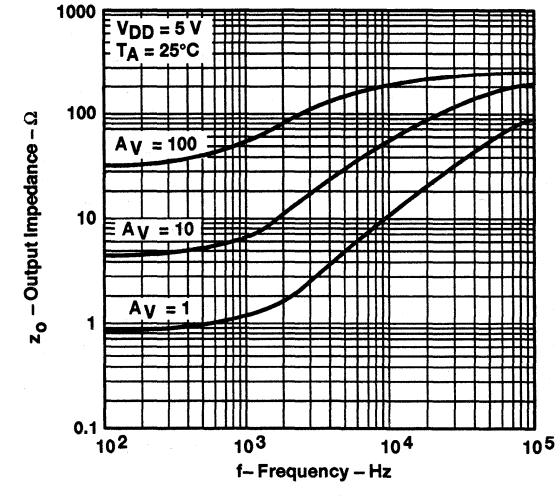


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO vs FREQUENCY

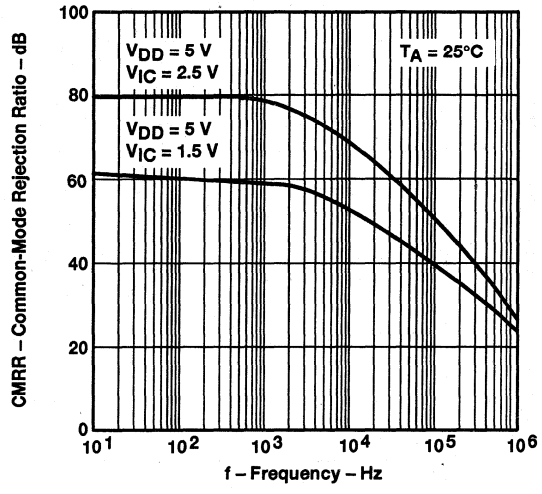


Figure 28

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

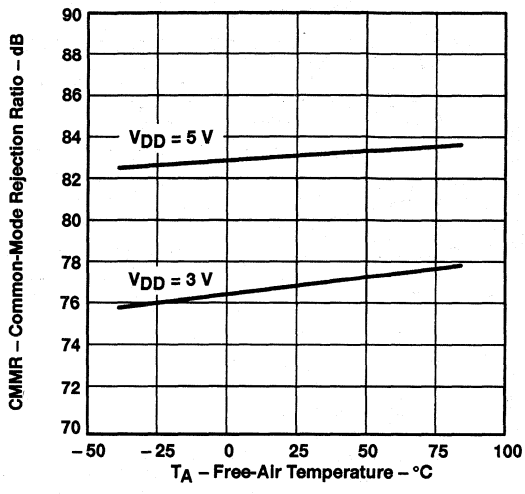


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

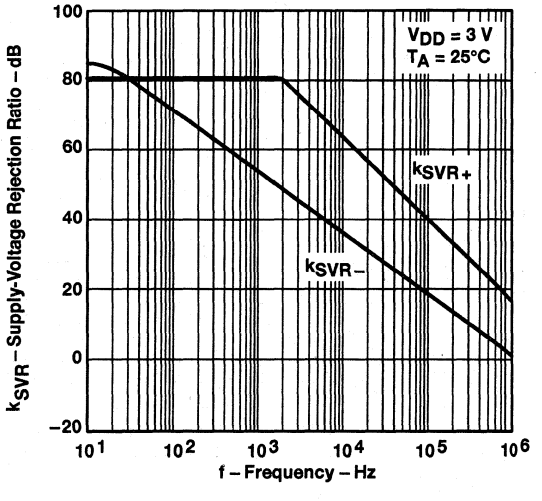


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

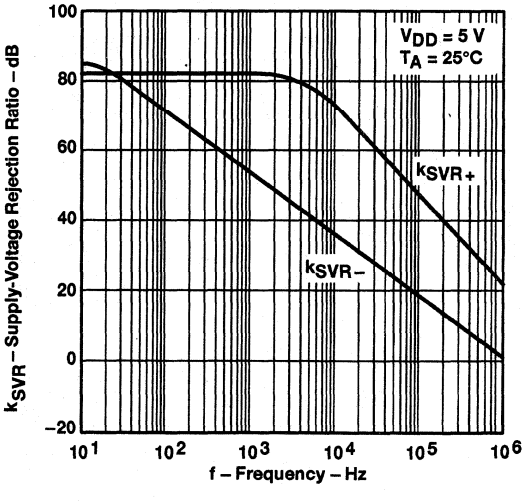


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

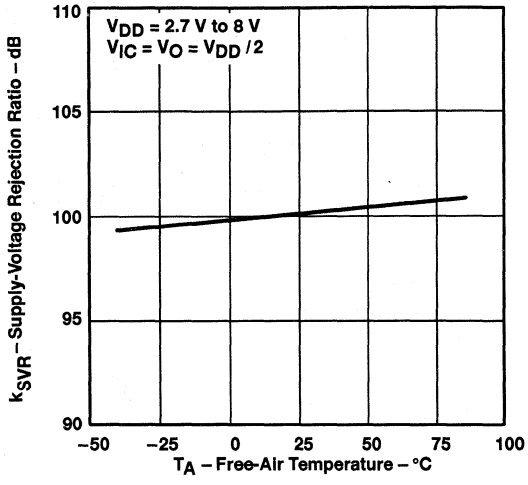


Figure 32

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

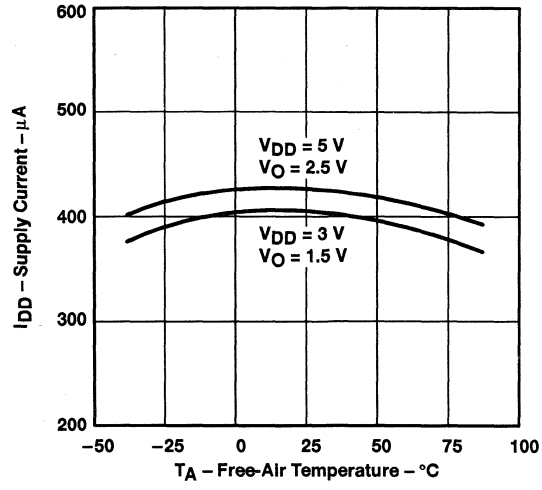


Figure 33

SLEW RATE vs LOAD CAPACITANCE

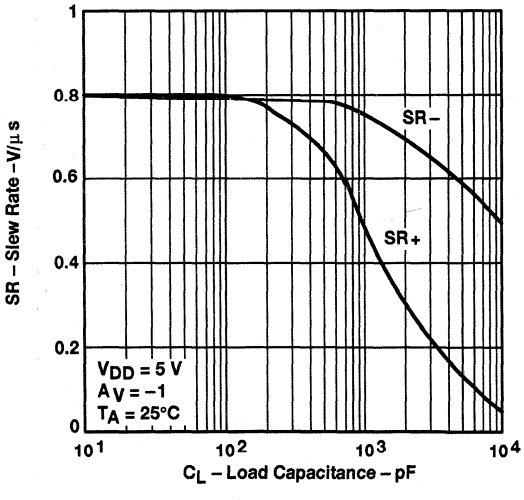


Figure 34

SLEW RATE vs FREE-AIR TEMPERATURE

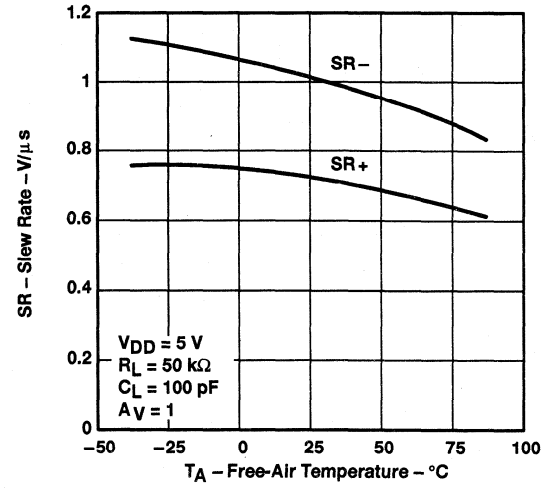


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

INVERTING LARGE-SIGNAL PULSE RESPONSE

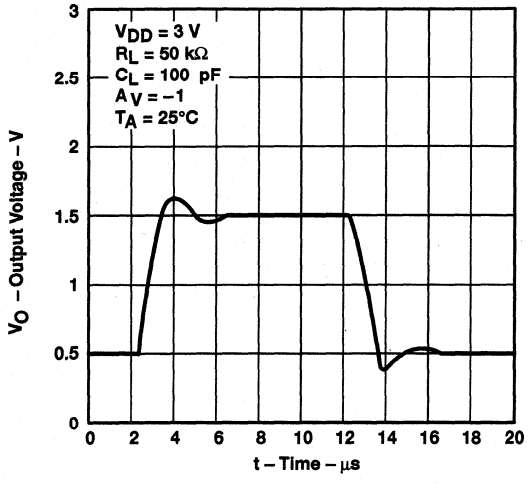


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

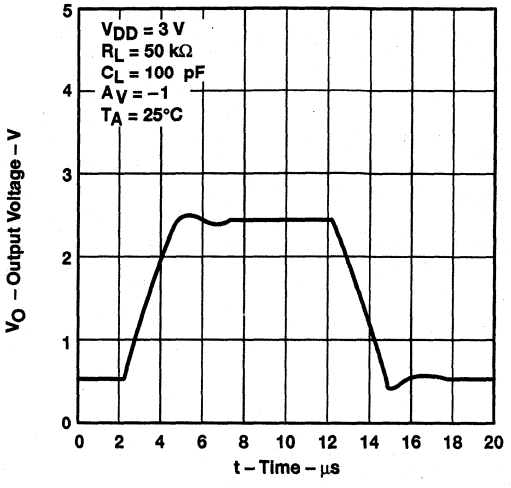


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

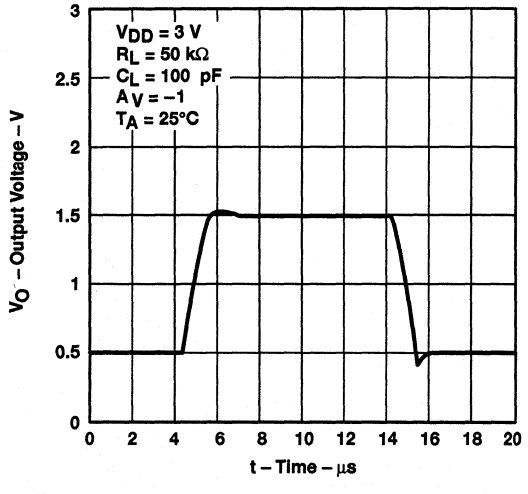


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

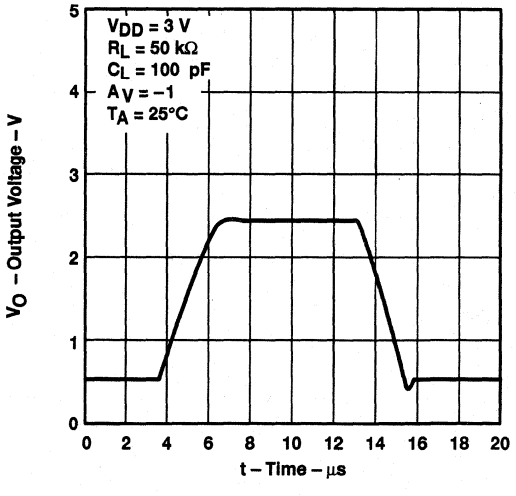


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING SMALL-SIGNAL
PULSE RESPONSE

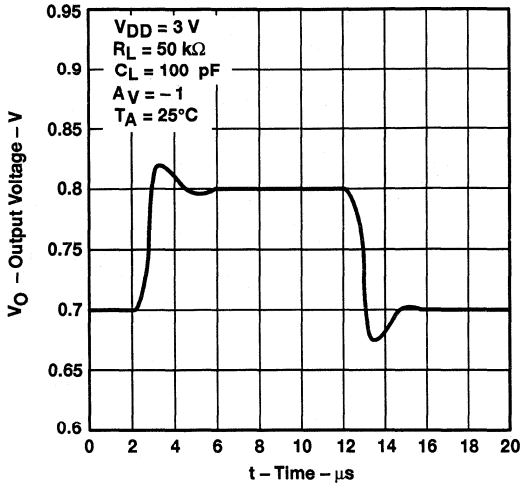


Figure 40

INVERTING SMALL-SIGNAL
PULSE RESPONSE

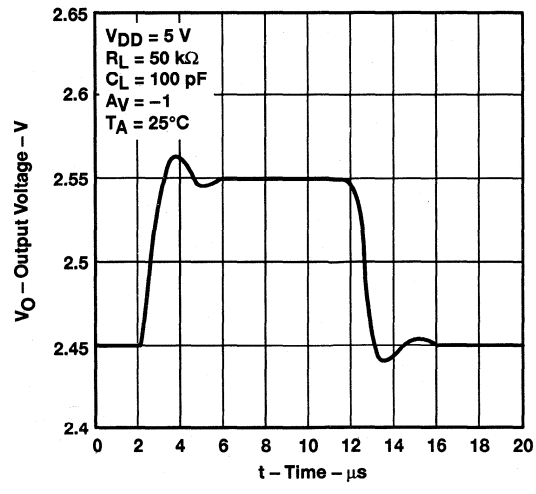


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

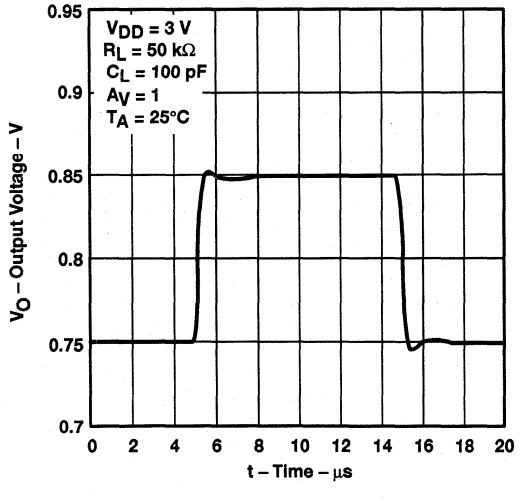


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

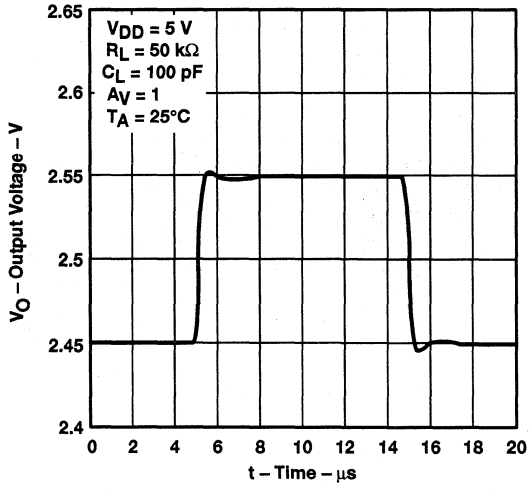


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

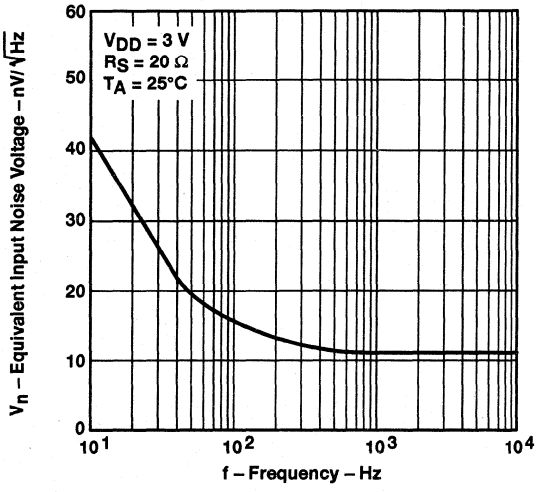


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

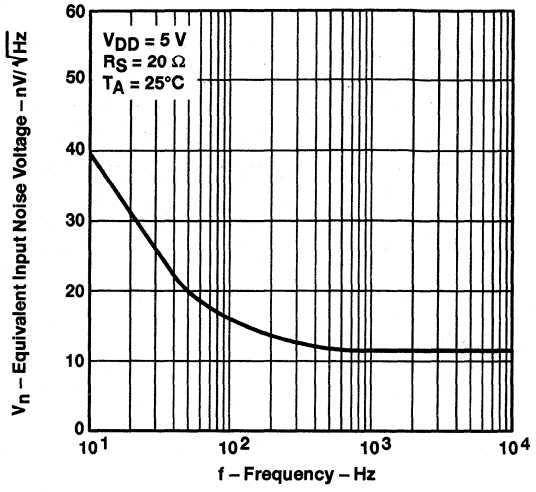


Figure 45

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

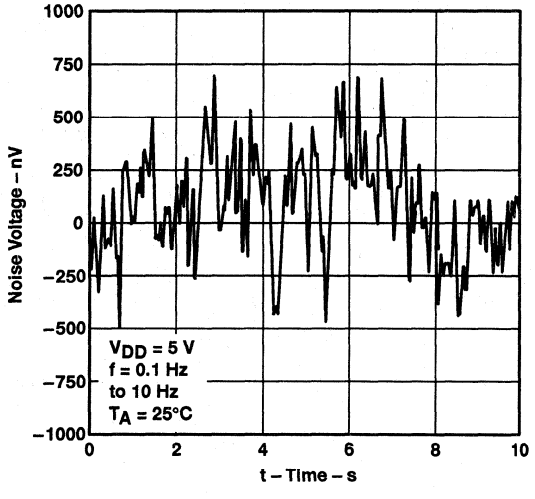


Figure 46

INTEGRATED NOISE VOLTAGE vs FREQUENCY

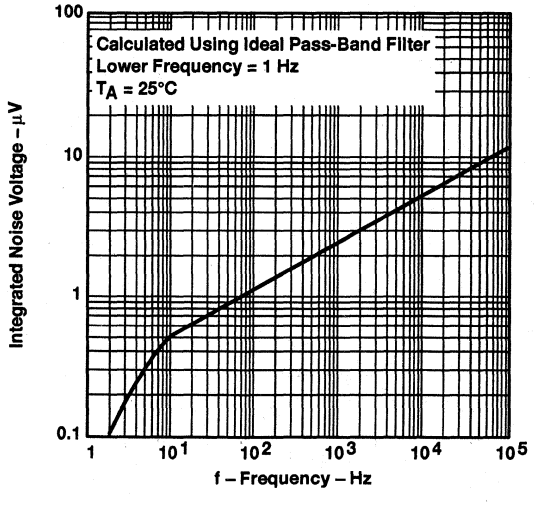


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

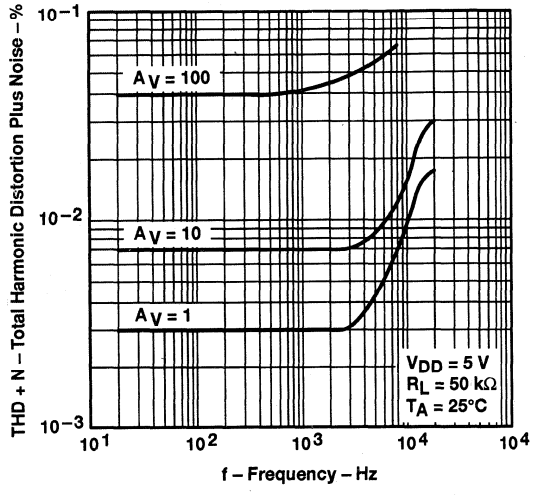


Figure 48

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

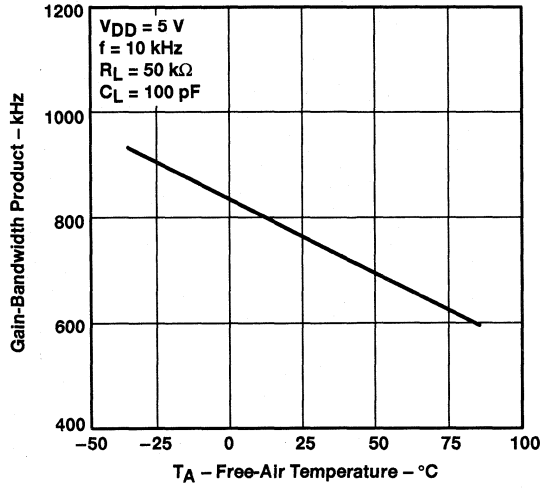


Figure 49

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

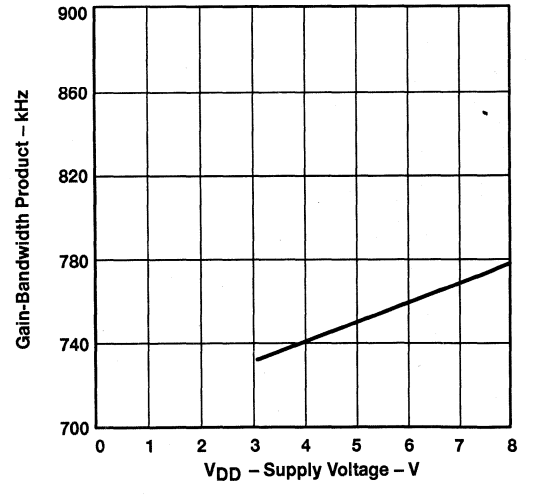


Figure 50

PHASE MARGIN vs LOAD CAPACITANCE

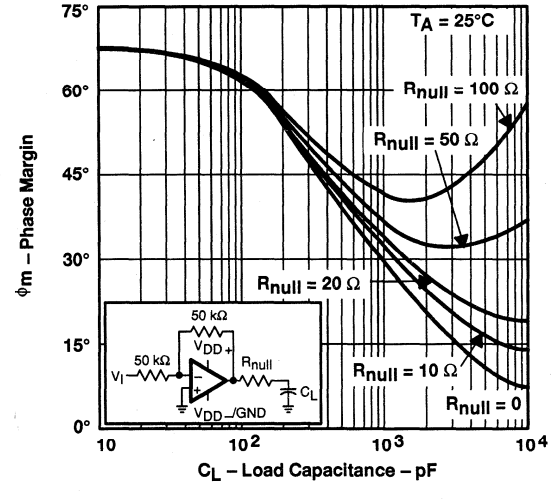


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

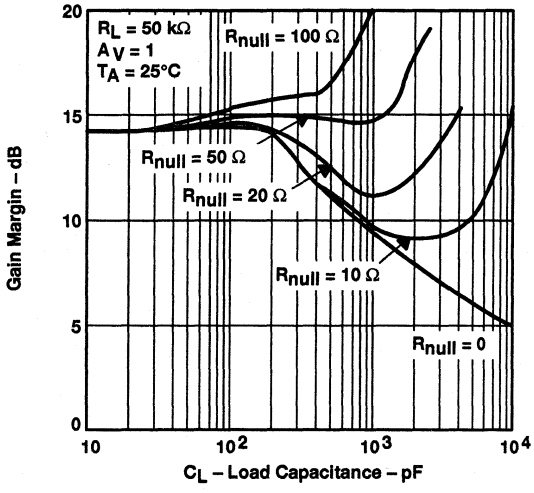


Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

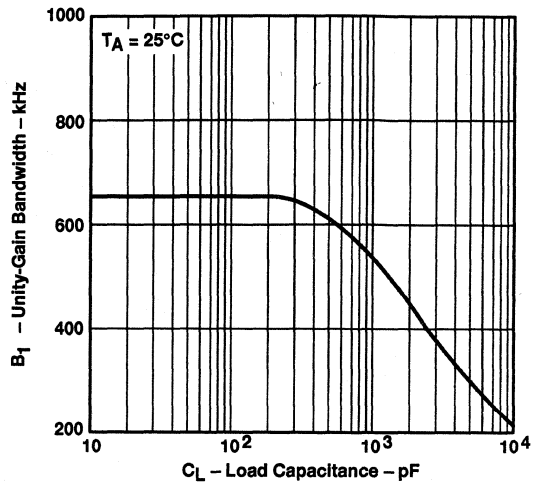
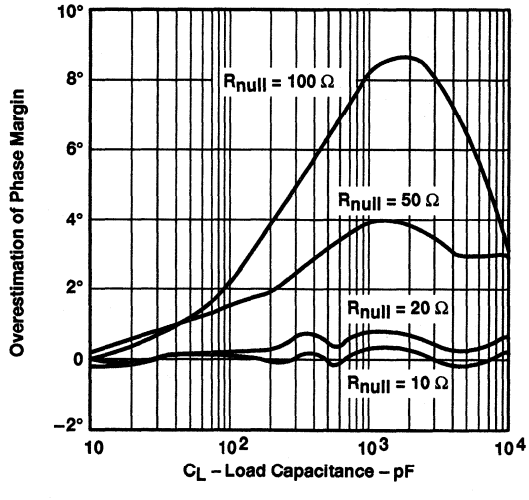


Figure 53

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE



† See application information

Figure 54

APPLICATION INFORMATION

loading considerations

The TLV2262 is a low-voltage, low-power version of the TLC2272 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLV2262 is similar to the TLC2272 and is capable of driving several milliamperes.

The design topology used for the TLV2262 or the TLV2272 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. While the TLV2272 is capable of greater than 1-mA drive from the positive rail, the TLV2262 is capable of only a few hundred microamperes. When designing with lower impedance loads (less than 50 kΩ) with the TLV2262, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLV2262 topology provides lower drive to the positive rail than other high-output-drive rail-to-rail operational amplifiers, it is a more stable topology.

driving large capacitive loads

The TLV2262 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

where :

$\Delta\theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

where :

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

APPLICATION INFORMATION

driving large capacitive loads (continued)

For the TLV2262, the pole associated with the load is typically 6 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 60 MHz, at C_L = 1000 pF, use 600 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone [equation (1)]. Equation (3) approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation (1) to better approximate the improvement in phase margin.

$$\Delta\theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \quad (3)$$

where :

$\Delta\theta_{m2}$ = reduction in phase margin
UGBW = unity-gain bandwidth frequency
F = factor from equation (2)
P_2 = unadjusted pole (60 MHz @ 10 pF, 6 MHz @100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

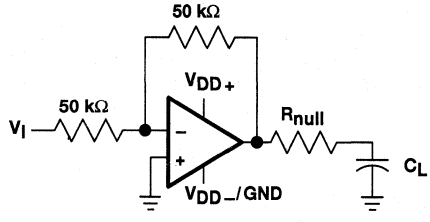


Figure 55. Series-Resistance Circuit

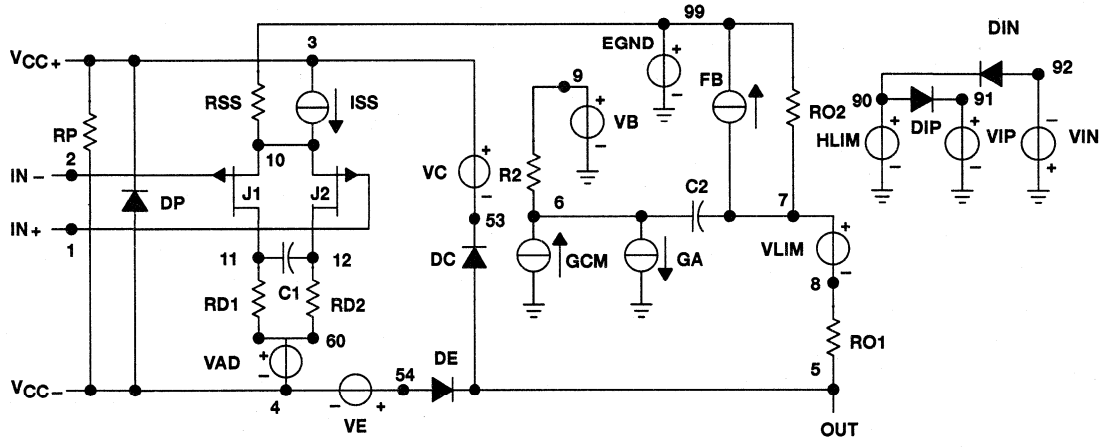
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel and subcircuit in Figure 56 are generated using the TLV2262 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLV2262 1 2 3 4 5
C1      11    12    5.004E–12
C2      6     7     20.00E–12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 5.89E6 –10E6 10E6 10E6 –10E6
GA      6     0     11    12 62.83E–6
GCM     0     6     10    99 22.34E–9
ISS     3     10    DC 11.00E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    15.92E3
RD2     60    12    15.92E3
R01     8     5     135
R02     7     99    135
RP      3     4     15.87E3
RSS     10    99    18.18E6
VAD     60    4     –.5
VB      9     0     DC 0
VC      3     53    DC .6
VE      54    4     DC .6
VLIM    7     8     DC 0
VLP     91    0     DC 0
VLN     0     92    DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=717.8E–6
+ VTO=–.04)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 1 mA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C**
- **Wide Supply Voltage Range 2.7 V to 8 V**
- **Macromodel Included**

description

The TLV2264 and TLV2264A are quad operational amplifiers manufactured using Texas Instruments Advanced LinCMOS™ process. These devices are optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with μpower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that these amplifiers exhibit rail-to-rail output swing. Figure 1 graphically depicts the high-level output voltage for different levels of output current for a 3-V single supply. The output dynamic range can be extended using the TLV2264 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0 to 2-V common-mode input voltage range for a 3-V supply. Furthermore, at 200 μA (typical) of supply current per amplifier, the TLV2264 family can achieve input offset voltage levels as low as 950 μV outperforming existing CMOS amplifiers. The Advanced LinCMOS™ process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input-impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

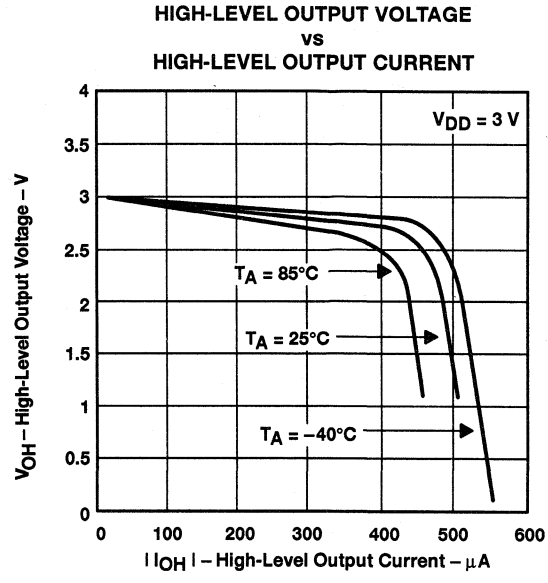


Figure 1

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
−40°C to 85°C	950 μV	TLV2264AID	TLV2264AIN	TLV2264AIPWLE	TLV2264Y
	2.5 mV	TLV2264ID	TLV2264IN	—	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2264IDR).
The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

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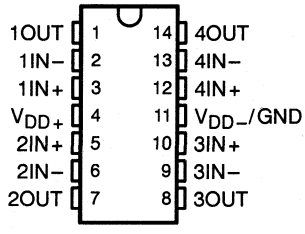
description (continued)

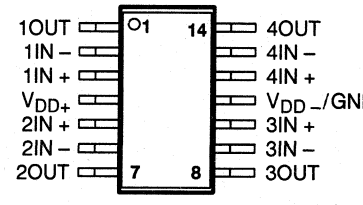
The TLV2264 and TLV2264A, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power-dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes these devices great choices when interfacing directly to analog-to-digital converters (ADCs). All of these features, combined with its temperature performance make the TLV2264 family ideal for remote pressure sensors, temperature control, active VR sensors, accelerometers, hand-held metering, and many other applications.

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.

D OR N PACKAGE
(TOP VIEW)



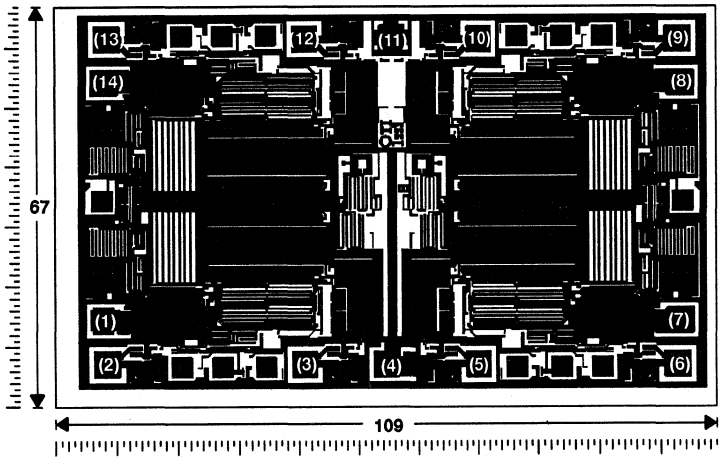
PW PACKAGE
(TOP VIEW)

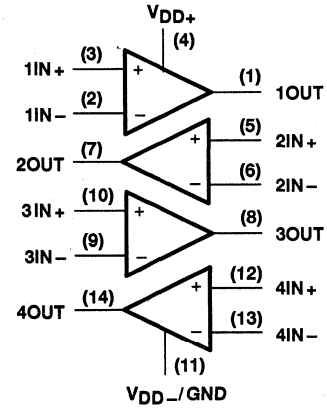


TLV2264Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2264. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

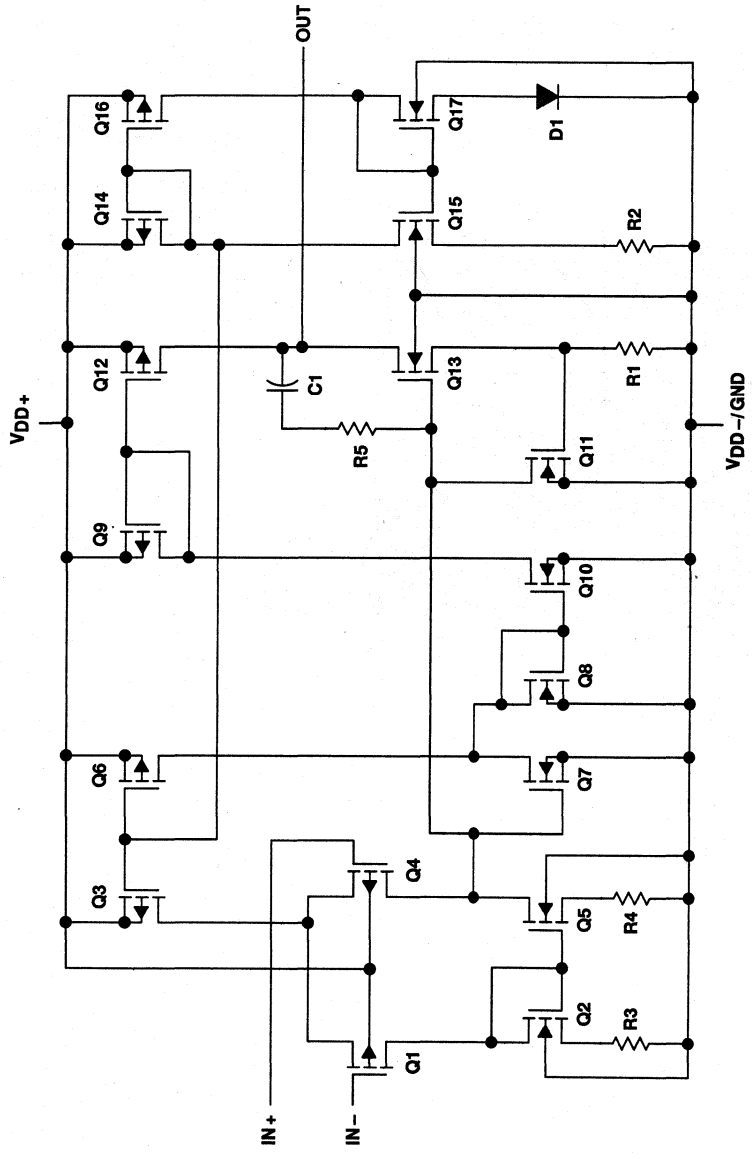
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF THE CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	76
Diodes	18
Resistors	52
Capacitors	6

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) ..... $V_{DD-}-0.3$ V to V_{DD+}
Input current, I_I (each input) ..... ±5 mA
Output current, I_O ..... ±50 mA
Total current into V_{DD+} ..... ±50 mA
Total current out of V_{DD-} ..... ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$ (see Note 1)	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −200 μA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.7 V to 1.7 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		300			300		kHz
t_s	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		61°			61°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −200 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ‡	25°C		550			550		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264			TLV2264A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		14			14		dB

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2264Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0,	R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current					0.5	150	pA
I_{IB}	Input bias current					1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω		0 to 2	−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA				2.99		V
		I_{OH} = −200 μA			2.7	2.75		
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 50 μA			10		mV
		V_{IC} = 0,	I_{OL} = 500 μA			100		
		V_{IC} = 0,	I_{OL} = 1 mA			200		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 50 kΩ†		60	100		V/mV
			R_L = 1 MΩ†			100		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz				8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω	65	77		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load	80	100		dB
I_{DD}	Supply current (four amplifiers)	V_O = 0,	No load			0.8	1	mA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2264Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω		300	2500	μV
I_{IO}	Input offset current				0.5	150	pA
I_{IB}	Input bias current				1	150	pA
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV,	R_S = 50 Ω	0 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −20 μA			4.99		V
		I_{OH} = −100 μA		4.85	4.94		
		I_{OH} = −200 μA		4.7	4.85		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA		0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA		0.09	0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA		0.2	0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ†	80	170		V/mV
			R_L = 1 MΩ†		550		
r_{id}	Differential input resistance				10^{12}		Ω
r_i	Common-mode input resistance				10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10		240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V,	V_O = 2.5 V, R_S = 50 Ω	70	83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, No load	V_{IC} = V_{DD}/2,	80	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load		0.8	1	mA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage	2, 3 4, 5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6, 7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_I	Input voltage	vs Supply voltage vs Free-air temperature	9 10
V_{OH}	High-level output voltage	vs High-level output current	11, 14
V_{OL}	Low-level output voltage	vs Low-level output current	12, 13, 15
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	16
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	17 18
V_{ID}	Differential input voltage	vs Output voltage	19, 20
A_{VD}	Differential voltage amplification	vs Load resistance vs Frequency vs Free-air temperature	21 22, 23 24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	28 29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	30, 31 32
I_{DD}	Supply current	vs Free-air temperature	33
SR	Slew rate	vs Load capacitance vs Free-air temperature	34 35
V_O	Large-signal pulse response	vs Time	36, 37, 38, 39
V_O	Small-signal pulse response	vs Time	40, 41, 42, 43
V_n	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage (referred to input)	Over a 10-second period	46
	Integrated noise voltage	vs Frequency	47
THD + N	Total harmonic distortion plus noise	vs Frequency	48
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	49 50
ϕ_m	Phase margin	vs Frequency vs Load capacitance	22, 23 51
	Gain margin	vs Load capacitance	52
B_1	Unity-gain bandwidth	vs Load capacitance	53
	Overestimation of phase margin	vs Load capacitance	54

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

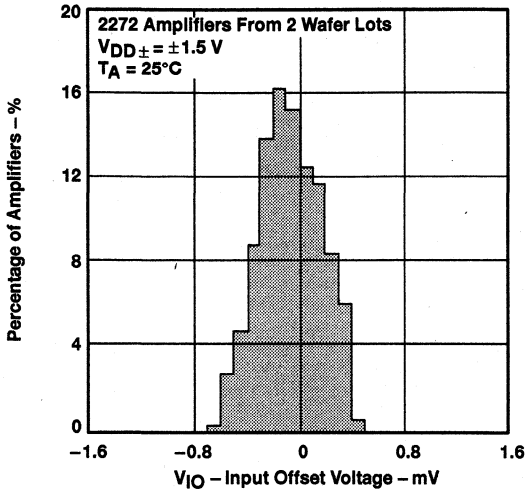


Figure 2

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

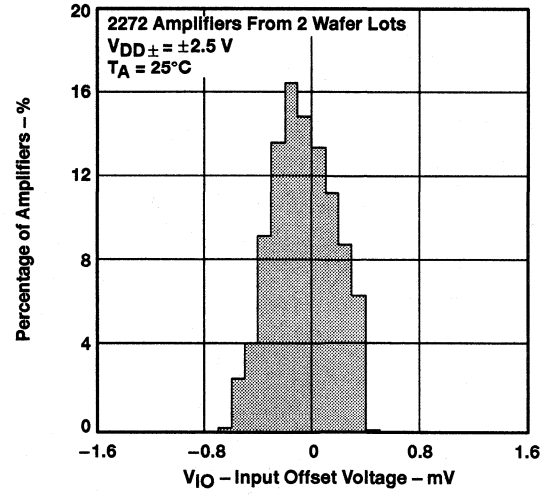


Figure 3

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

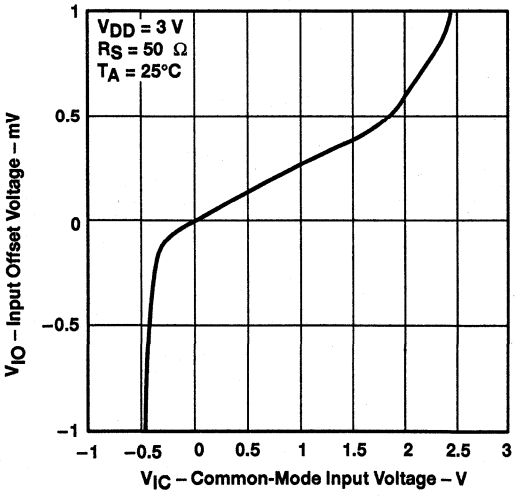


Figure 4

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

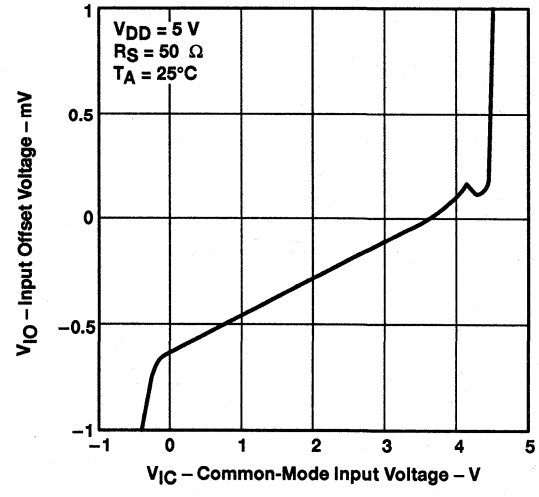


Figure 5

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

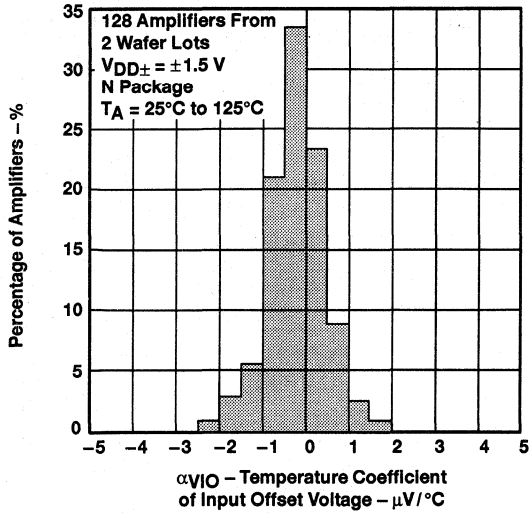


Figure 6

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

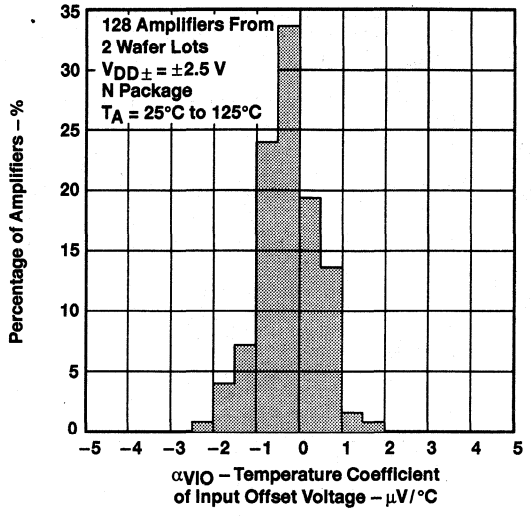


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

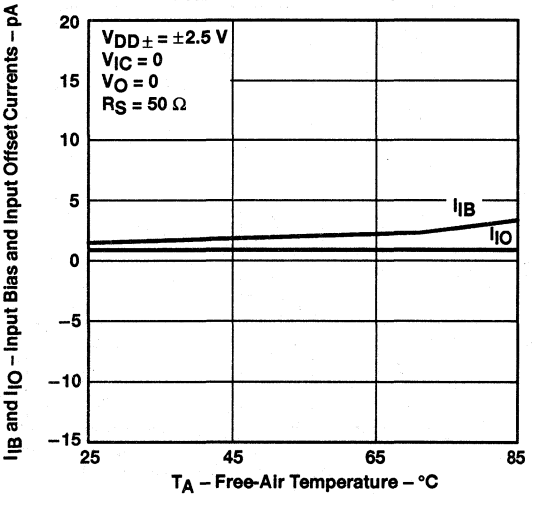


Figure 8

INPUT VOLTAGE vs SUPPLY VOLTAGE

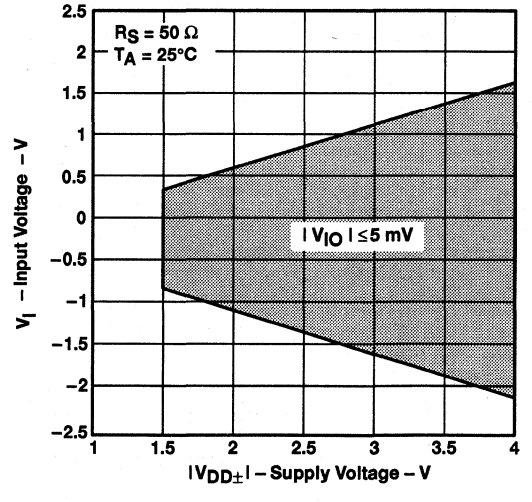


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†‡

INPUT VOLTAGE vs FREE-AIR TEMPERATURE

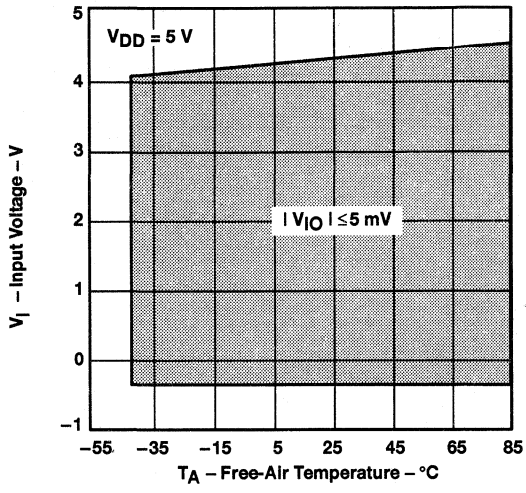


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

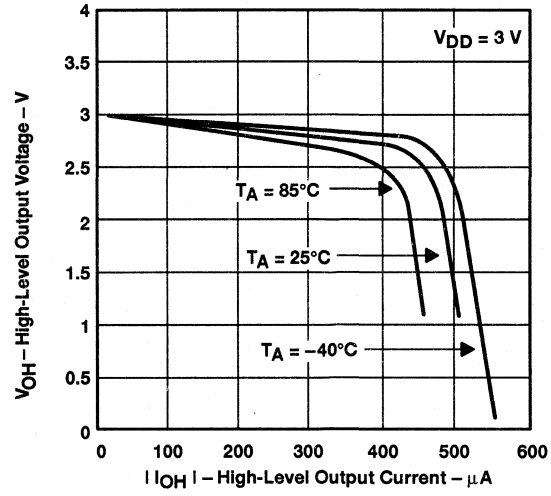


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

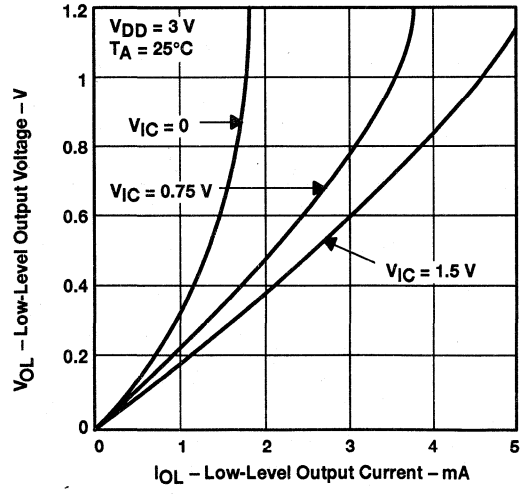


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

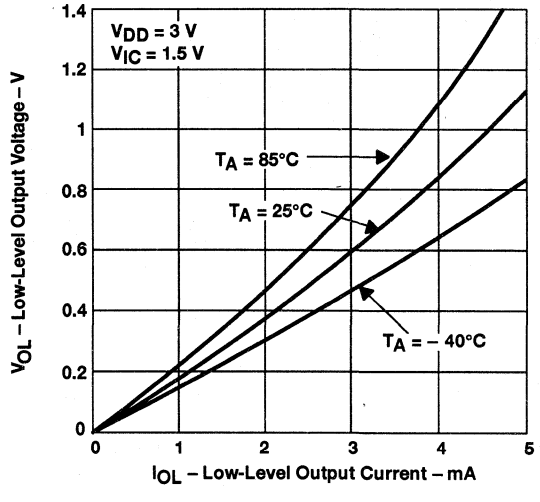


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

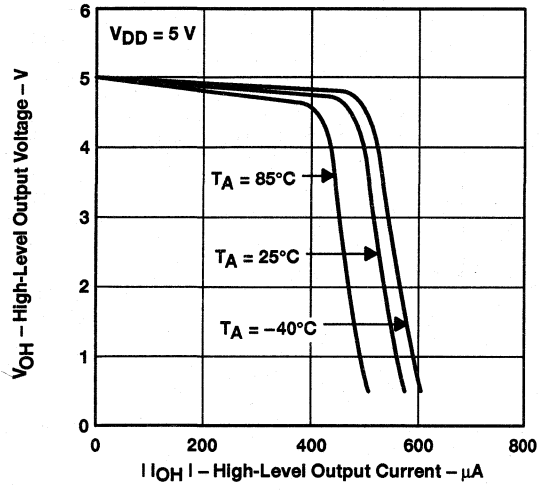


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

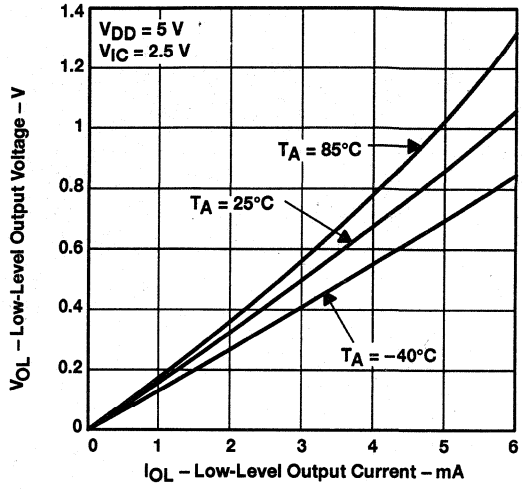


Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

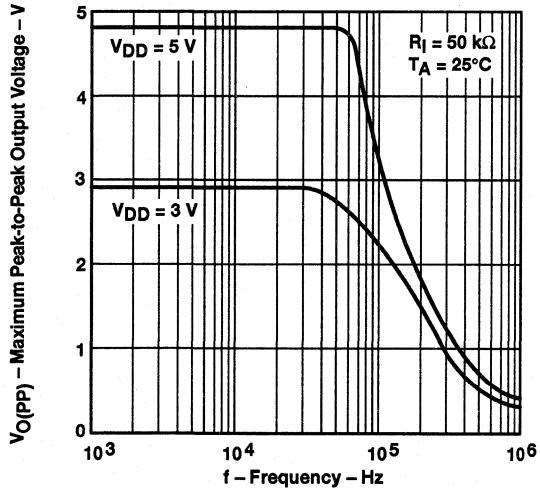


Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

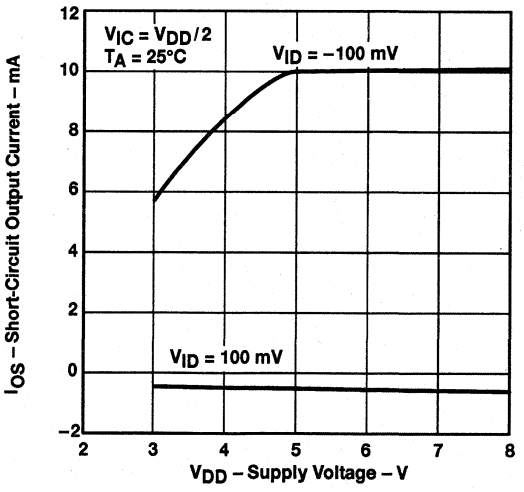


Figure 17

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

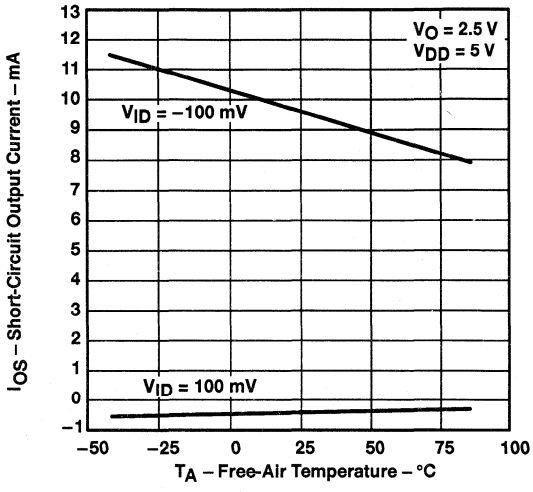


Figure 18

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

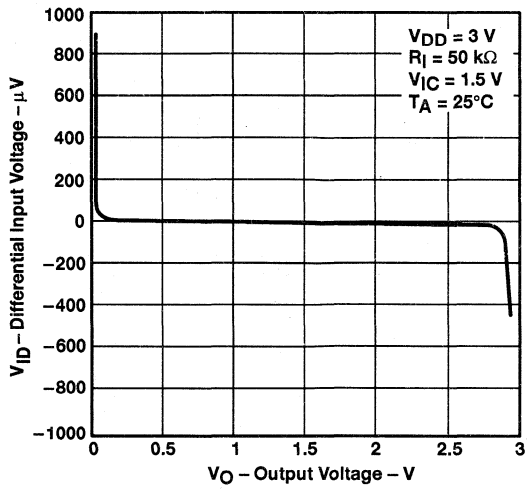


Figure 19

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

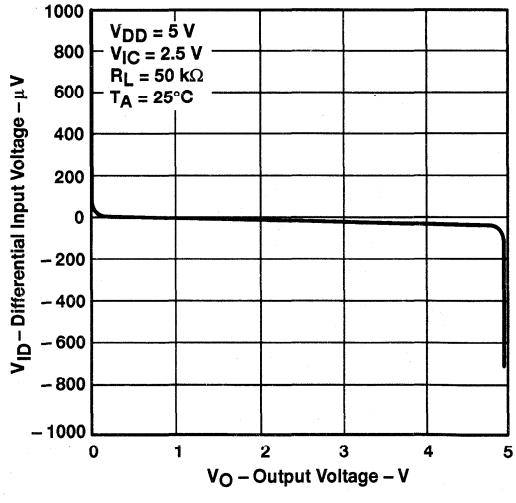


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

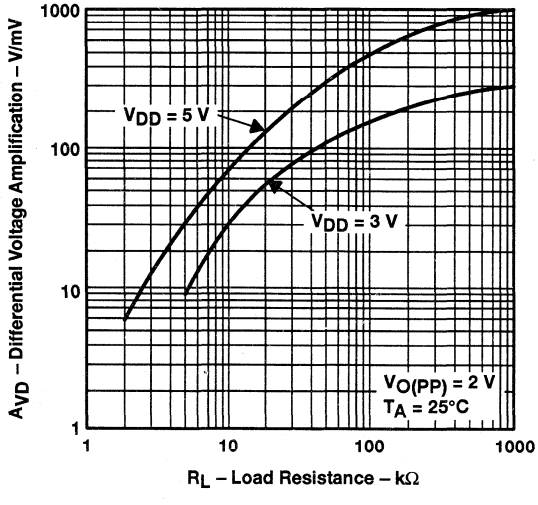


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

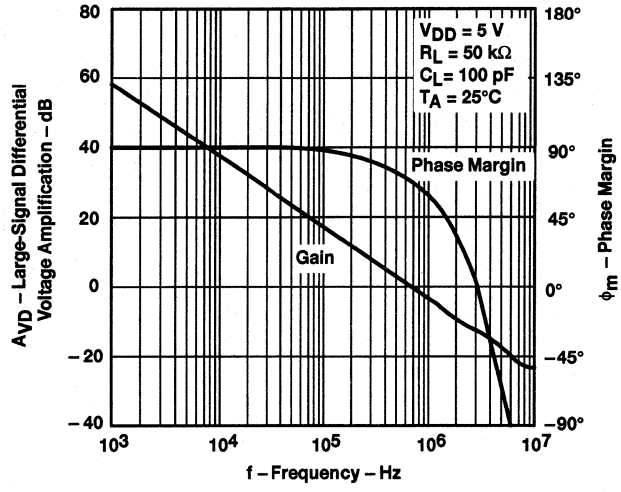


Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

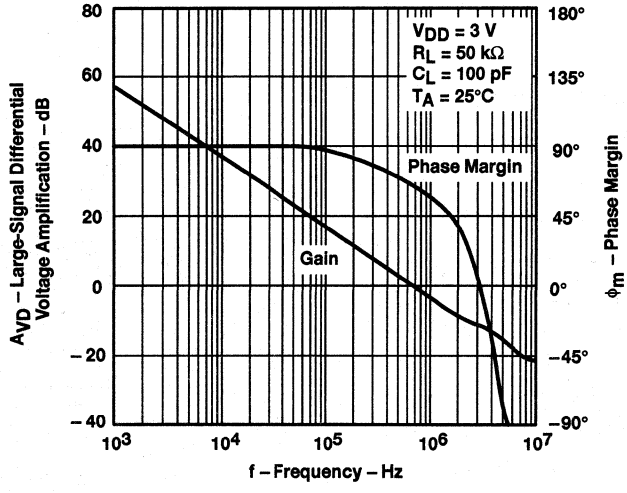


Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

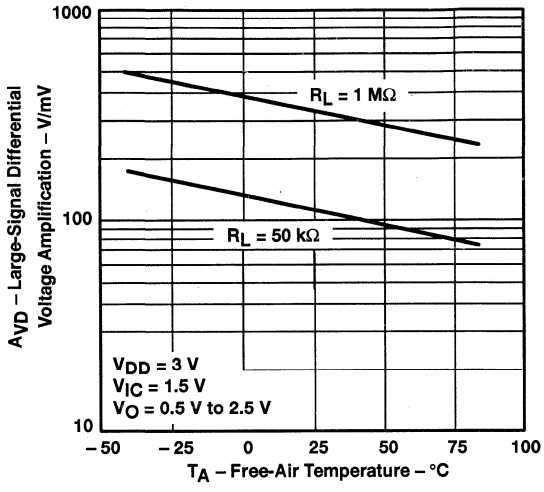


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

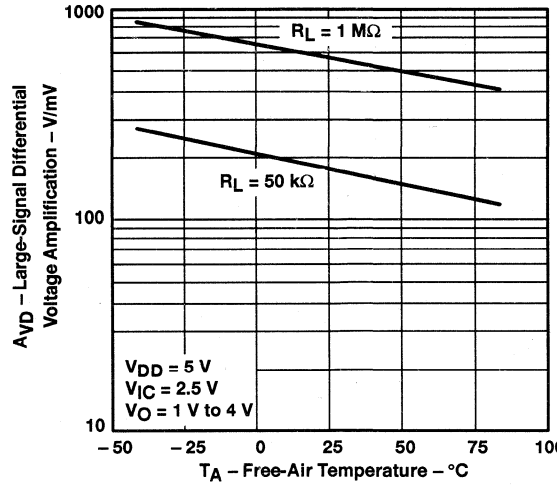


Figure 25

OUTPUT IMPEDANCE vs FREQUENCY

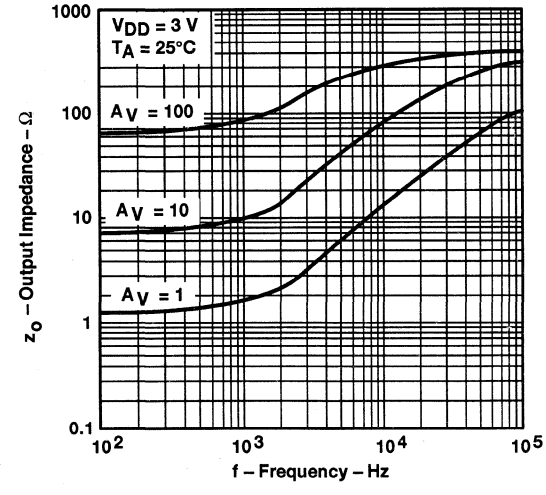


Figure 26

OUTPUT IMPEDANCE vs FREQUENCY

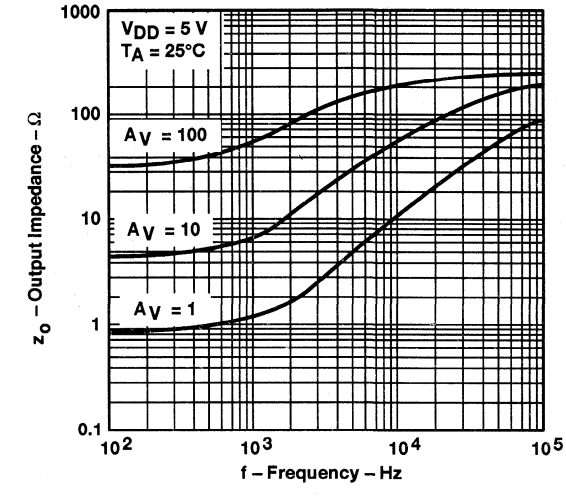


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

COMMON-MODE REJECTION RATIO vs FREQUENCY

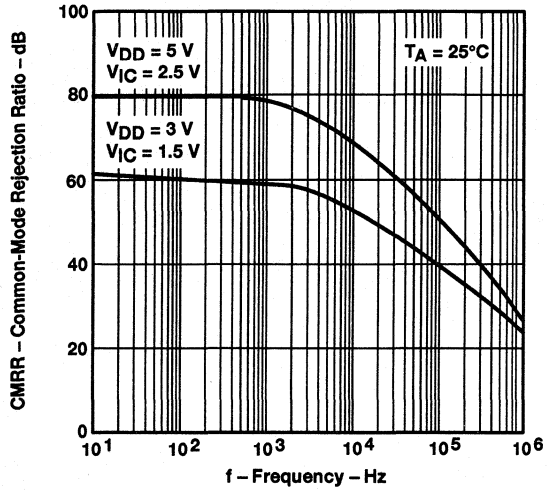


Figure 28

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

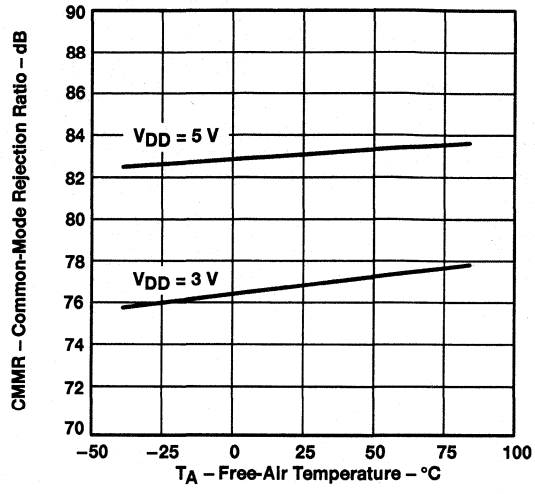


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

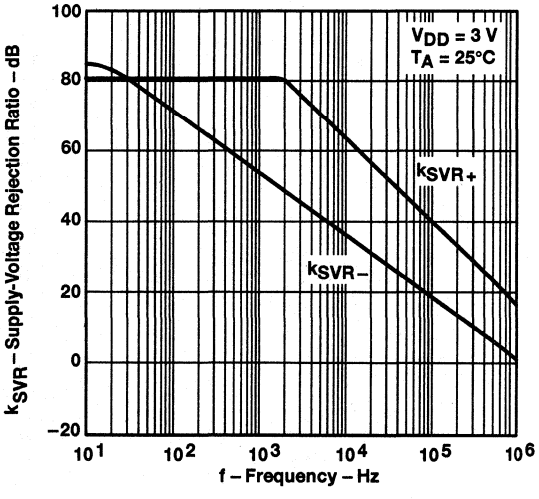


Figure 30

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

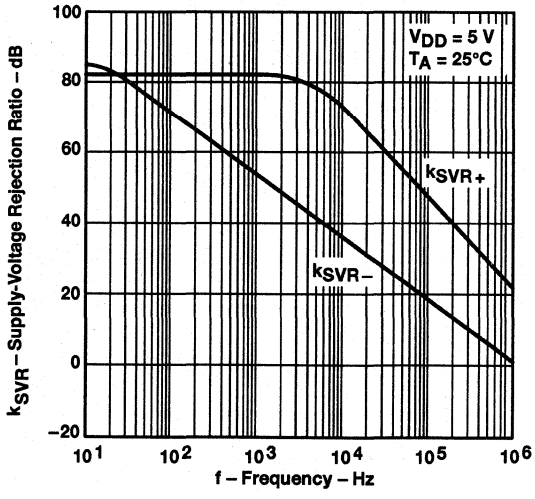


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

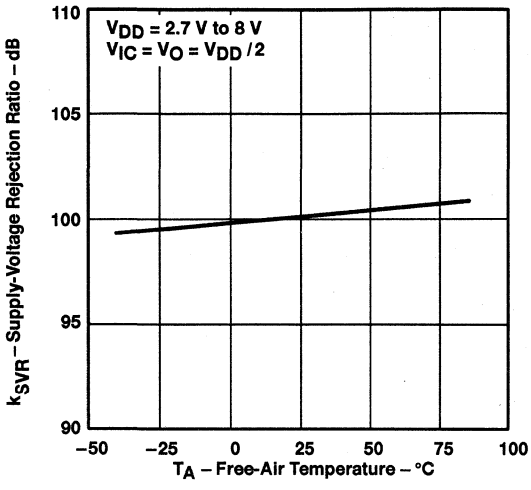


Figure 32

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

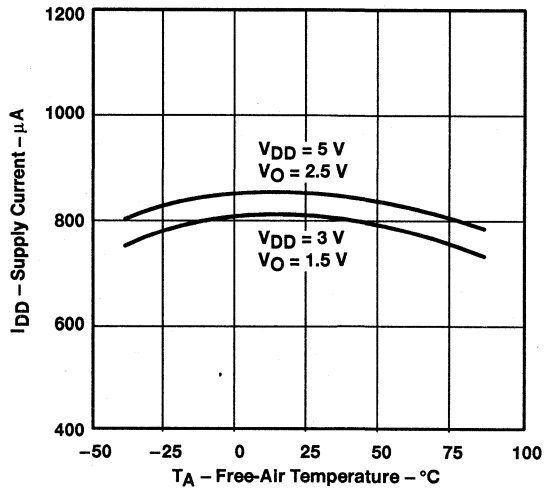


Figure 33

SLEW RATE vs LOAD CAPACITANCE

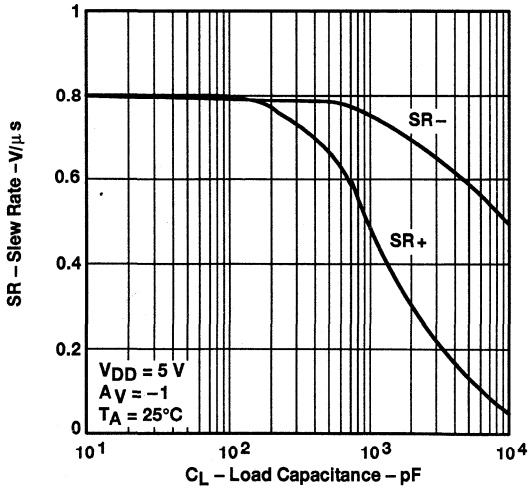


Figure 34

SLEW RATE vs FREE-AIR TEMPERATURE

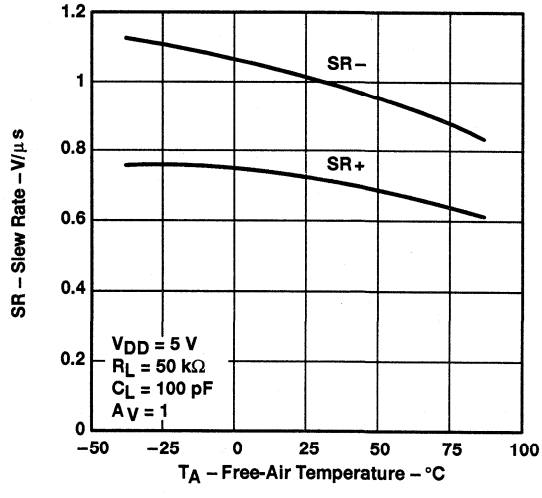


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING LARGE-SIGNAL PULSE RESPONSE

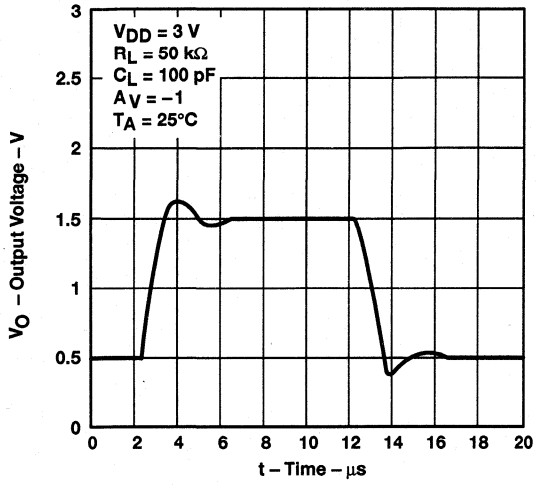


Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE

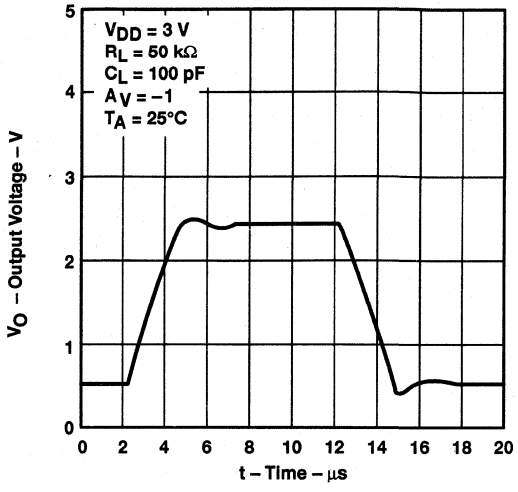


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

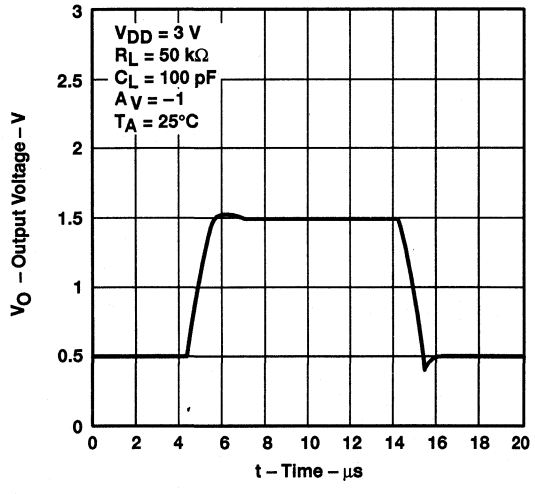


Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

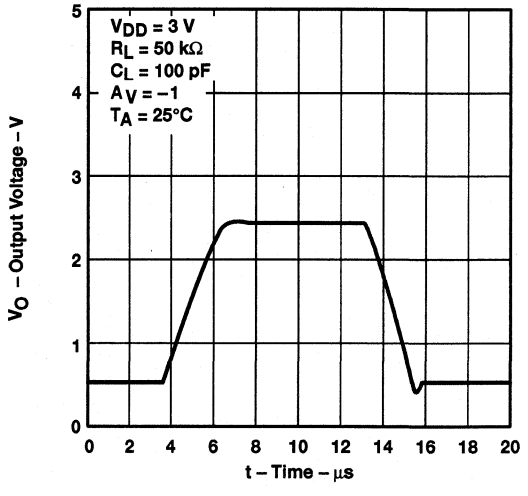


Figure 39

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

INVERTING SMALL-SIGNAL
PULSE RESPONSE

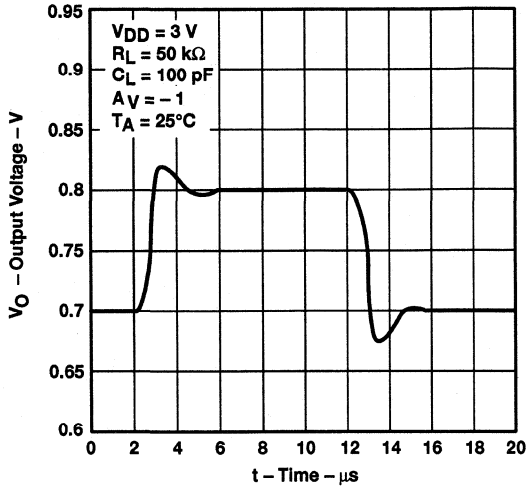


Figure 40

INVERTING SMALL-SIGNAL
PULSE RESPONSE

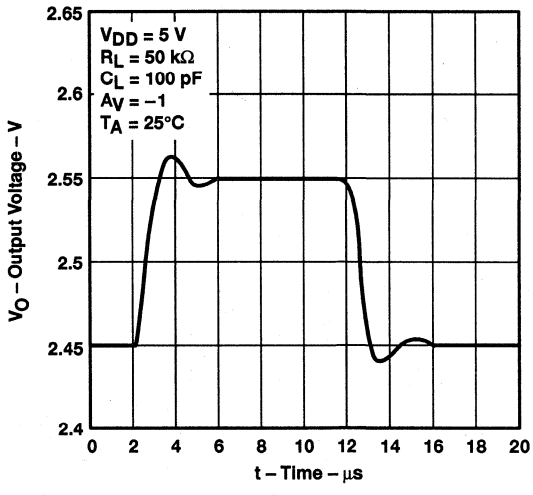


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

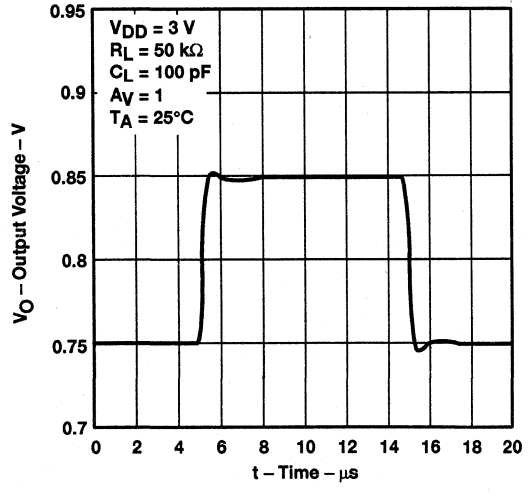


Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

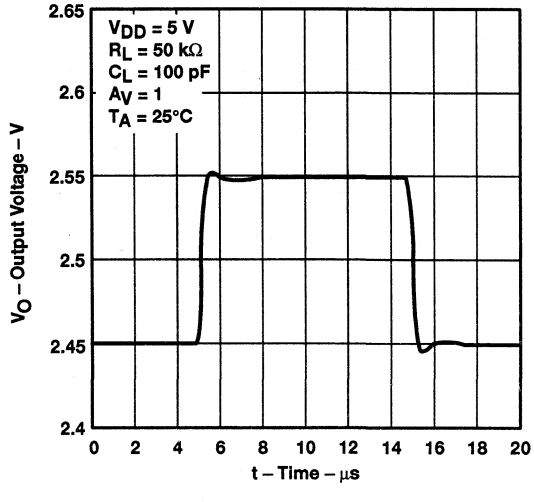


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

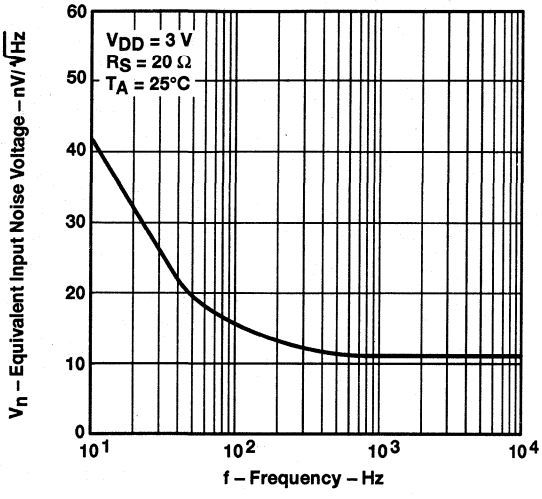


Figure 44

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

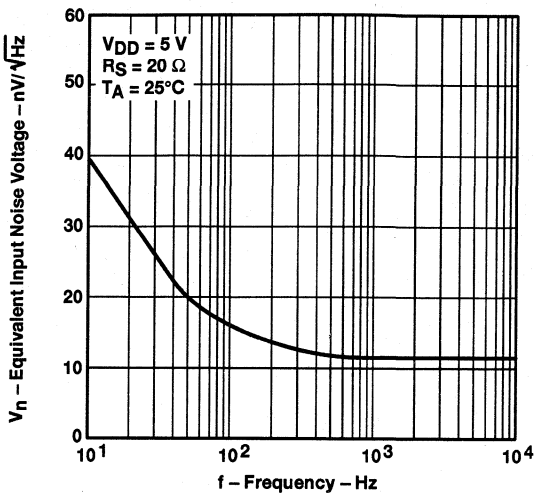


Figure 45

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD

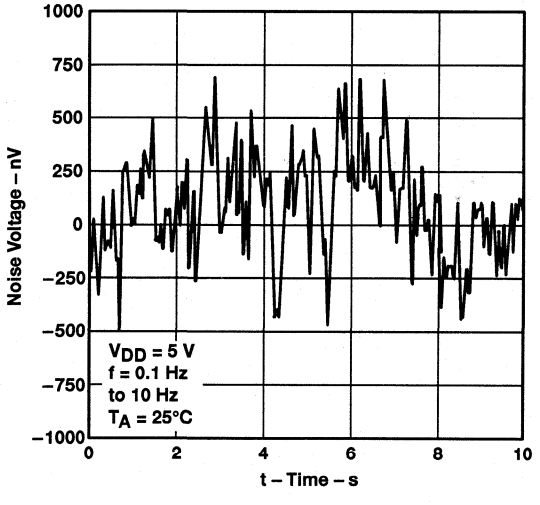


Figure 46

INTEGRATED NOISE VOLTAGE
vs
FREQUENCY

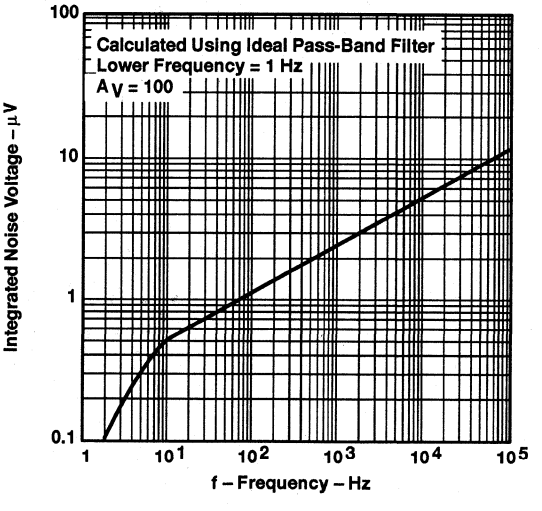


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS†‡

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

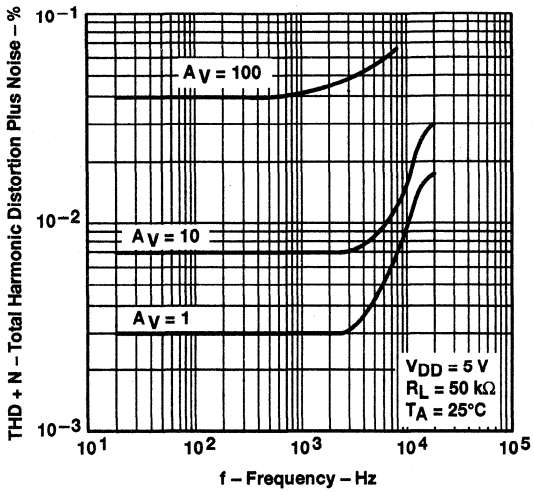


Figure 48

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

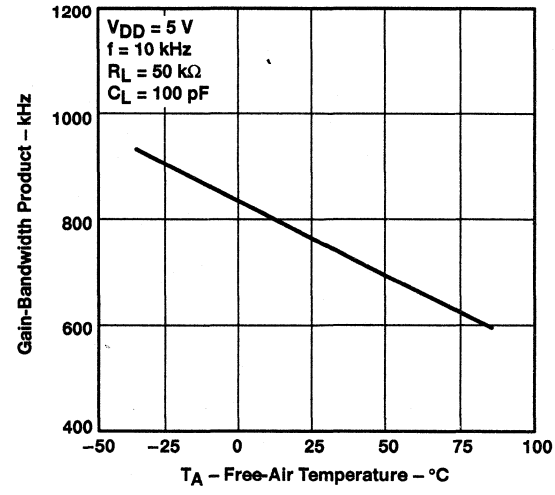


Figure 49

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

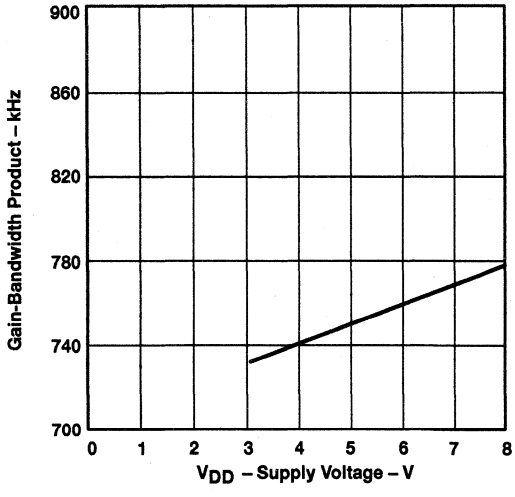


Figure 50

PHASE MARGIN
vs
LOAD CAPACITANCE

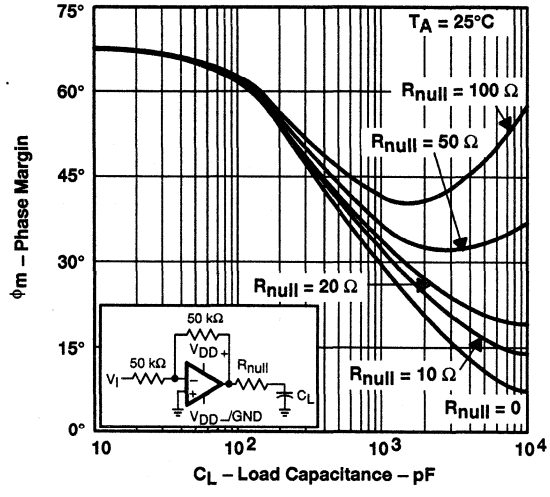


Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN MARGIN
vs
LOAD CAPACITANCE

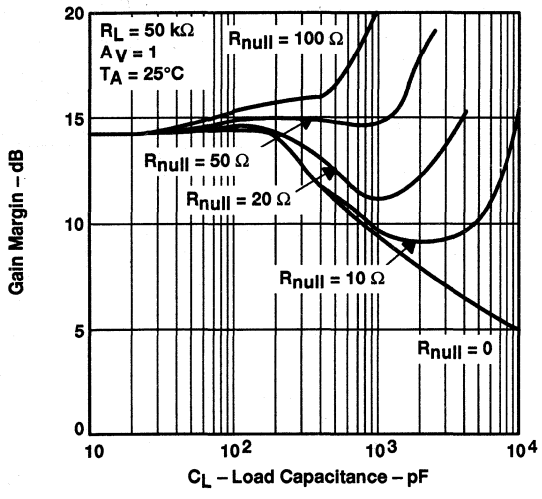


Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

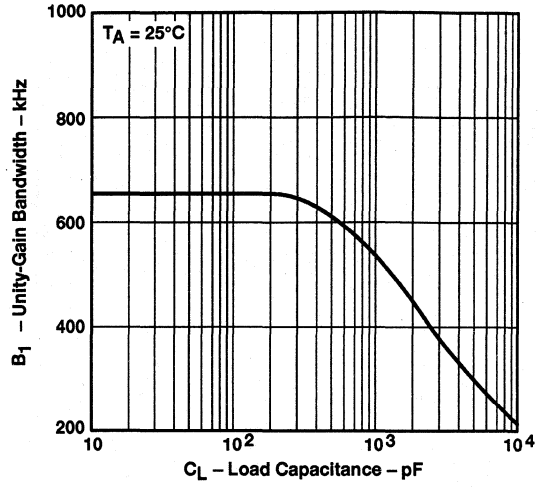
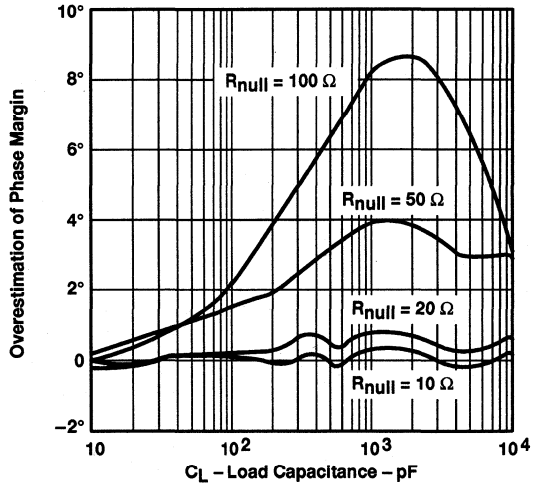


Figure 53

OVERESTIMATION OF PHASE MARGIN†
vs
LOAD CAPACITANCE



† See application information

Figure 54

APPLICATION INFORMATION

loading considerations

The TLV2264 is a low-voltage, low-power version of the TLC2274 with the appropriate design changes relative to the lower power level. The output drive performance to the negative rail for the TLV2264 is similar to the TLC2274 and is capable of driving several milliamperes.

The design topology used for the TLV2264 or the TLC2274 limits the drive to the positive rail to a value very close to the I_{DD} for the amplifier. While the TLC2274 is capable of greater than 1-mA drive from the positive rail, the TLV2264 is capable of only a few hundred microamperes. When designing with lower impedance loads (less than 50 kΩ) with the TLV2264, the lower drive capability to the positive rail needs to be taken into consideration. Although the TLV2264 topology provides lower drive to the positive rail than other high-output-drive rail-to-rail operational amplifiers, it is a more stable topology.

driving large capacitive loads

The TLV2264 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

where :

$\Delta\theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation (1), UGBW must be approximated from Figure 53.

Using equation (1) alone overestimates the improvement in phase margin, as illustrated in Figure 54. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation (2).

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

where :

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

APPLICATION INFORMATION

driving large capacitive loads (continued)

For the TLV2264, the pole associated with the load is typically 6 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 60 MHz, at C_L = 1000 pF, use 600 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone [equation (1)]. Equation (3) approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation (1) to better approximate the improvement in phase margin.

$$\Delta\theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \quad (3)$$

where :

$\Delta\theta_{m2}$ = reduction in phase margin
UGBW = unity-gain bandwidth frequency
F = factor from equation (2)
P_2 = unadjusted pole (60 MHz @ 10 pF, 6 MHz @100 pF, etc.)

Using these equations with Figure 54 and Figure 55 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

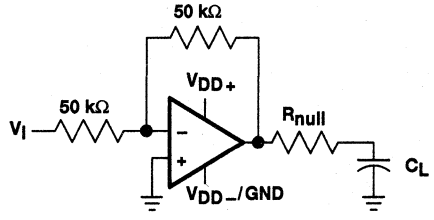


Figure 55. Series-Resistance Circuit

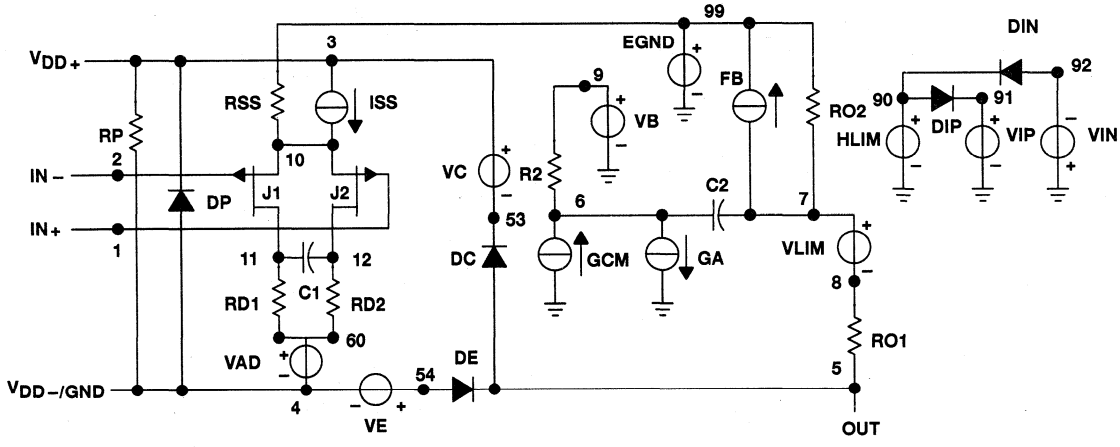
APPLICATION INFORMATION

macromodel information

Macromodel information provided is derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel and subcircuit in Figure 56 are generated using the TLV2264 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



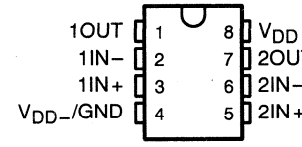

```
.SUBCKT TLV2264 1 2 3 4 5
C1      11    12    1.372E–12
C2      6     7     10.00E–12
DC      5     53    DX
DE      54    5     DX
DLP     90    91    DX
DLN     92    90    DX
DP      4     3     DX
EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB      7     99    POLY (5) VB VC VE VLP
+ VLN 0 19.79E6 –40E6 40E6 40E6 –40E6
GA      6     0     11    12 21.05E–6
GCM     0     6     10    99 7.486E–9
ISS     3     10    DC 5.500E–6
HLIM    90    0     VLIM 1K
J1      11    2     10 JX
J2      12    1     10 JX
R2      6     9     100.0E3
RD1     60    11    47.51E3
RD2     60    12    47.51E3
R01     8     5     120
R02     7     99    120
RP      3     4     15.42E3
RSS     10    99    36.36E6
VAD     60    4     –.6
VB      9     0     DC 0
VC      3     53    DC .58
VE      54    4     DC .58
VLIM    7     8     DC 0
VLP     91    0     DC 0
VLN     0     92    DC 5.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=161.1E–6
+ VTO=–.09)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

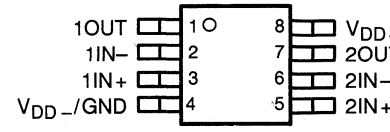
PSpice and *Parts* are trademarks of MicroSim Corporation.

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



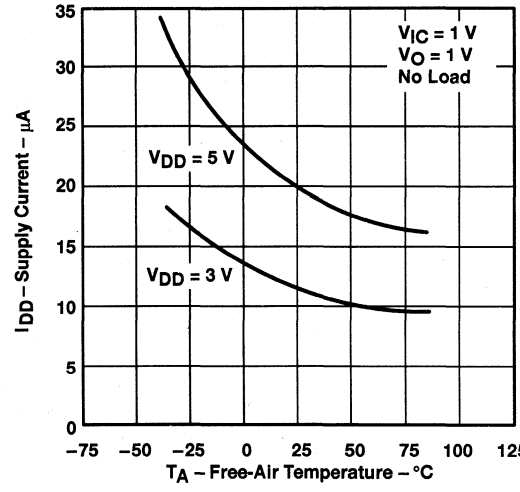
description

The TLV2322 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low-power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier specified at only 27 μA over its full temperature range of –40°C to 85°C.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	9 mV	TLV2322ID	TLV2322IP	TLV2322IPWLE	TLV2322Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2322IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2322IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

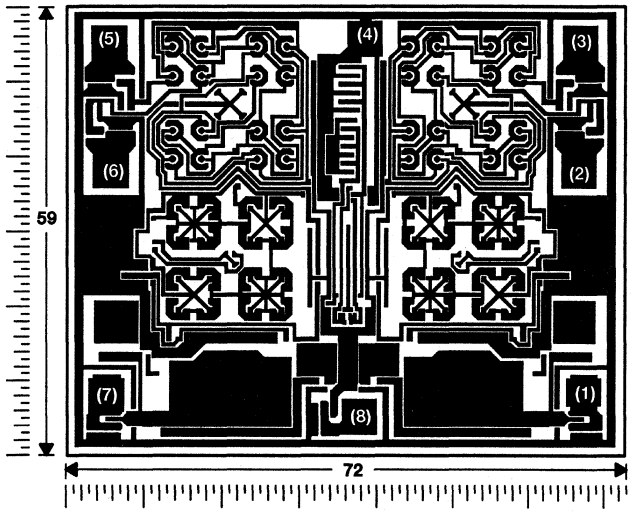
To facilitate the design of small portable equipment, the TLV2322 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

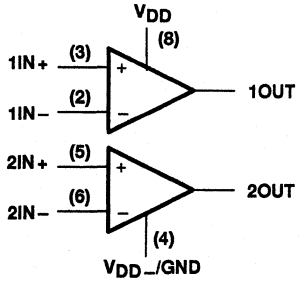
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2322 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD can result in the degradation of the device parametric performance.

TLV2322Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2322I. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

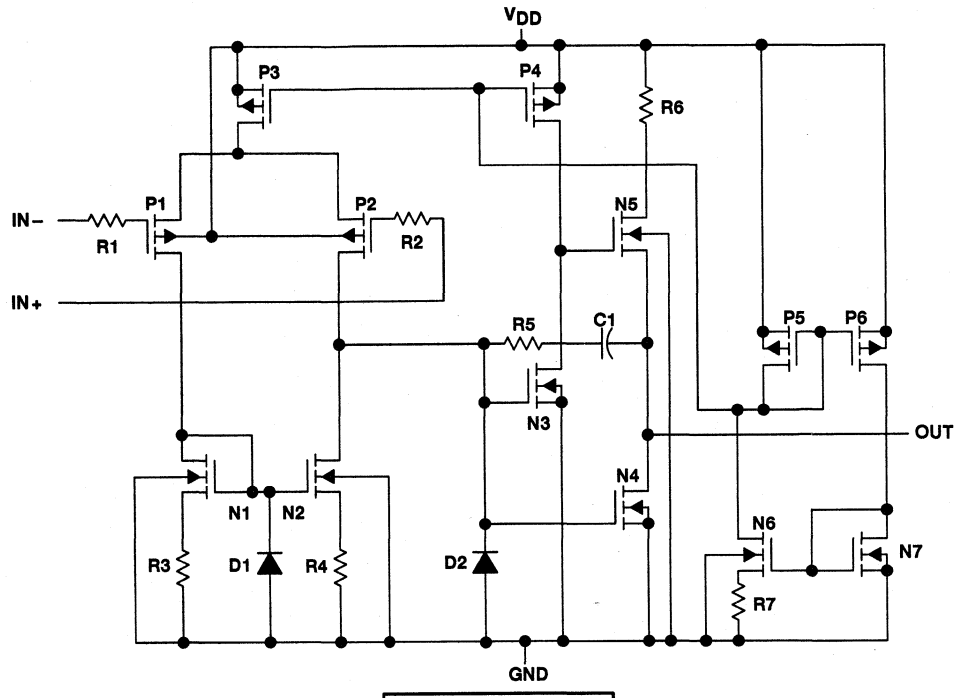
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TLV2322 equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

† Includes both, amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD}\pm$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mV	5.8 mW/°C	377 mW
P	1000 mV	8.0 mW/°C	520 mW
PW	525 mV	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2322						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		12	34		20	34	μA
			Full range			54			54	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f= B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2322Y						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ		1.1	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{ID})	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	86		70	86		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		12	34		20	34	µA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	5 6 7
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	8 9, 11 10 12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature	13 14
I_{IB}	Input bias current	vs Temperature	15
I_{IO}	Input offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage vs Temperature	17 18
SR	Slew rate	vs Supply voltage vs Temperature	19 20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	22 23
A_{VD}	Large-signal differential voltage amplification	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	26 27 28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE**

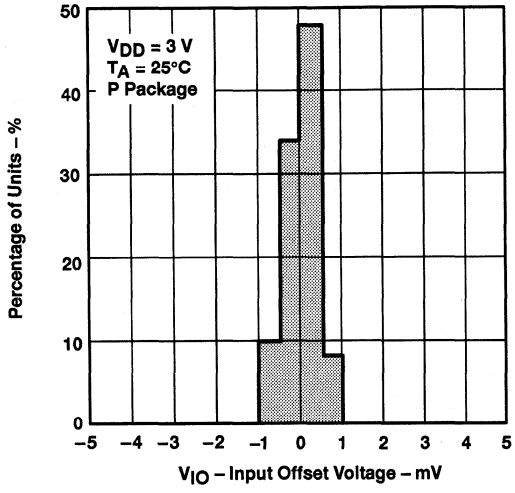


Figure 1

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE**

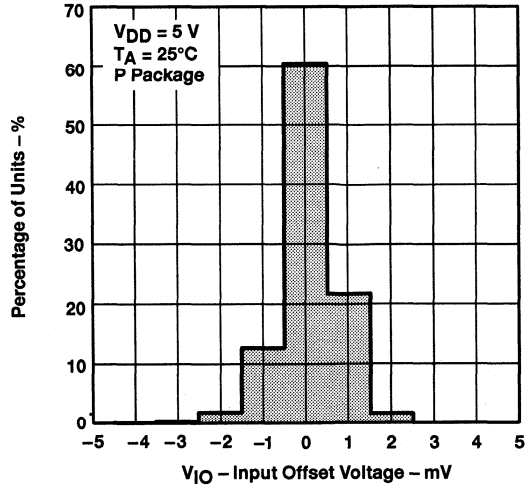


Figure 2

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

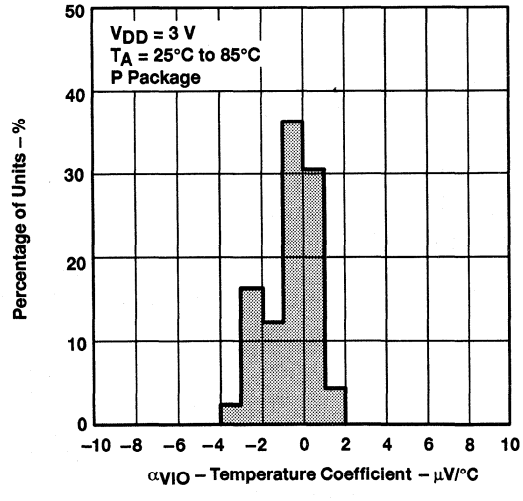


Figure 3

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

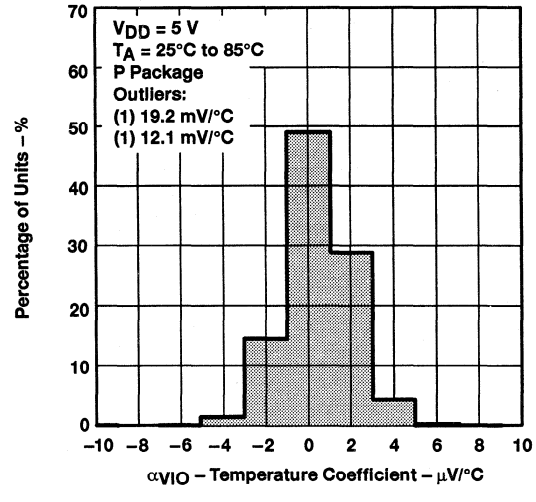


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

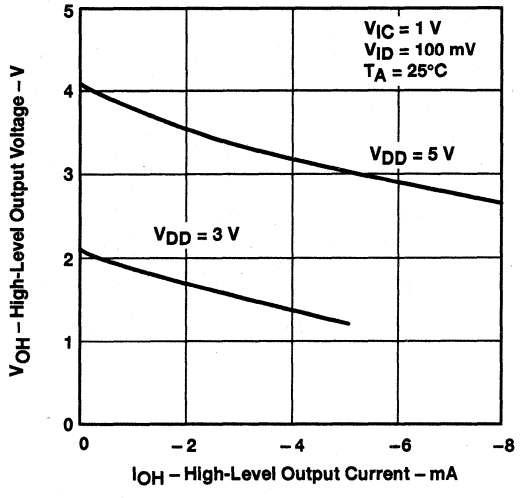


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

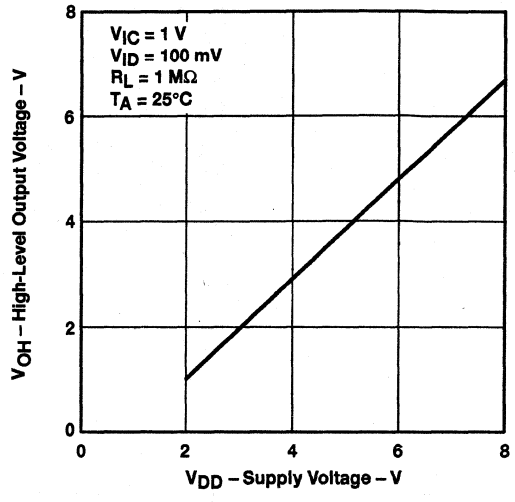


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

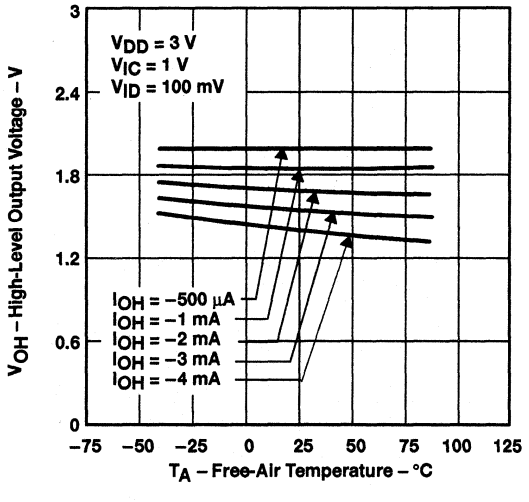


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

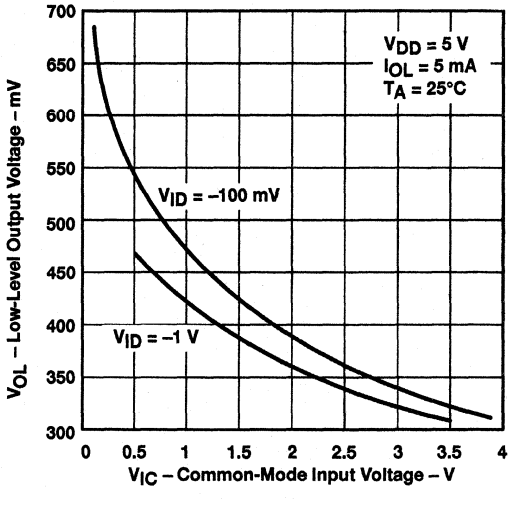


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

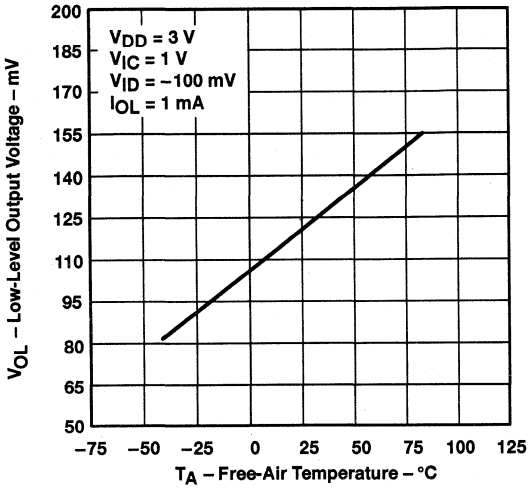


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

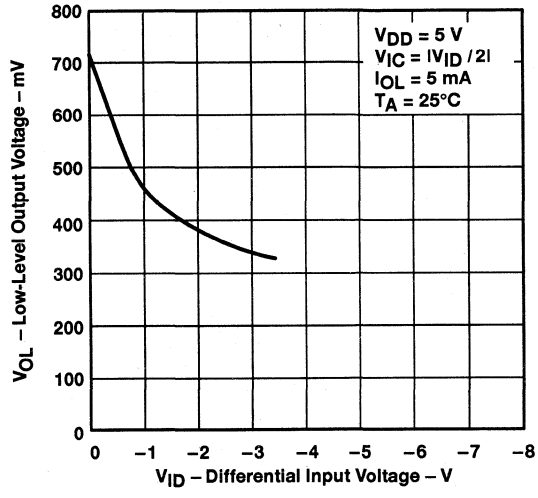


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

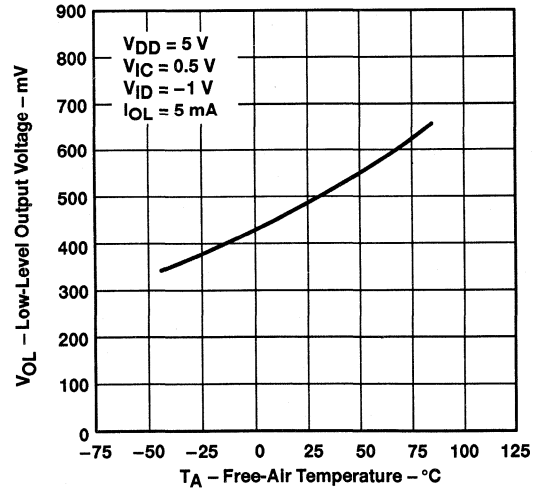


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

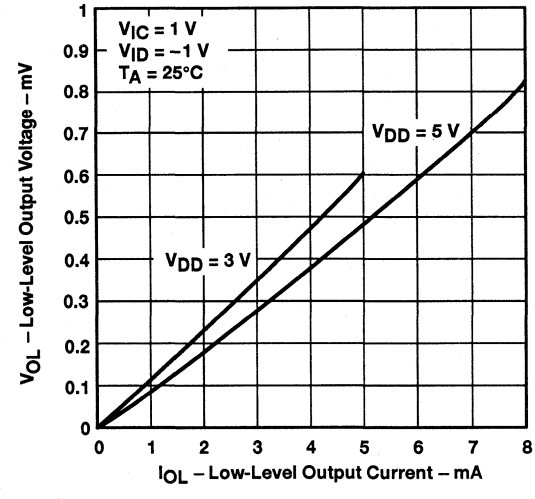


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

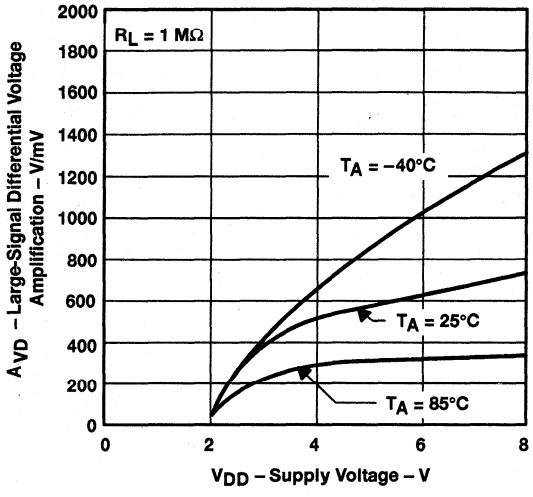


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

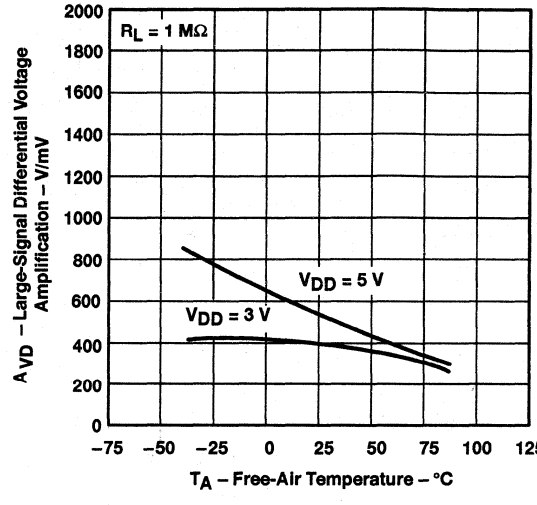
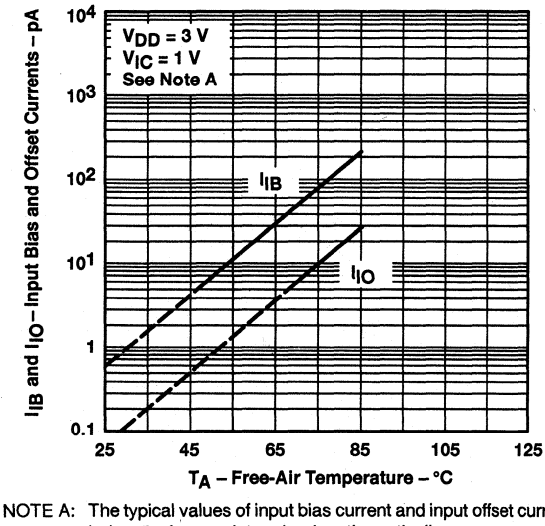


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

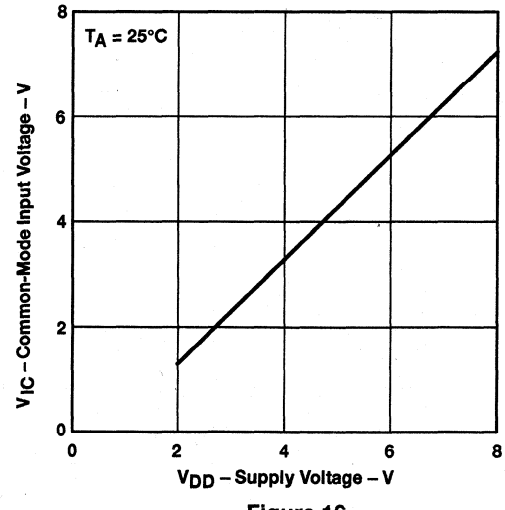


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

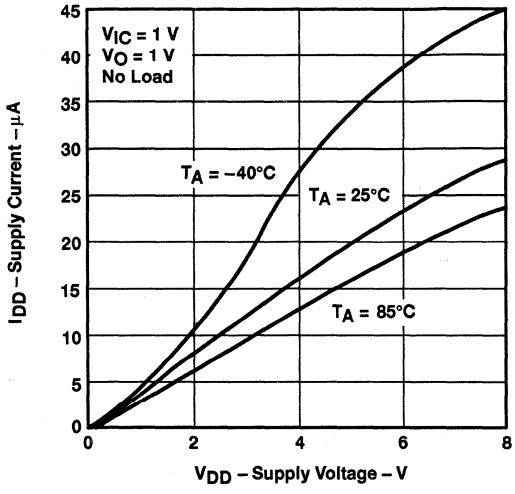


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

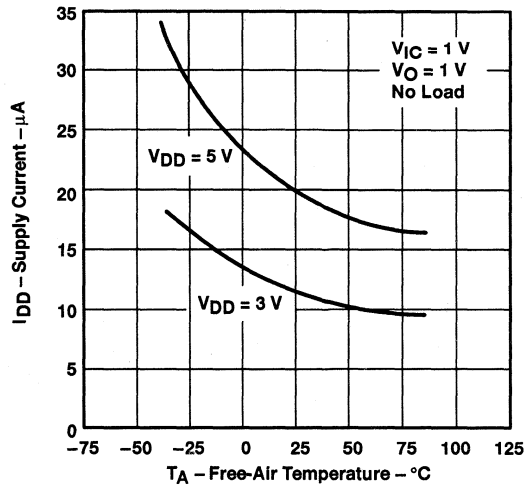


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

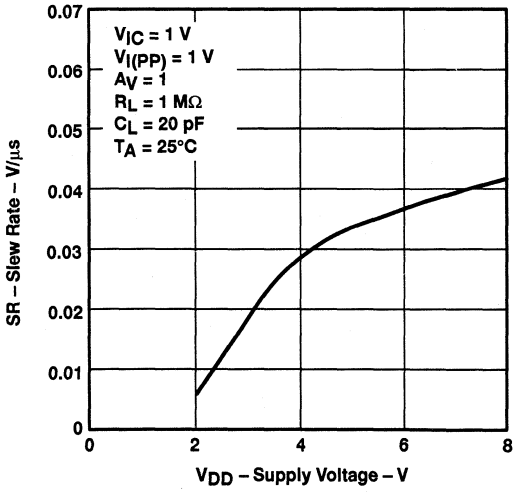


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

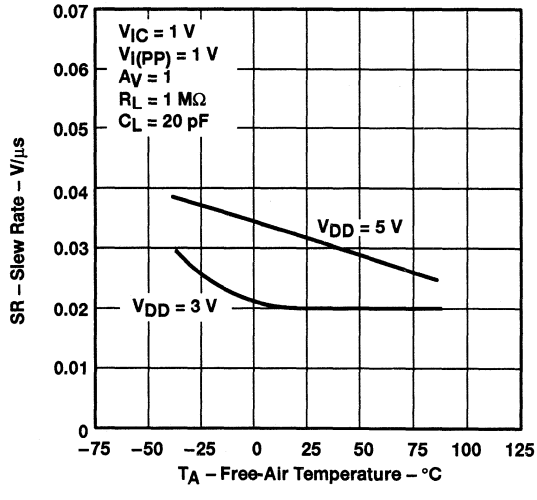


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

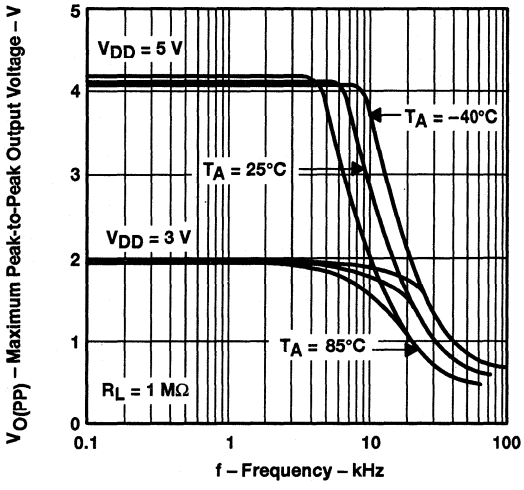


Figure 21

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

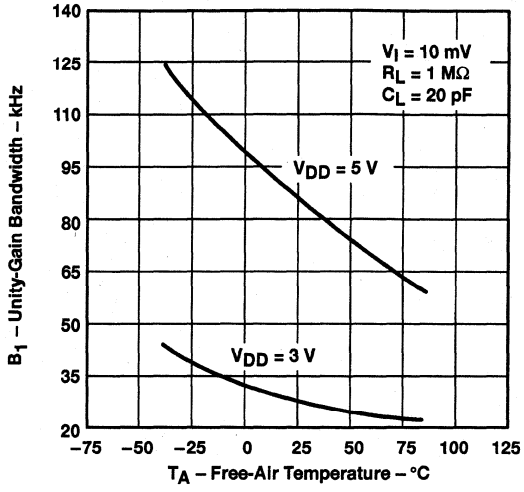


Figure 22

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

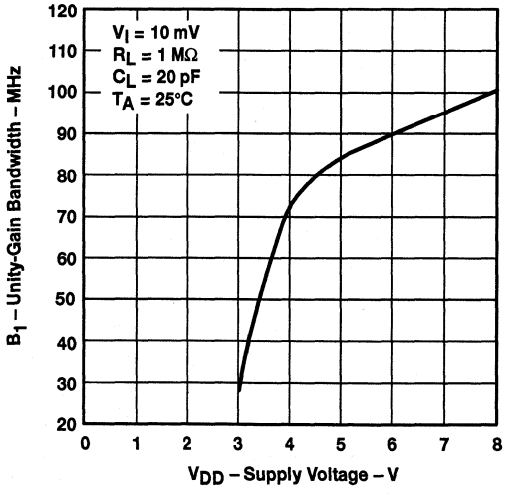


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

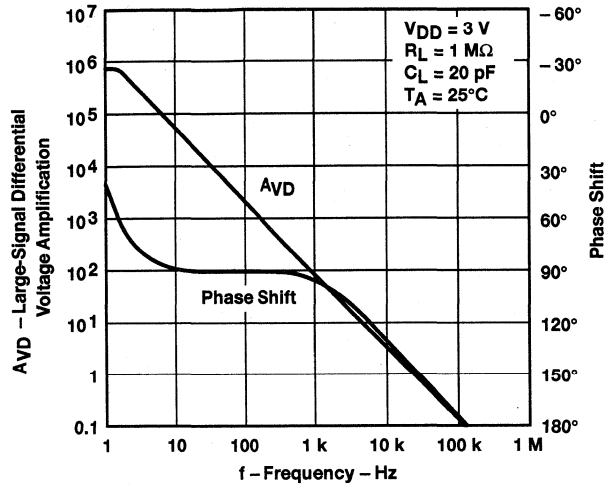


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

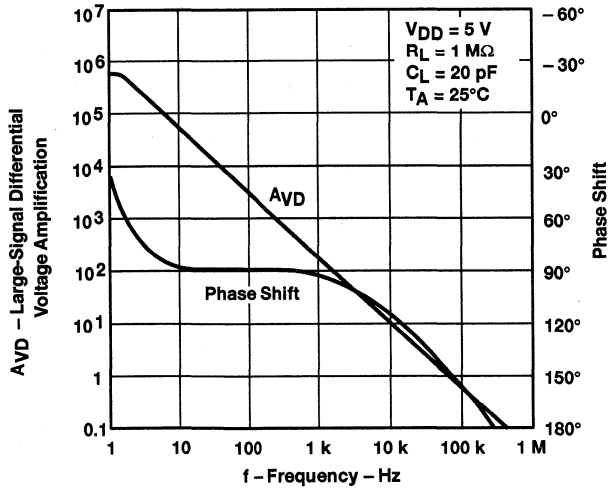


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

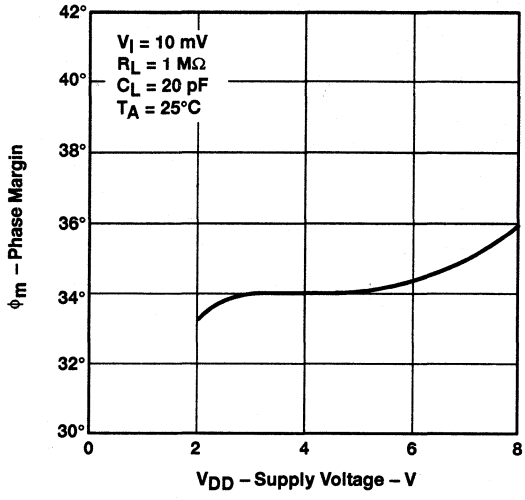


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

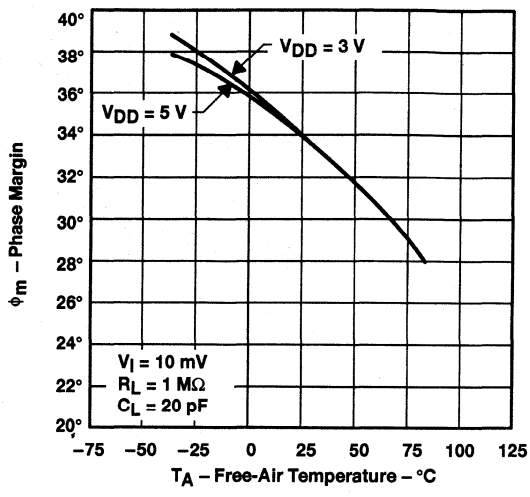


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

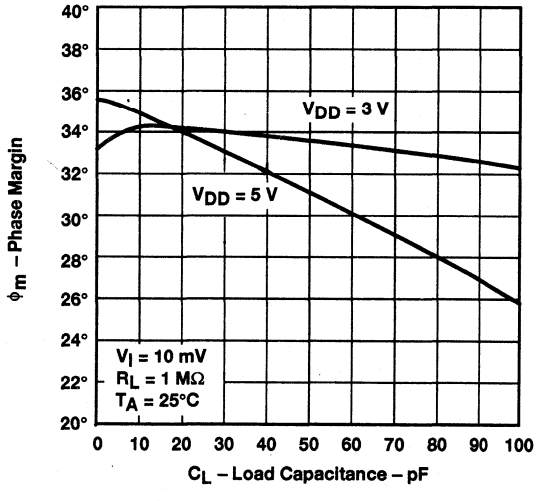


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

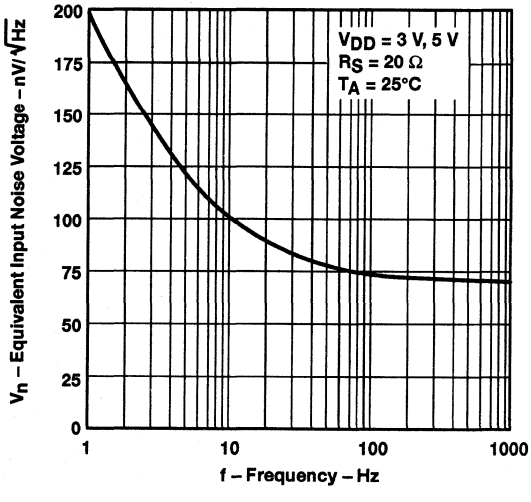


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2322 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

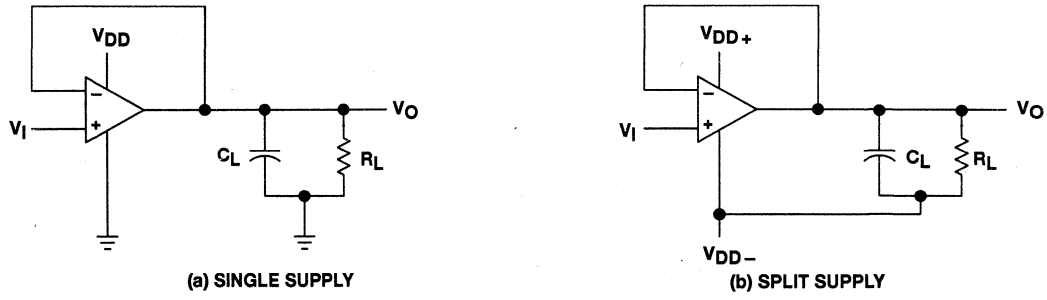


Figure 30. Unity-Gain Amplifier

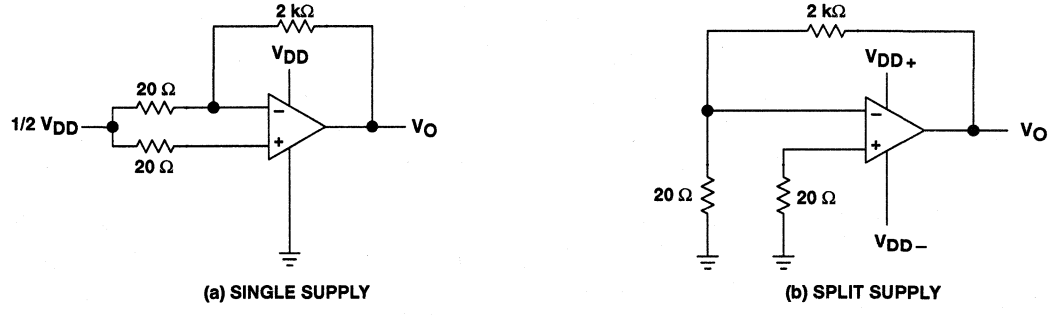


Figure 31. Noise-Test Circuits

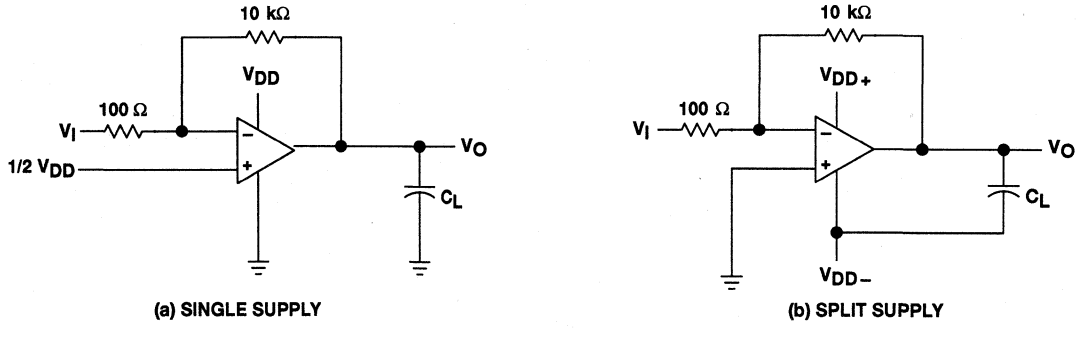


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2322 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

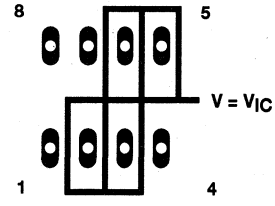


Figure 33. Isolation Metal Around Device Inputs (P package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance that can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

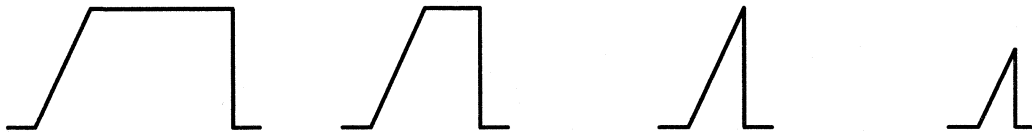


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2322 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

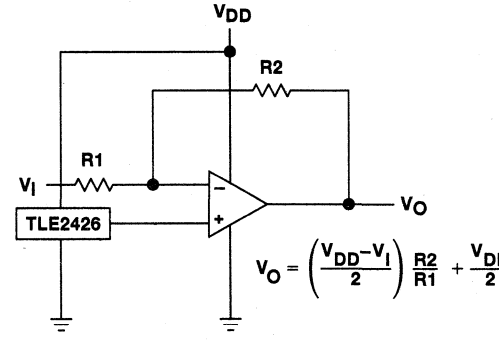


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2322 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

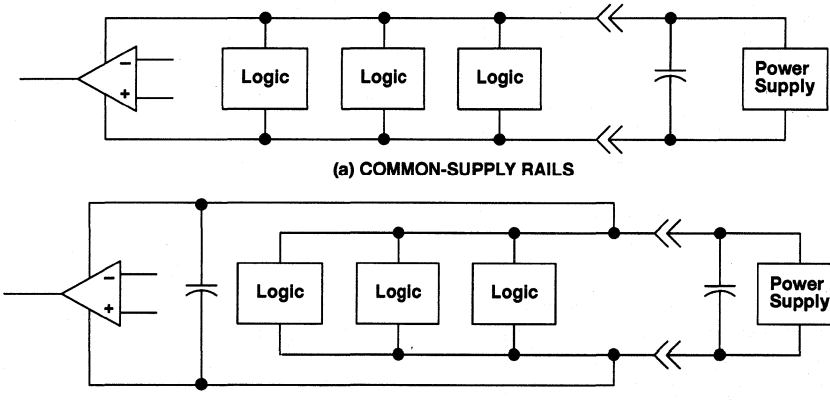


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2322 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

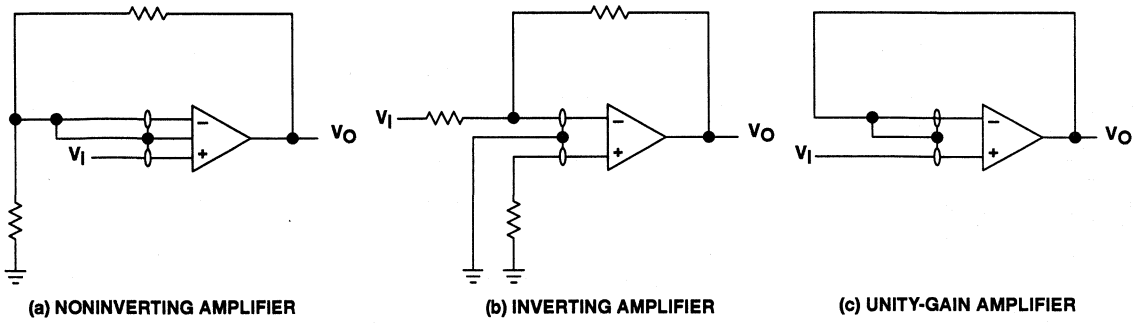
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2322 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2322 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2322 result in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

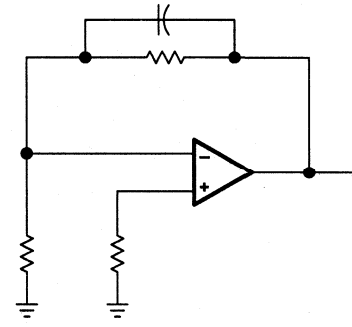


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2322 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD can result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2322 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal-protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage

APPLICATION INFORMATION

by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2322 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2322 possesses excellent high-level output voltage and current capability methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

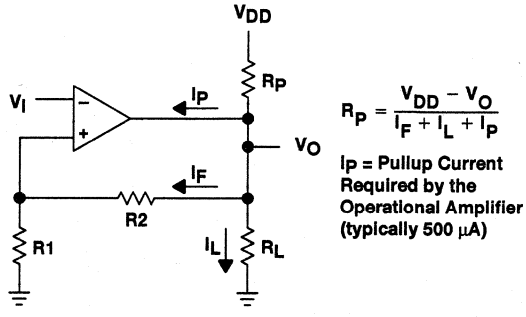


Figure 39. Resistive Pullup to Increase V_{OH}

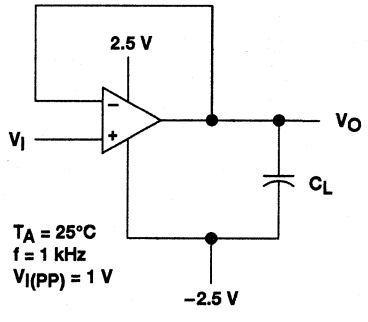
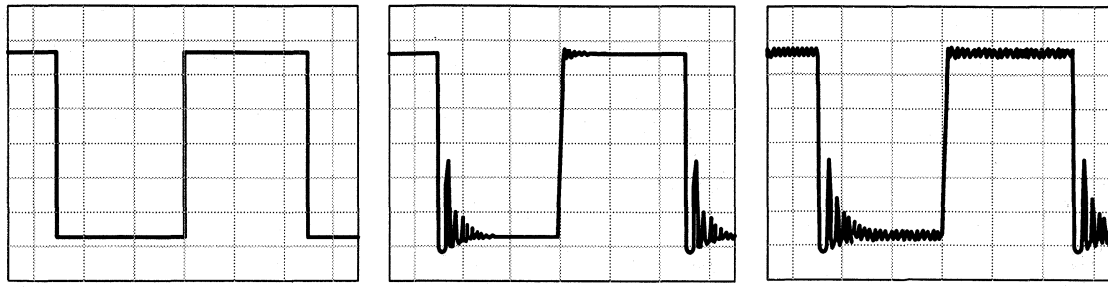


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2322 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

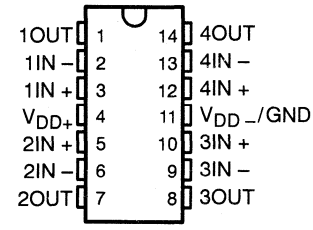
(b) C_L = 260 pF, R_L = NO LOAD

(c) C_L = 310 pF, R_L = NO LOAD

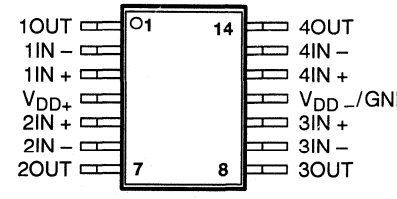
Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and Up to V_{DD} –1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



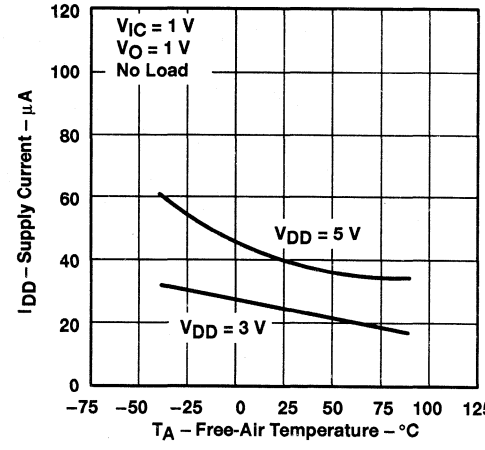
description

The TLV2324 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier is specified at only 27 μA over its full temperature range of –40°C to 85°C.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate, LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making them ideal for interfacing to high-impedance sources such as in sensor circuits or filter applications.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	10 mV	TLV2324ID	TLV2324IN	TLV2324IPWLE	TLV2324Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2324IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2324IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

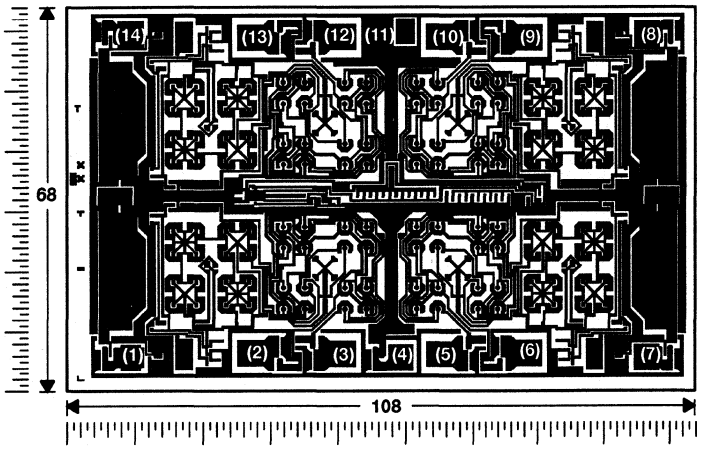
To facilitate the design of small portable equipment, the TLV2324 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline package (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

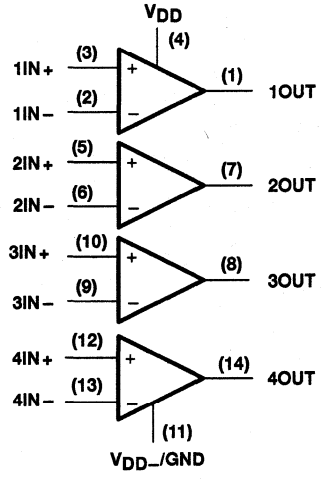
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2324 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2324Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2324. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

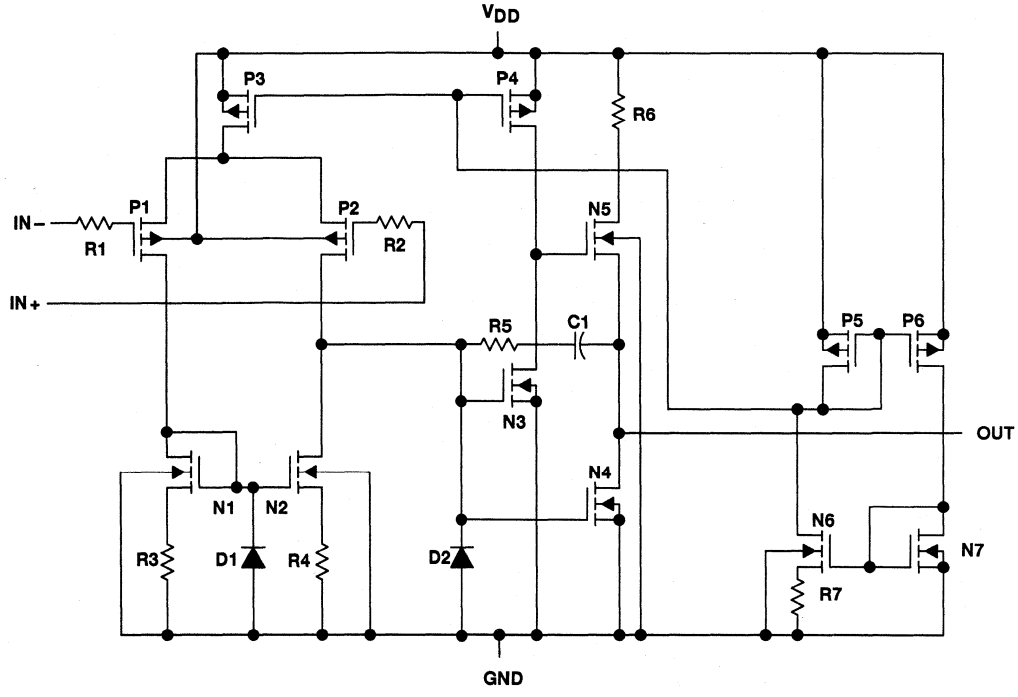
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (12) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	108
Diodes	8
Resistors	28
Capacitors	4

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mV	7.6 mW/°C	494 mW
N	1575 mV	12.6 mW/°C	819 mW
PW	700 mV	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2324I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		24	68		39	68	μA
			Full range			108			108	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$= 1 V	25°C		0.03		V/μs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 30	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 32	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2324Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 1 MΩ		1.1	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = 100 mV,		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 1 MΩ,	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, R_S = 50 Ω	V_{IC} = 1 V,	70	86		70	86		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		24	68		39	68	μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	5 6 7
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	8 9, 11 10 12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature vs Frequency	13 14 24, 25
I_{IB}	Input bias current	vs Temperature	15
I_{IO}	Input offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage vs Temperature	17 18
SR	Slew rate	vs Supply voltage vs Temperature	19 20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	22 23
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	26 27 28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE

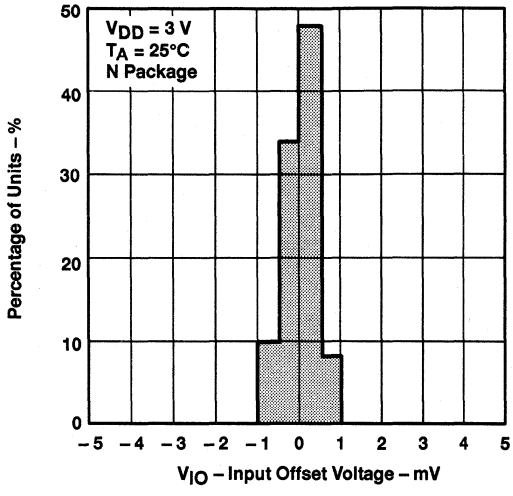


Figure 1

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE

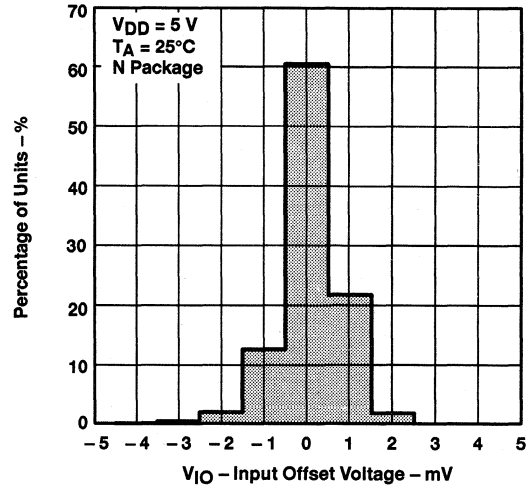


Figure 2

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

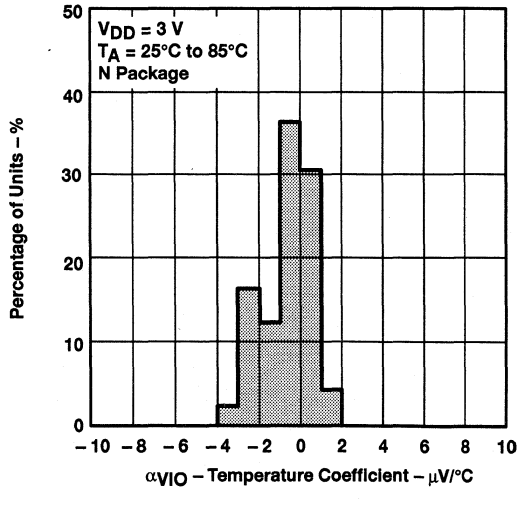


Figure 3

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

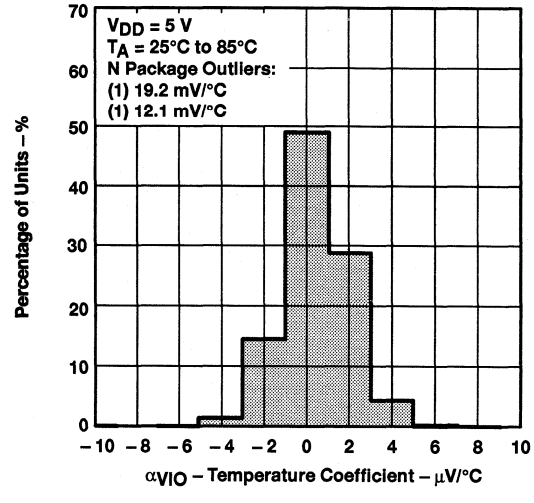


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

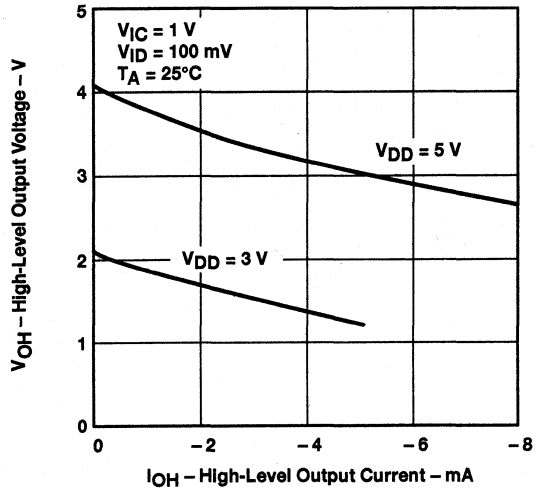


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

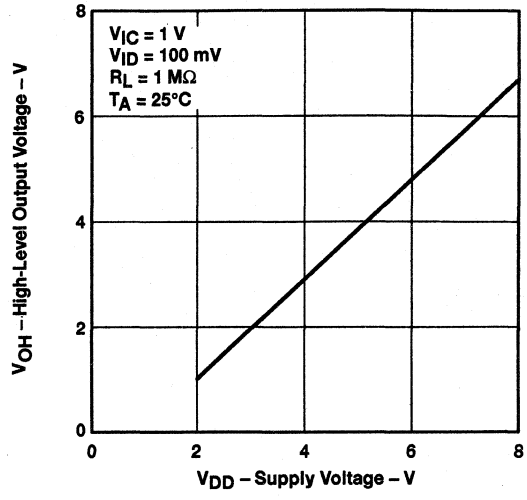


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

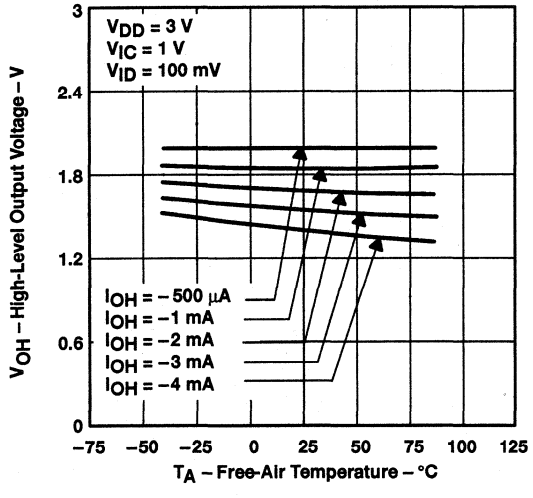


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

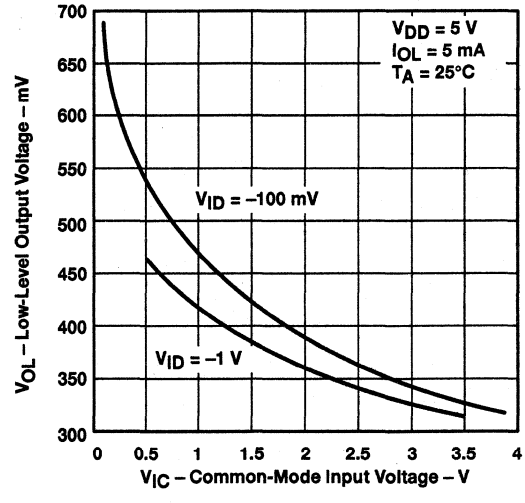


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

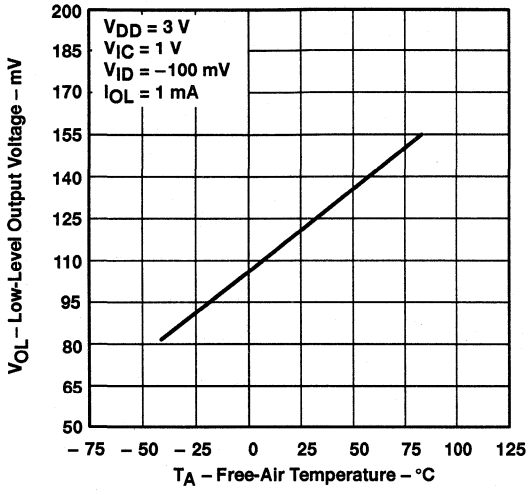


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

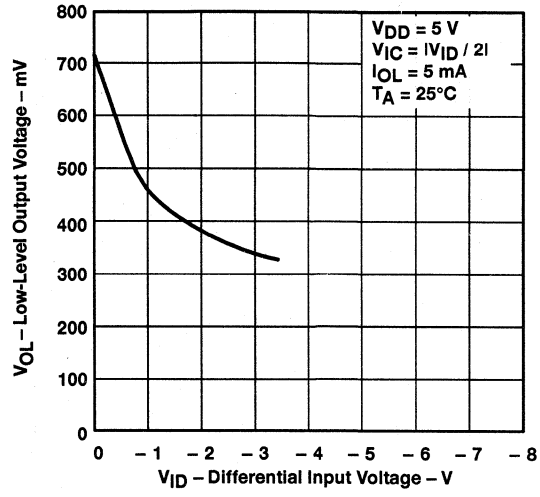


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

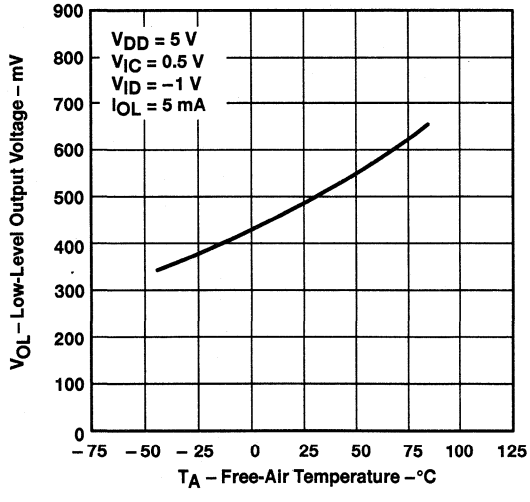


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

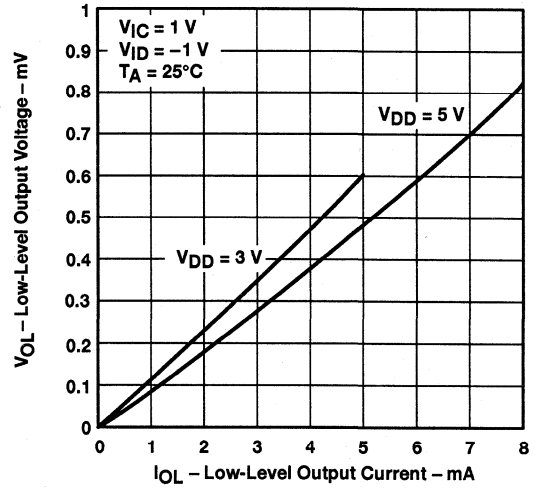


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

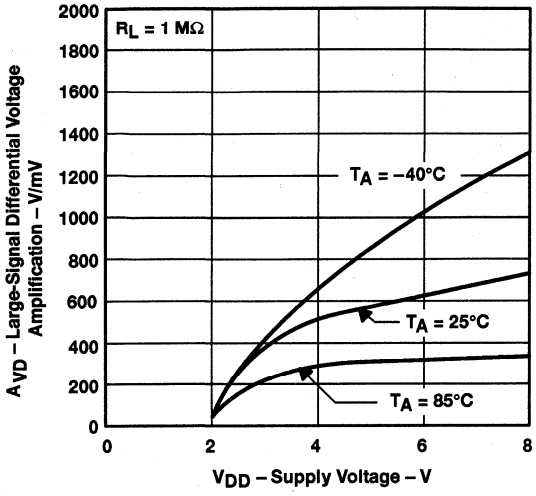


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

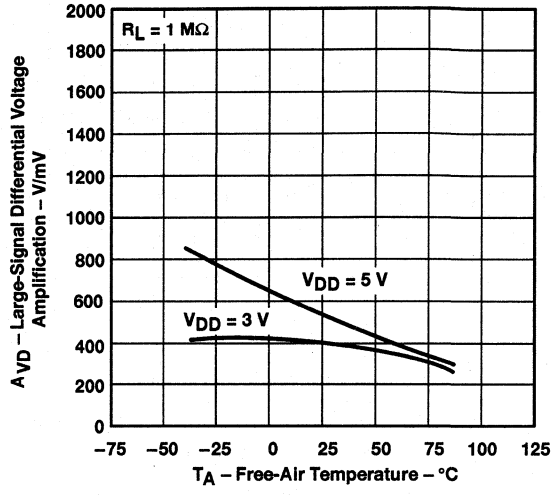
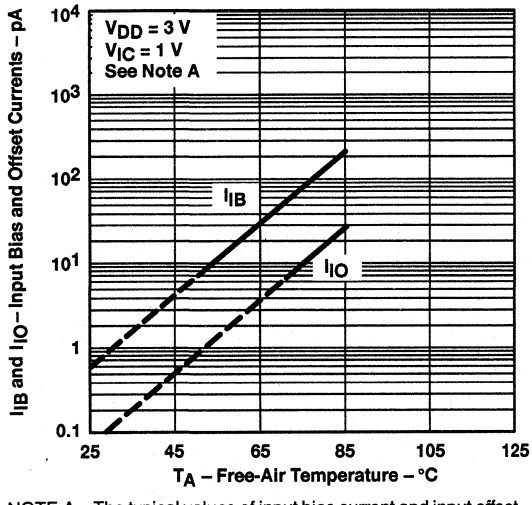


Figure 14

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

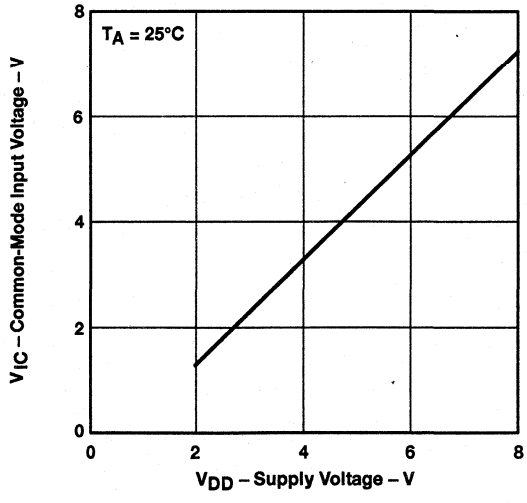


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

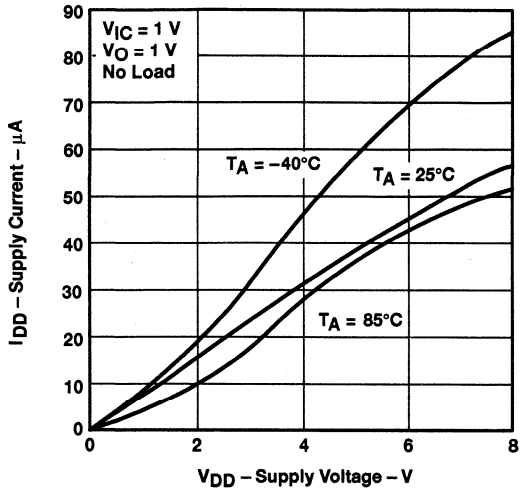


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

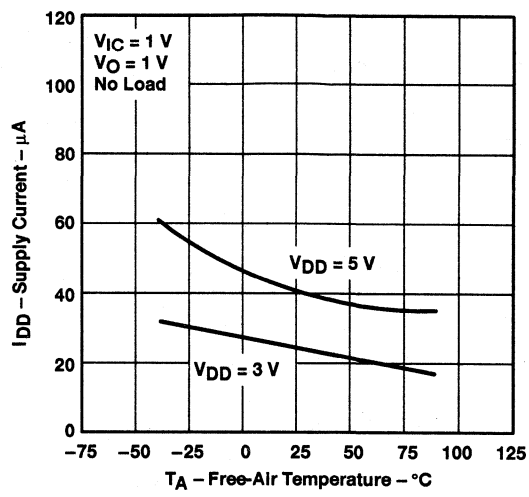


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

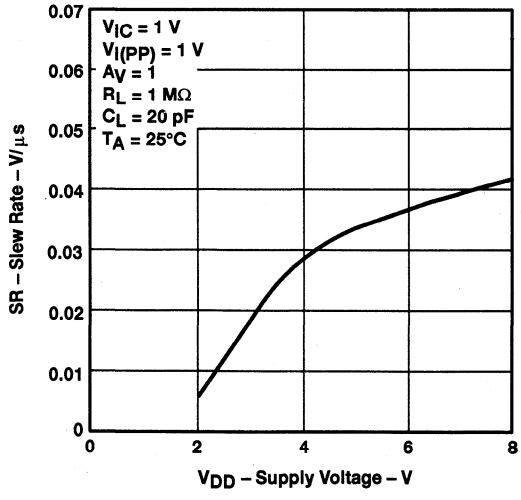


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

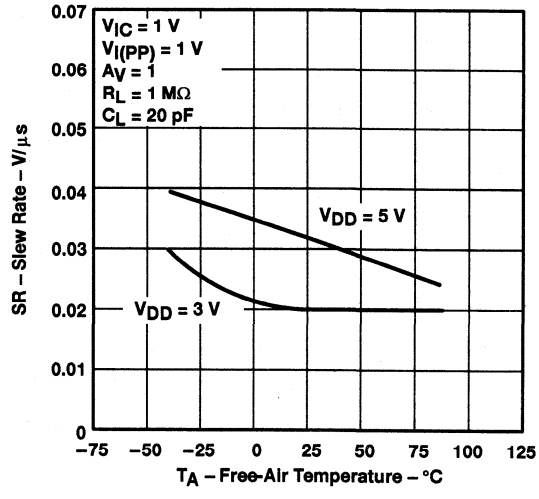


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

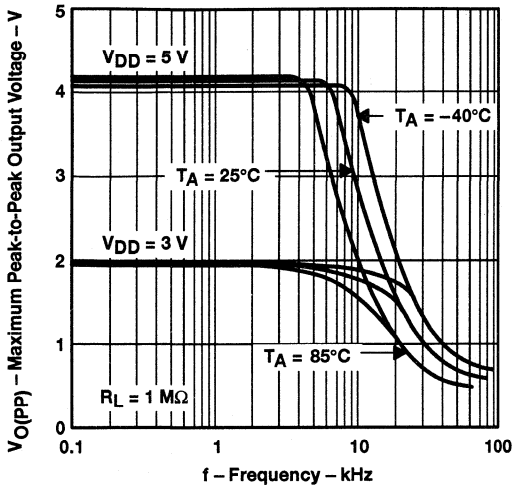


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

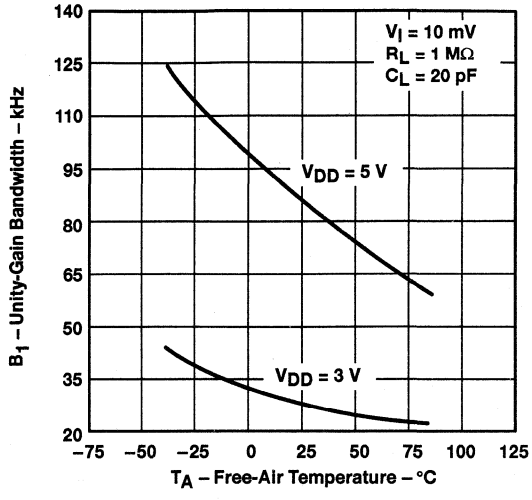


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

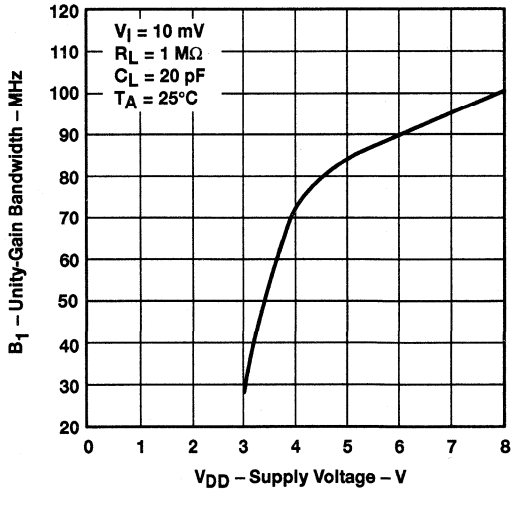


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

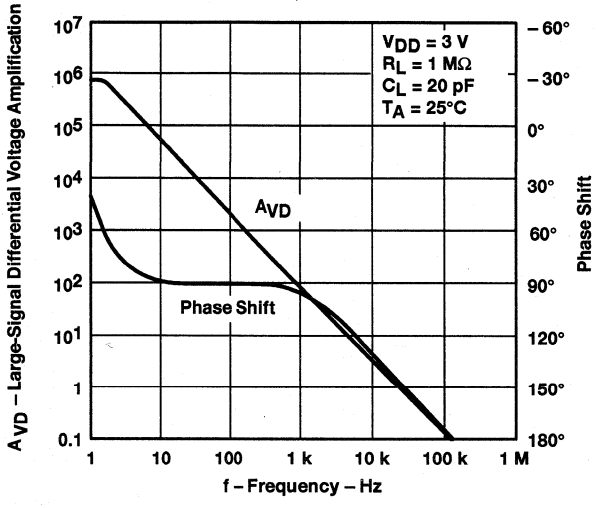


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

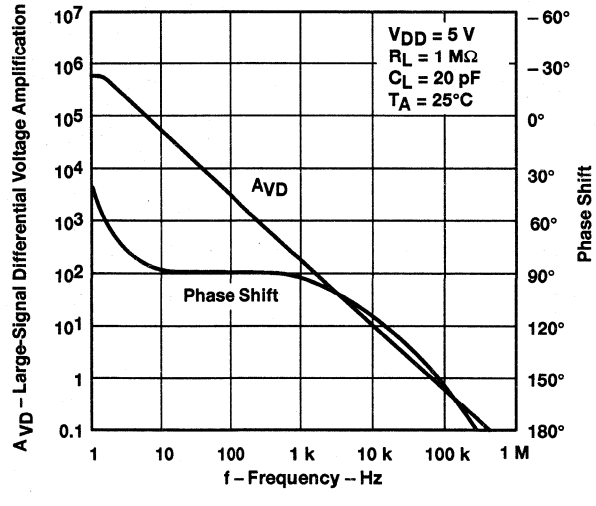


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

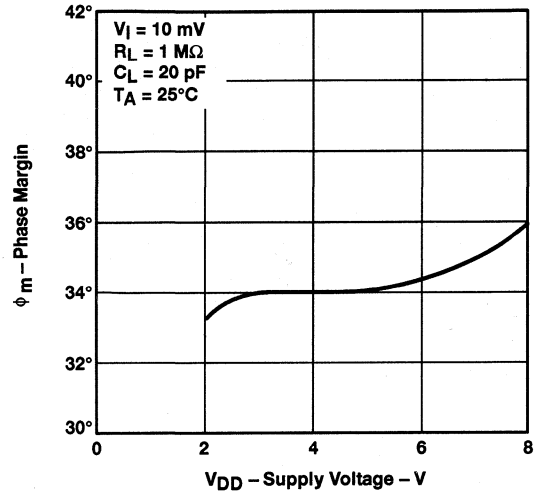


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

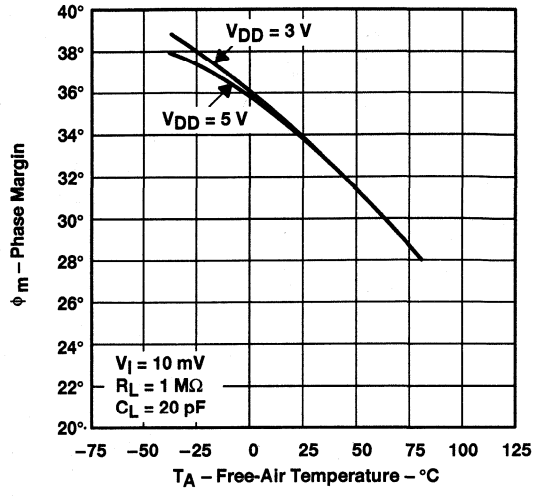


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

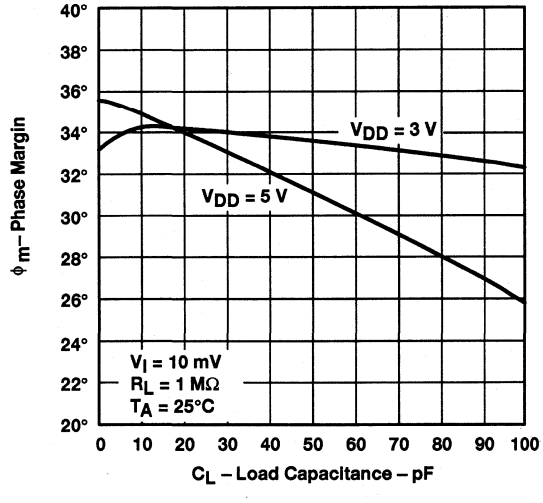


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

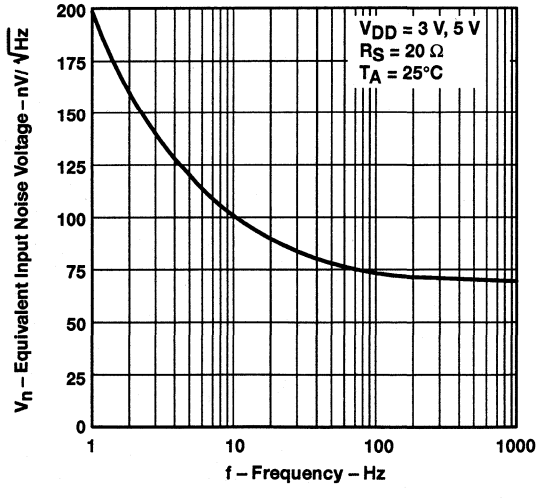
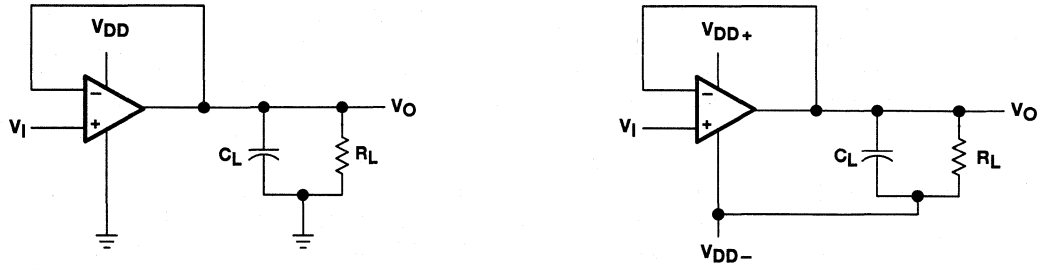


Figure 29

PARAMETER MEASUREMENT INFORMATION

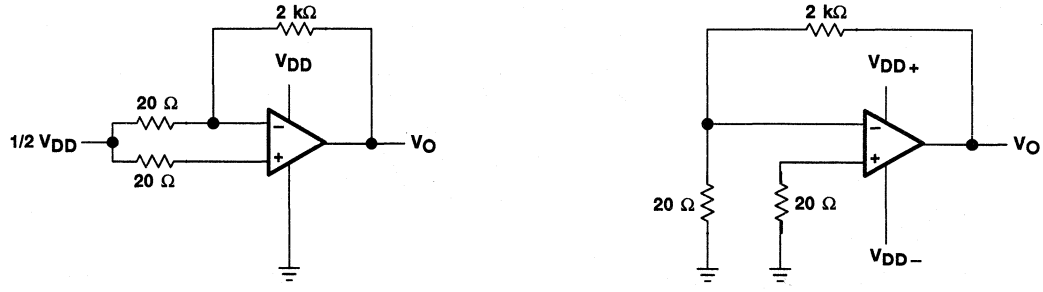
single-supply versus split-supply test circuits

Because the TLV2324 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



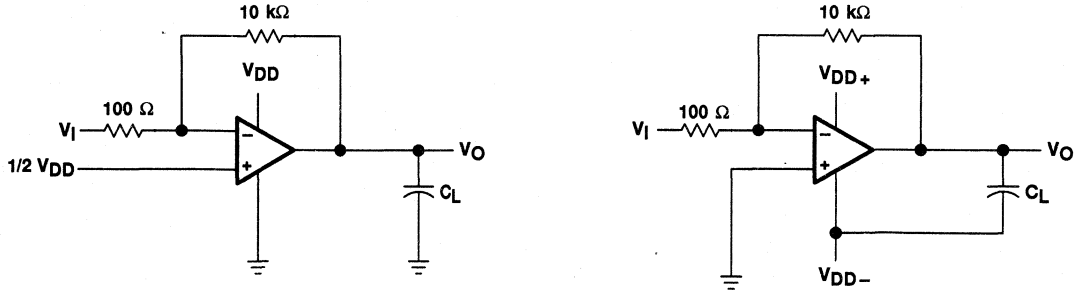
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 31. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2324 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

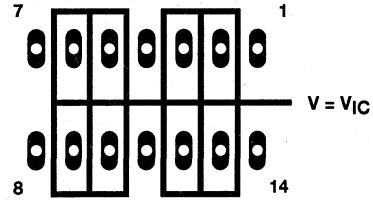


Figure 33. Isolation Metal Around Device Inputs (N package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

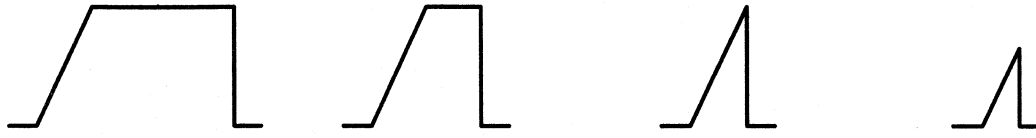


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2324 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

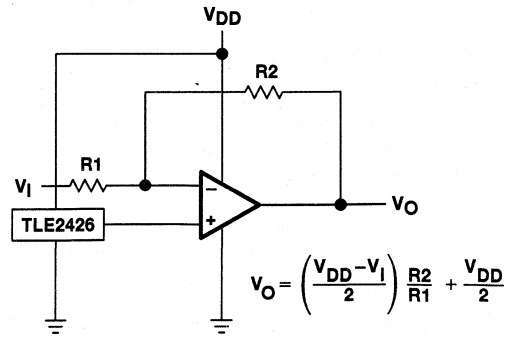
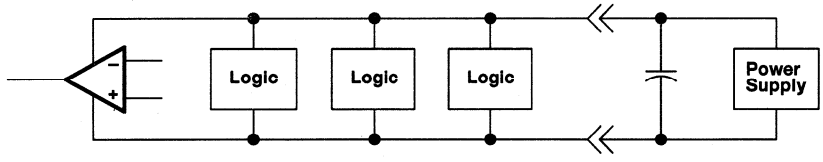


Figure 35. Inverting Amplifier With Voltage Reference

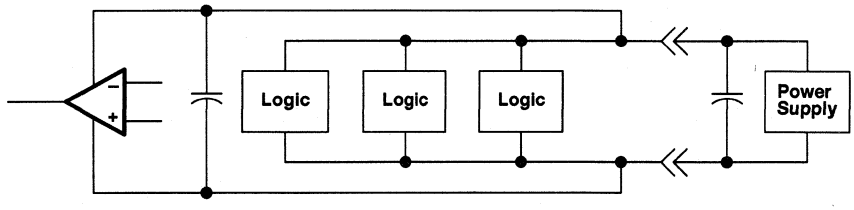
Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

The TLV2324 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON-SUPPLY RAILS



(b) SEPARATE-BYPASSED SUPPLY RAILS (preferred)

Figure 36. Common Versus Separate Supply Rails

APPLICATION INFORMATION

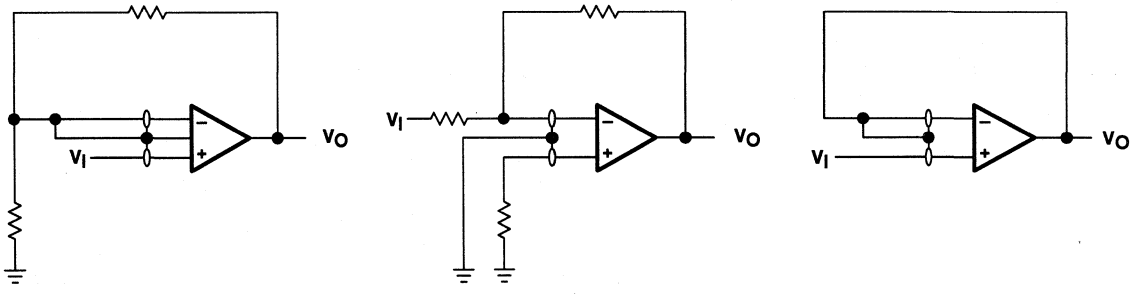
input characteristics

The TLV2324 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2324 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2324 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2324 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

APPLICATION INFORMATION

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

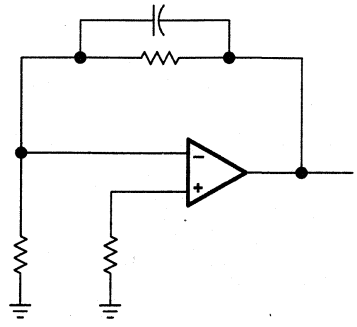


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2324 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2324 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal-protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rail as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with the increasing temperature and supply voltages.

APPLICATION INFORMATION

output characteristics

The output stage of the TLV2324 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2324 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

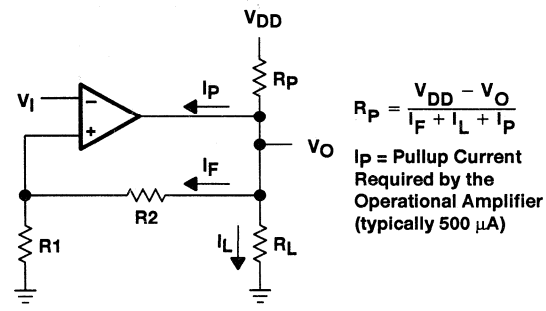


Figure 39. Resistive Pullup to Increase V_{OH}

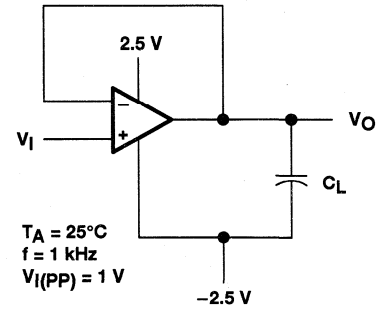
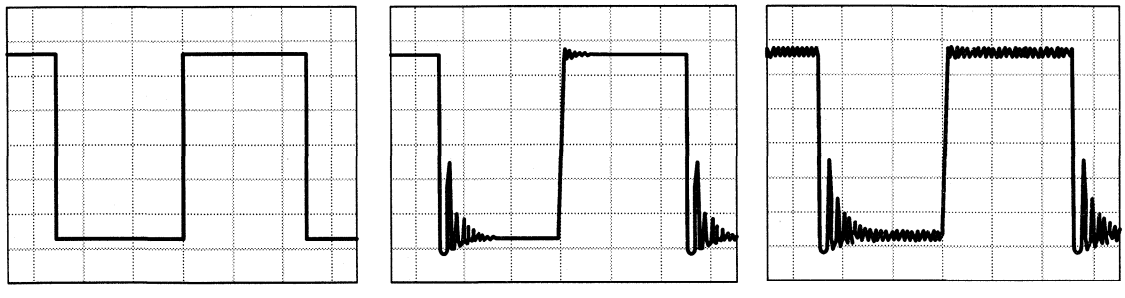


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2324 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

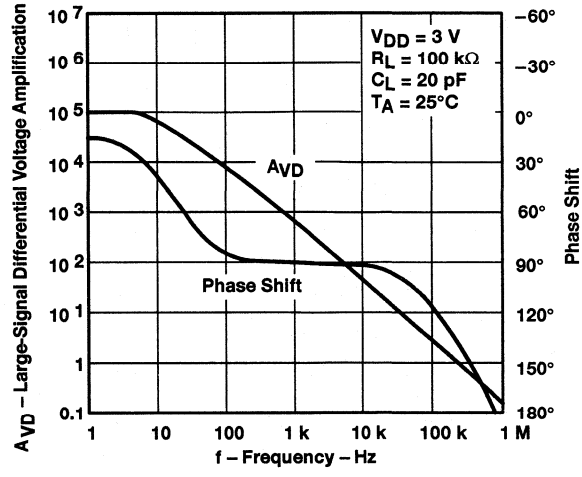


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



description

The TLV2332 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike the TLV2322 which is optimized for ultra-low power, the TLV2332 is designed to provide a combination of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V of the positive rail.

Having a maximum supply current of only 310 μA per amplifier over full temperature range, the TLV2332 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifier's typical slew rate is 0.38 V/μs and its bandwidth is 300 kHz. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels. The TLV2332 operational amplifiers are especially well suited for use in low-current or battery-powered applications.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

To facilitate the design of small portable equipment, the TLV2332 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline package (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	9 mV	TLV2332ID	TLV2332IP	TLV2332IPWLE	TLV2332Y

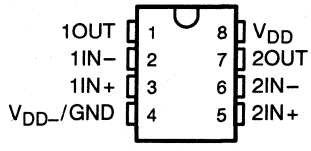
The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2332IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2332IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

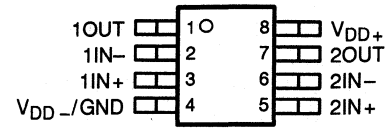
description (continued)

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2332 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

D OR P PACKAGE
(TOP VIEW)



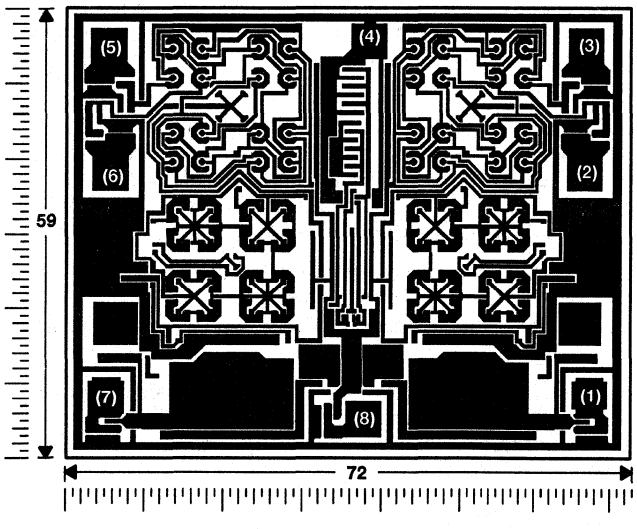
PW PACKAGE
(TOP VIEW)

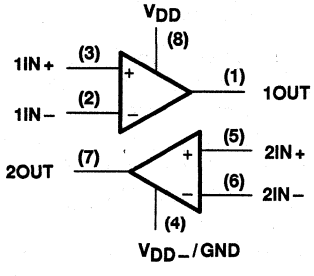


TLV2332Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2332. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

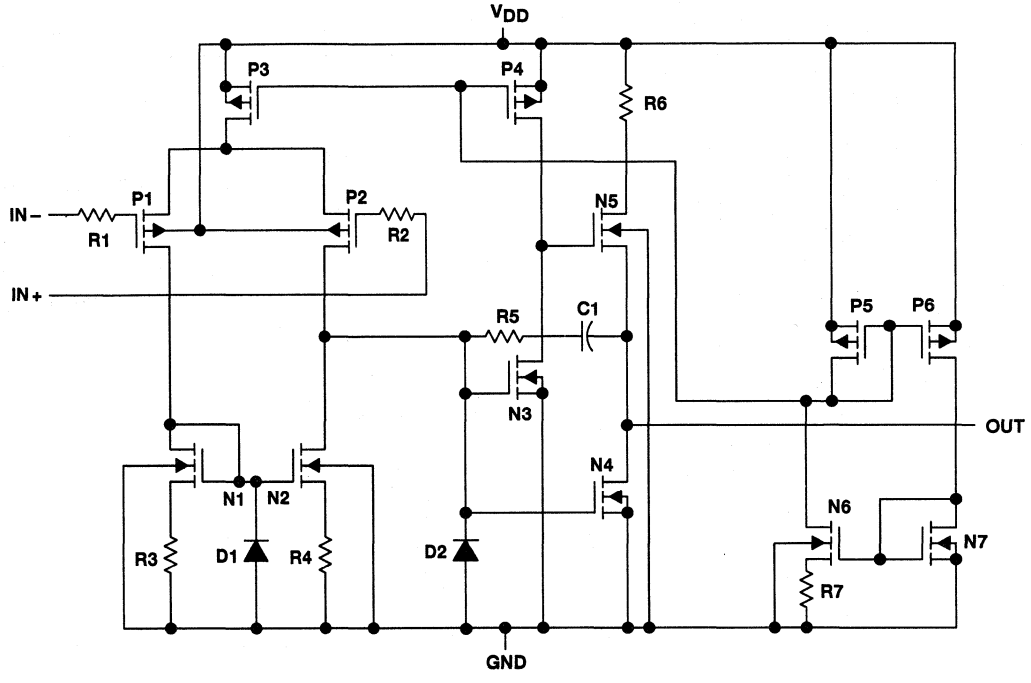
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2332I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		160	500		210	560	μA
			Full range			620			800	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2332I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2332I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		43°		
				25°C		40°		
				85°C		38°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2332Y						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ		0.6	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	94		70	94		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		160	500		210	560	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	5 6 7
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	8 9, 11 10 12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature	13 14
I_{IB}	Input bias current	vs Temperature	15
I_{IO}	Input offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage vs Temperature	17 18
SR	Slew rate	vs Supply voltage vs Temperature	19 20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	22 23
A_{VD}	Large-signal differential voltage amplification	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	26 27 28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE

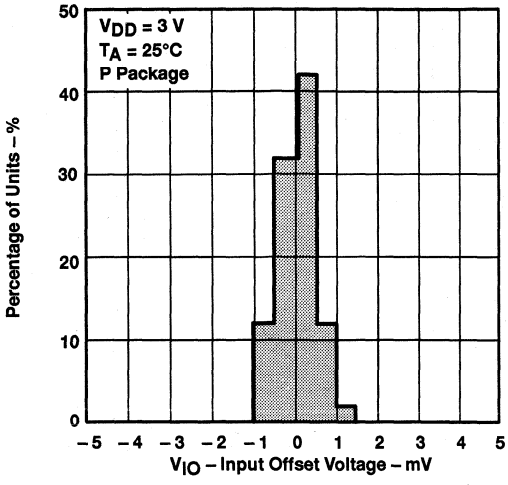


Figure 1

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE

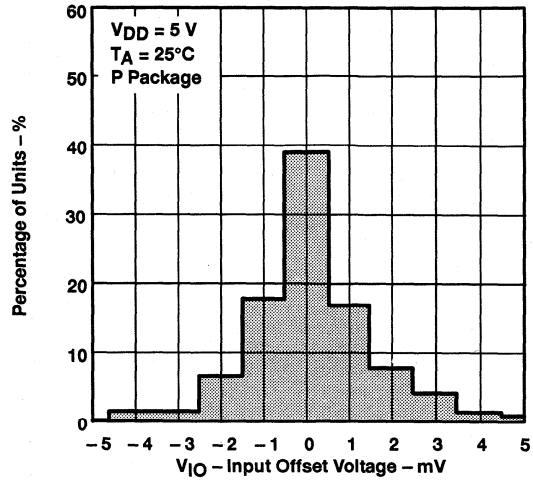


Figure 2

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

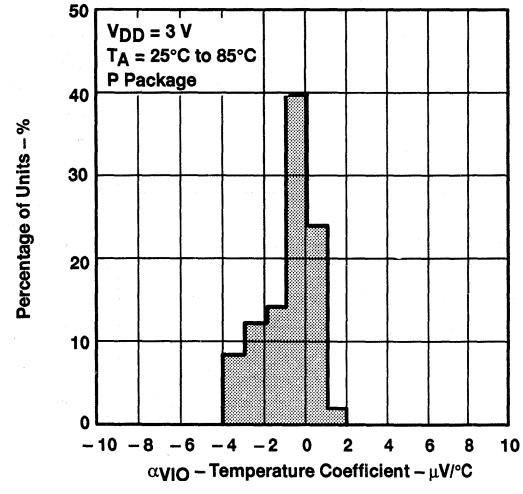


Figure 3

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

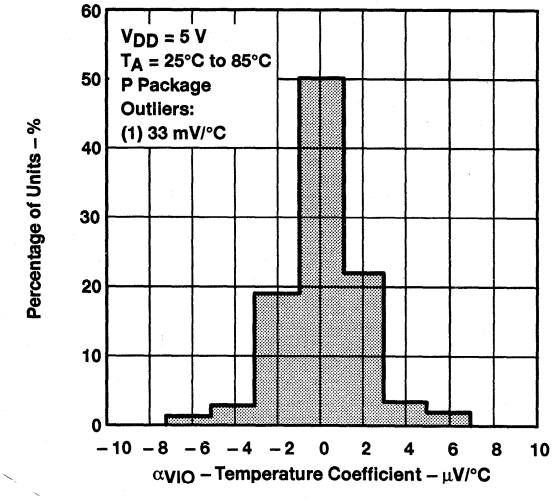


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

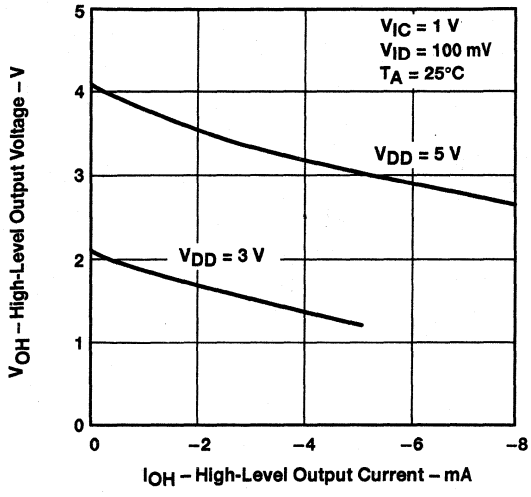


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

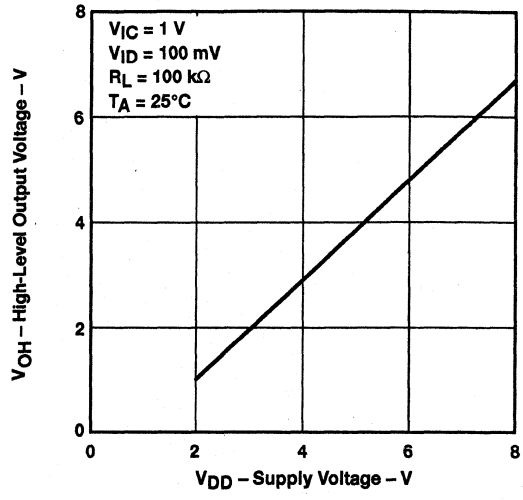


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

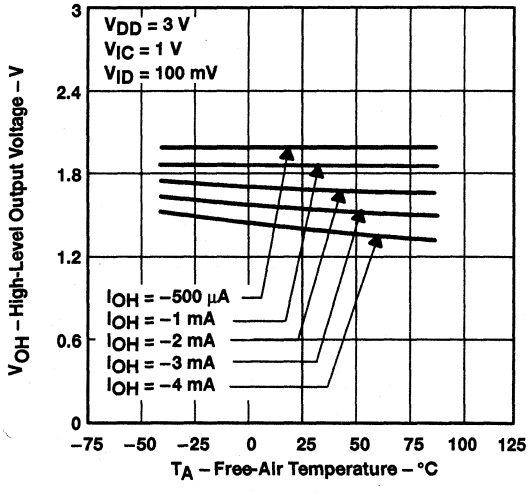


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

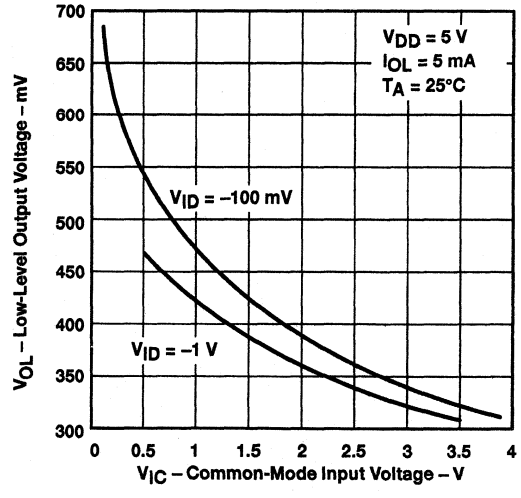


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

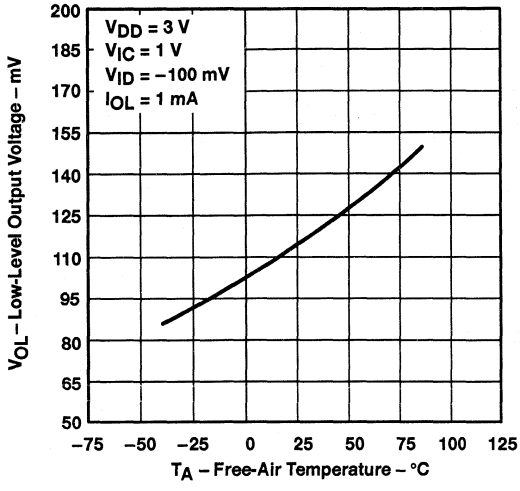


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

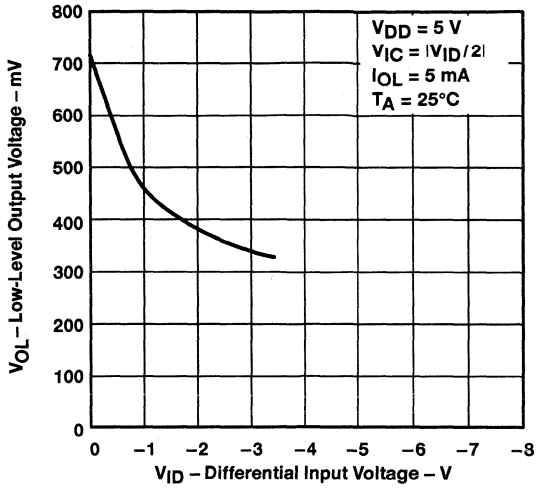


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

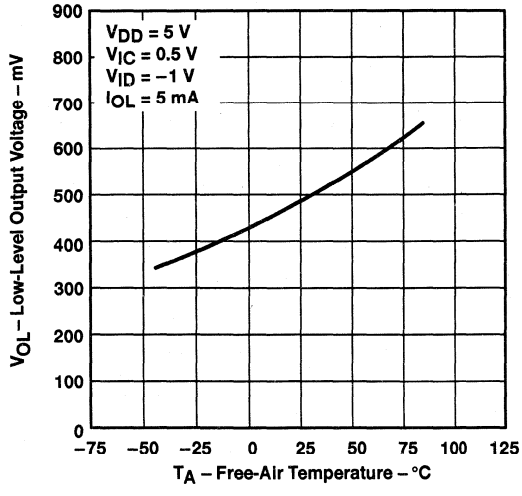


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

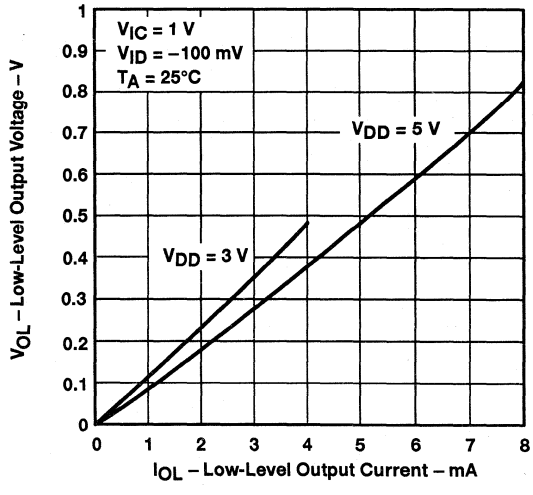


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

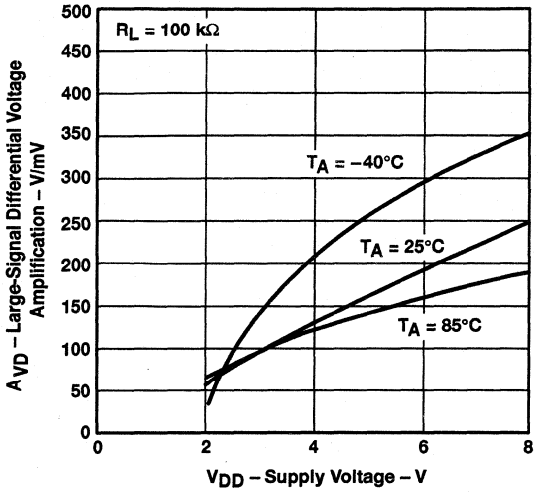


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

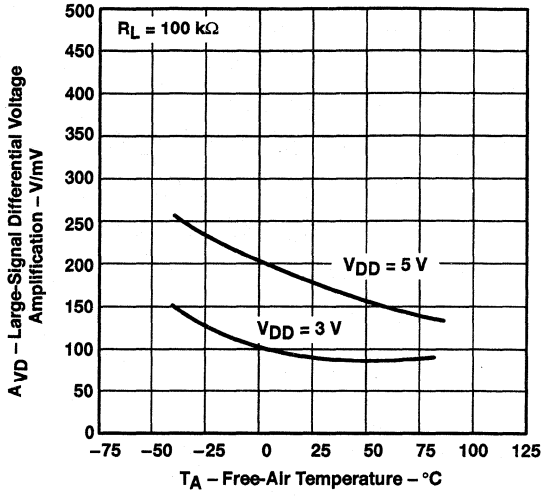
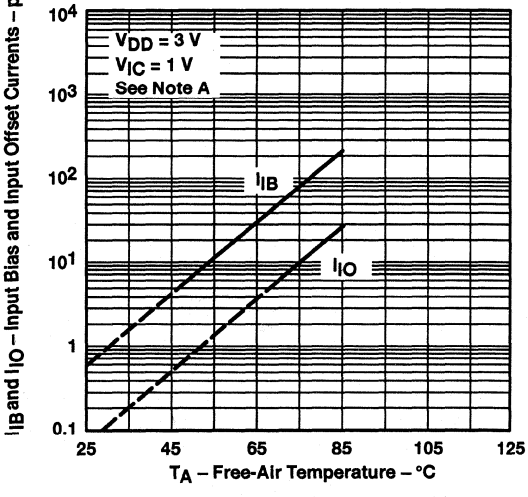


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

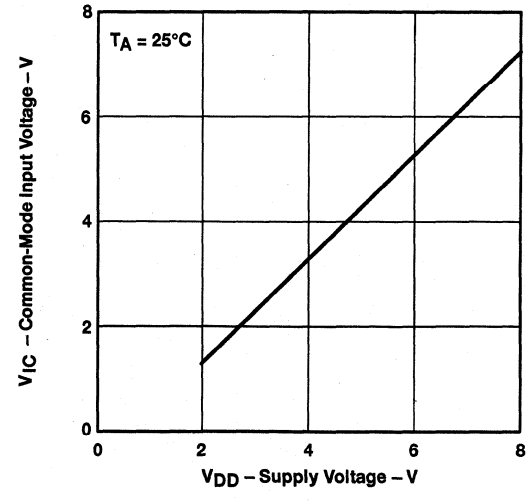


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

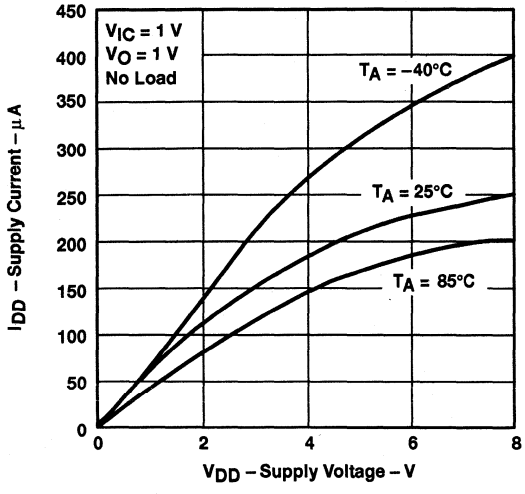


Figure 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

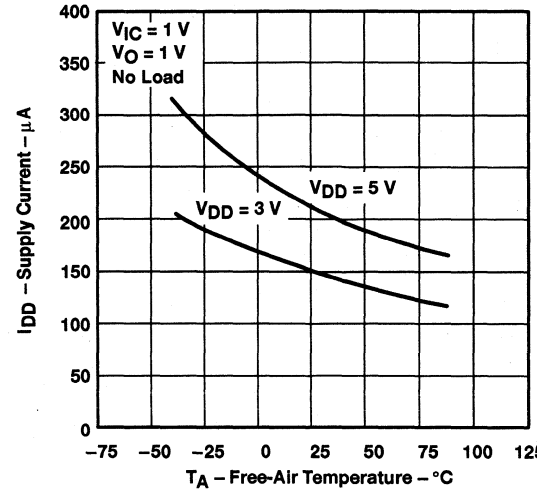


Figure 18

SLEW RATE
vs
SUPPLY VOLTAGE

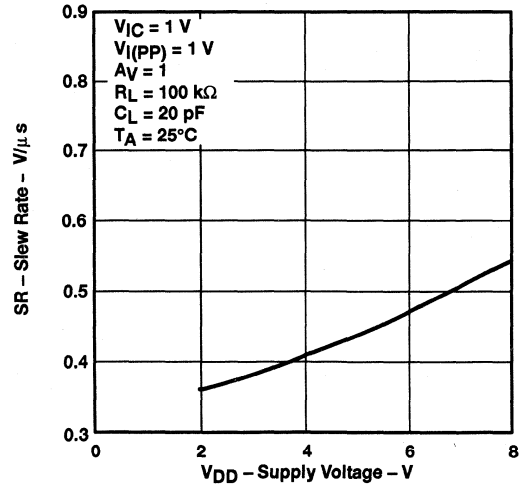


Figure 19

SLEW RATE
vs
FREE-AIR TEMPERATURE

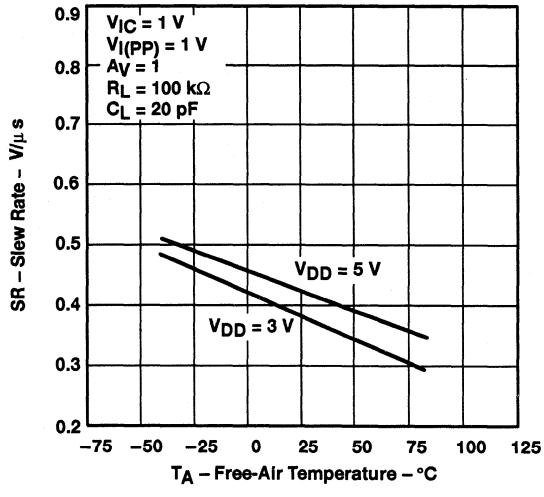


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

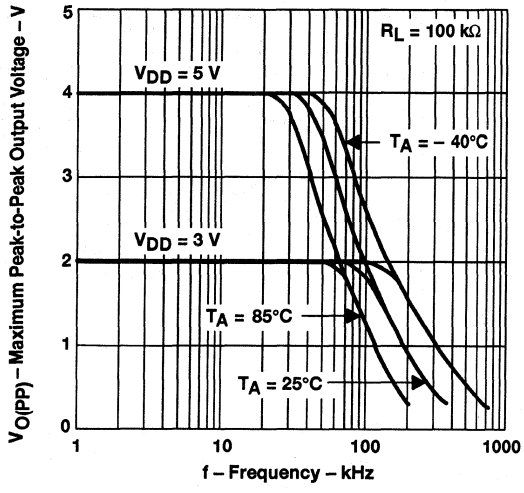


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

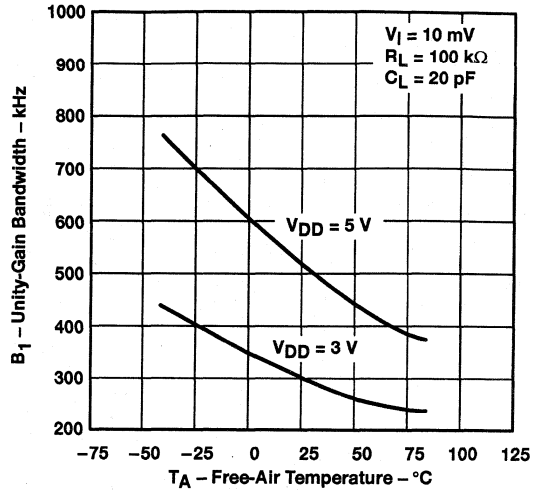


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

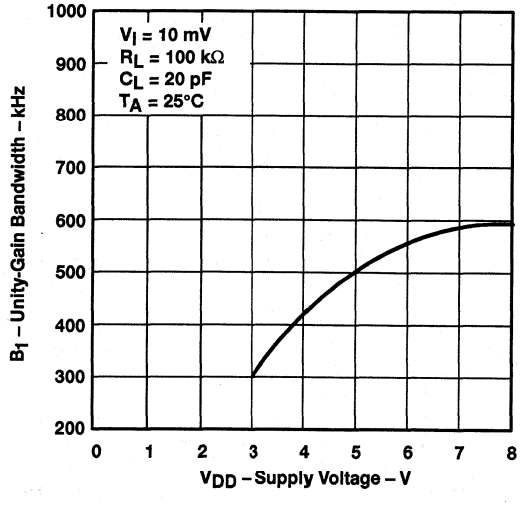


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

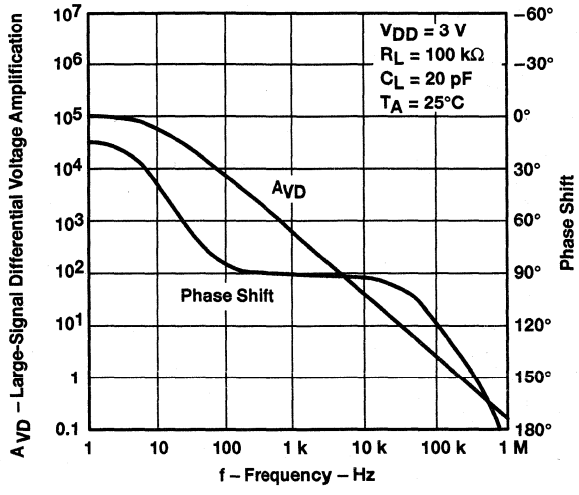


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

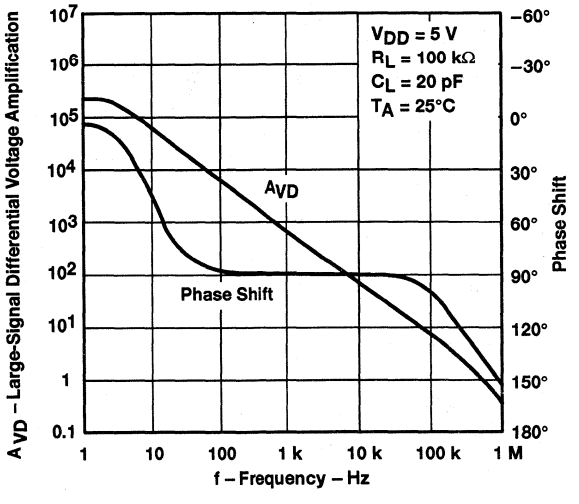


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

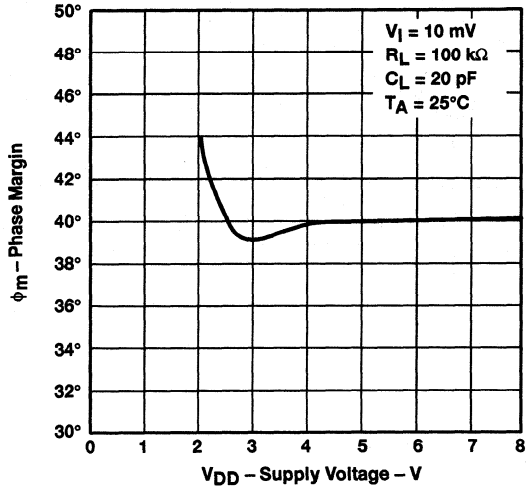


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

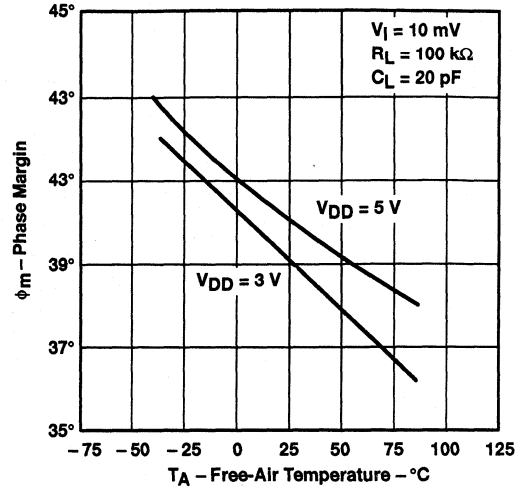


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

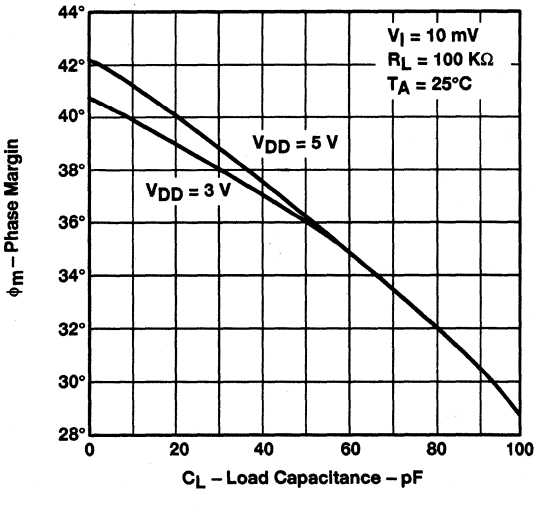


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

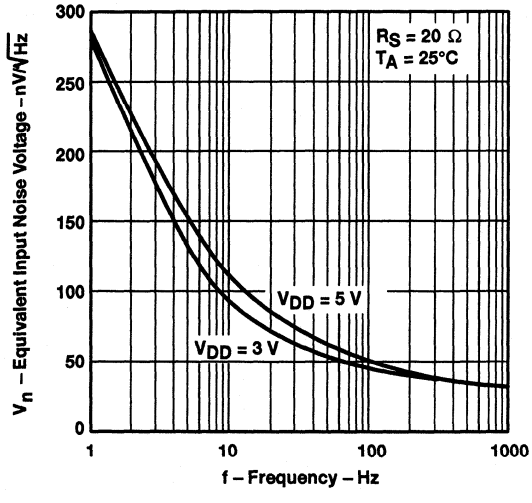
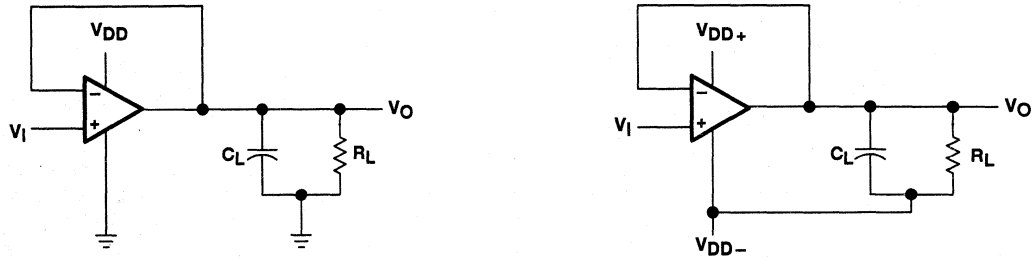


Figure 29

PARAMETER MEASUREMENT INFORMATION

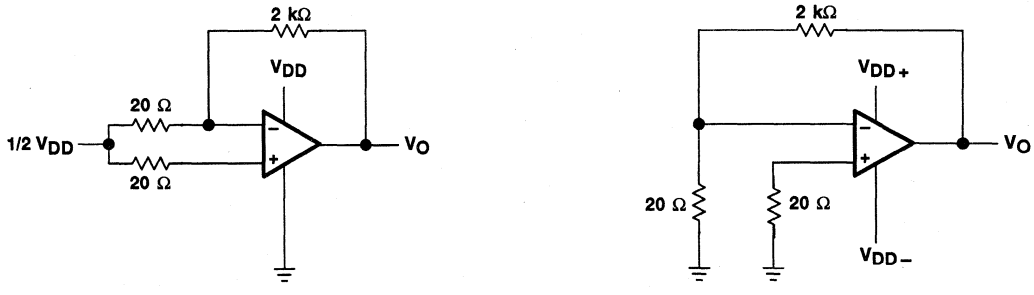
single-supply versus split-supply test circuits

Because the TLV2332 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



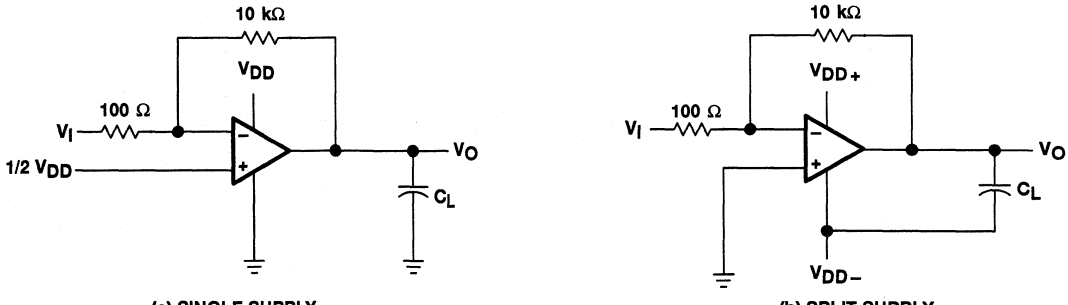
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 31. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2332 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

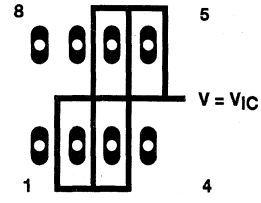


Figure 33. Isolation Metal Around Device Inputs
(P package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

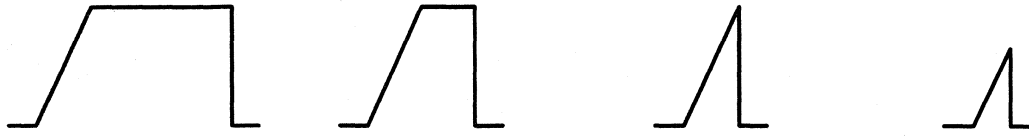
full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2332 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

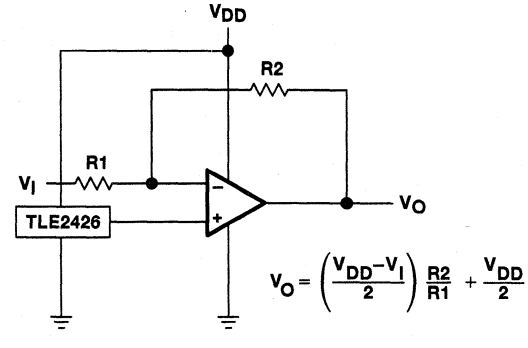


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2332 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

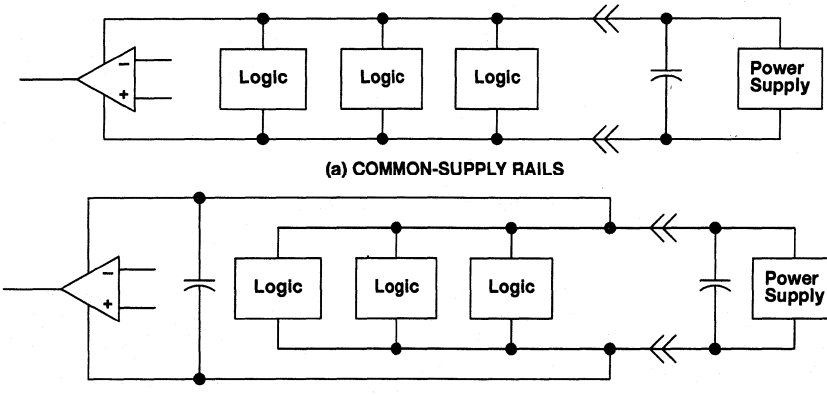


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2332 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

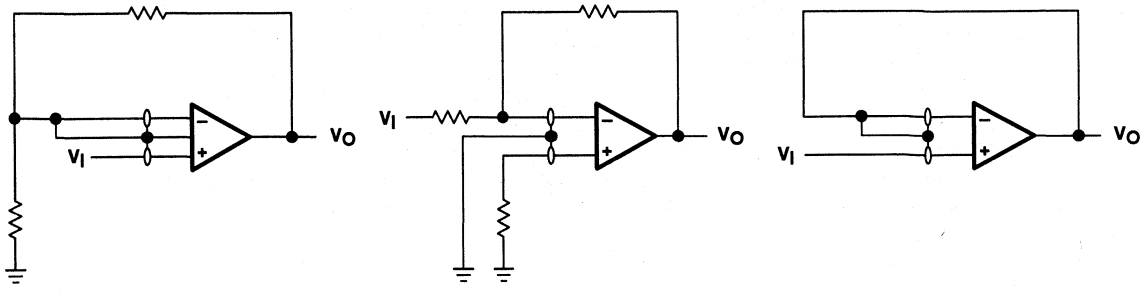
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2332 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2332 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2332 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifiers circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

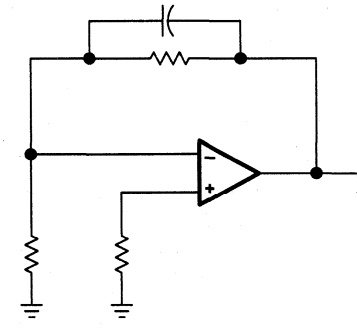


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2332 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C. Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2332 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however,

APPLICATION INFORMATION

techniques should be used to reduce the chance of latch-up whenever possible. Internal-protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2332 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2332 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

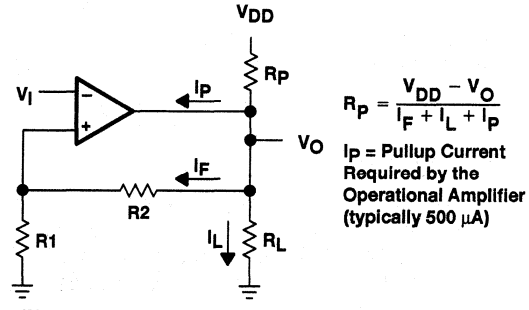


Figure 39. Resistive Pullup to Increase V_{OH}

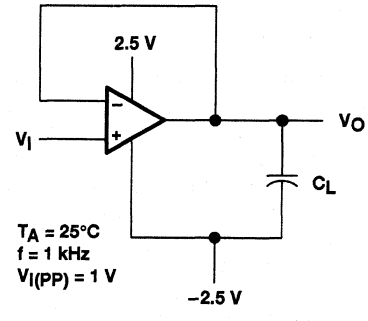
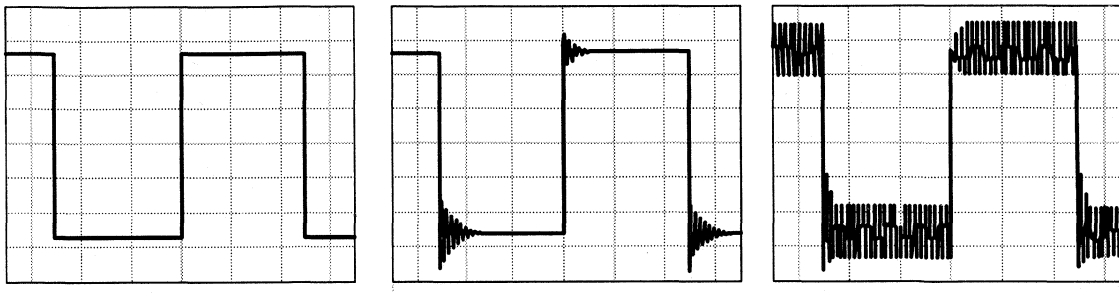


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2332 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

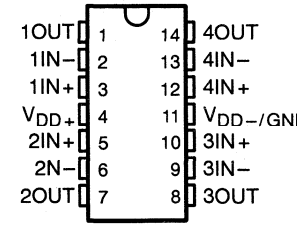
(b) C_L = 170 pF, R_L = NO LOAD

(c) C_L = 190 pF, R_L = NO LOAD

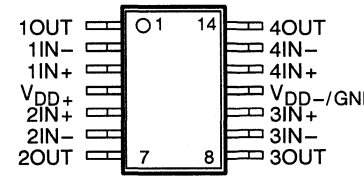
Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



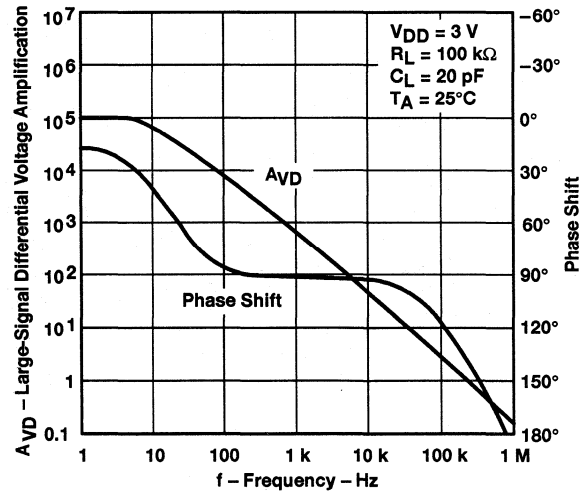
description

The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. Unlike the TLV2324 which is optimized for ultra-low power, the TLV2334 is designed to provide a combination of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V and is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of –40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

Having a maximum supply current of only 300 μA per amplifier over full temperature range, the TLV2334 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifier's typical slew rate is 0.38 V/μs and its bandwidth is 300 kHz. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels.

The TLV2334 operational amplifiers are especially well suited for use in low current or battery-powered applications.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	10 mV	TLV2334ID	TLV2334IN	TLV2334IPWLE	TLV2334Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2334IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2334IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents making them ideal for interfacing to high-impedance sources such as in sensor circuits or filter applications.

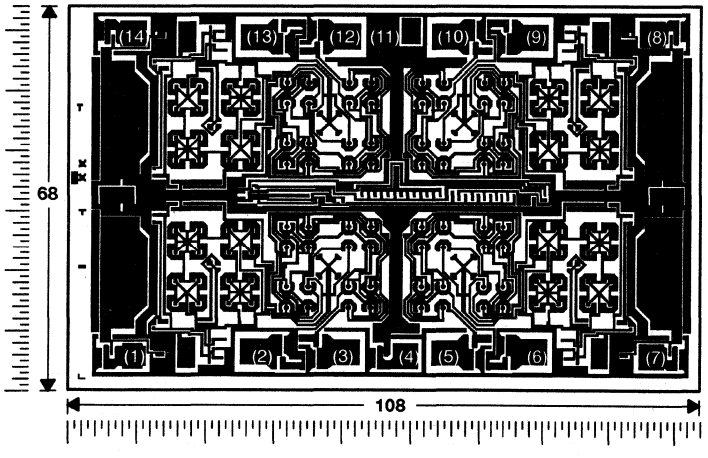
To facilitate the design of small portable equipment, the TLV2334 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

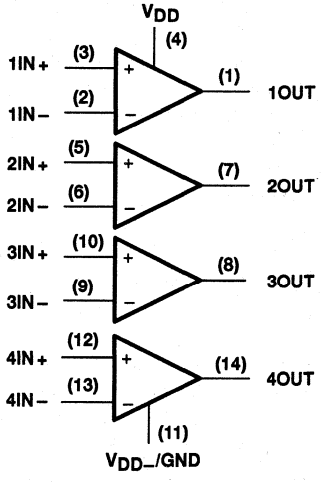
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2334 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2334Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2334. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

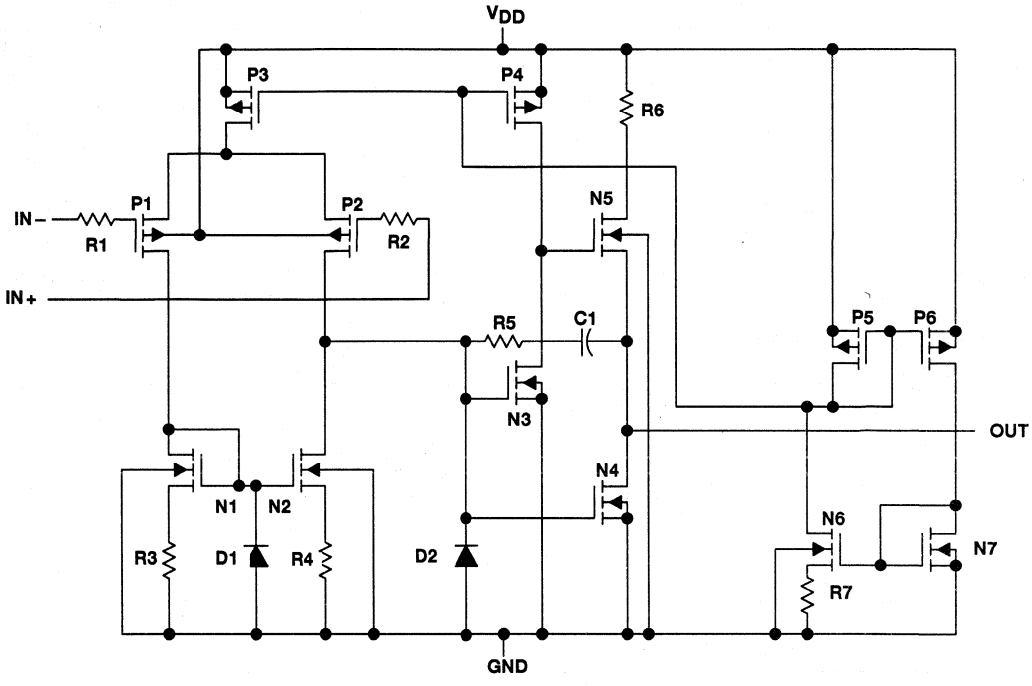
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	108
Diodes	8
Resistors	28
Capacitors	4

† Includes all amplifiers, ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage, range V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mV	7.6 mW/°C	494 mW
N	1575 mV	12.6 mW/°C	819 mW
PW	700 mV	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2334I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		320	1000		420	1120	μA
			Full range			1200			1600	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2334I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2334I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 30	25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 32	25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 100 kΩ,	−40°C		43°		
				25°C		40°		
				85°C		38°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2334Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V R_L = 100 kΩ		0.6	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = −100 mV,		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 100 kΩ,	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_{IC} = 1 V, R_S = 50 Ω	V_O = 1 V,	70	94		70	94		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		320	1000		420	1120	μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	5 6 7
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	8 9, 11 10 12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature vs Frequency	13 14 24, 25
I_{IB}	Input bias current	vs Temperature	15
I_{IO}	Input offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply current	16
I_{DD}	Supply current	vs Supply current vs Temperature	17 18
SR	Slew rate	vs Supply voltage vs Temperature	19 20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	22 23
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	26 27 28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE**

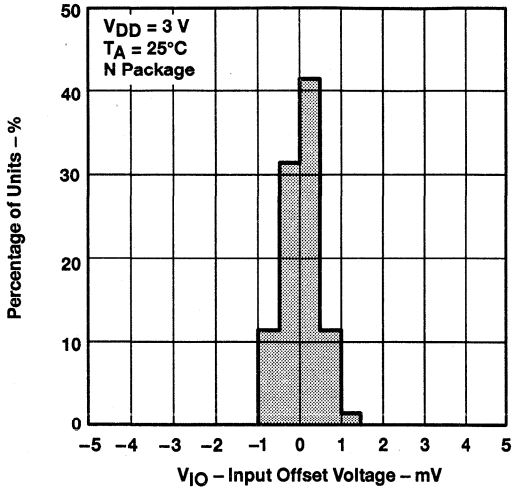


Figure 1

**DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE**

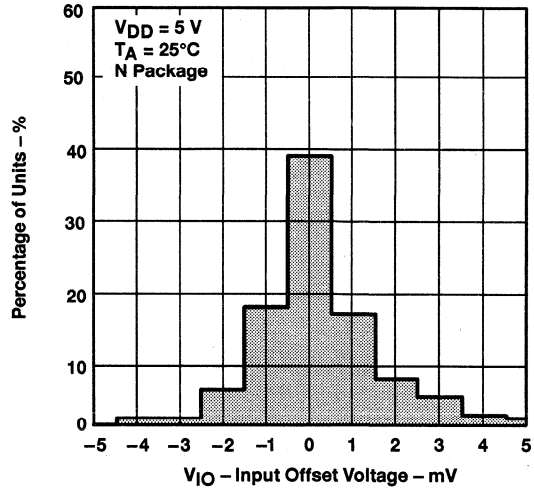


Figure 2

**DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

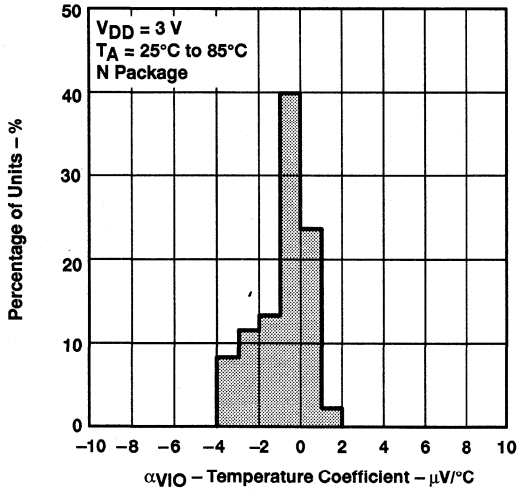


Figure 3

**DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

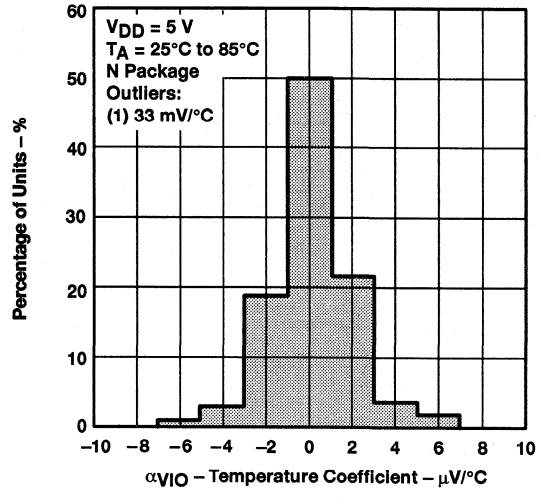


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

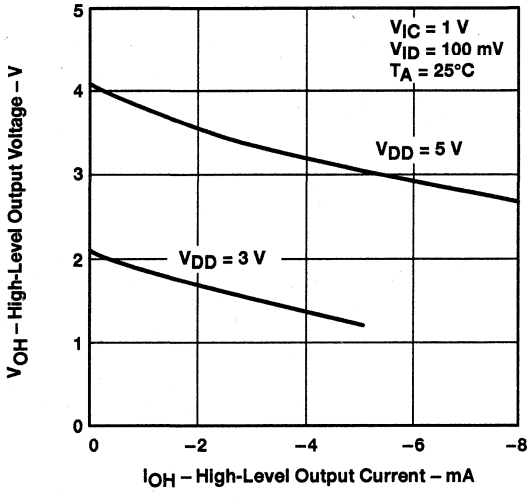


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

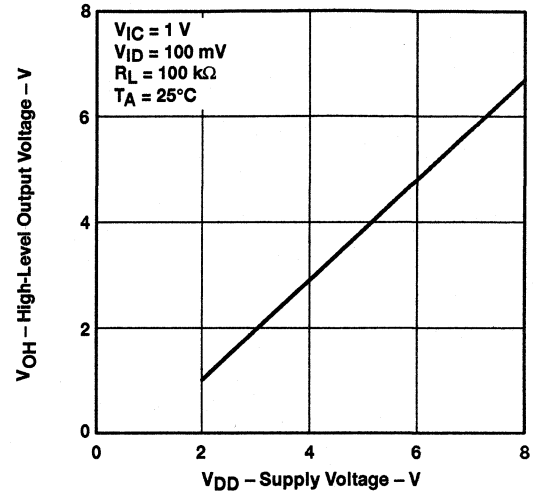


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

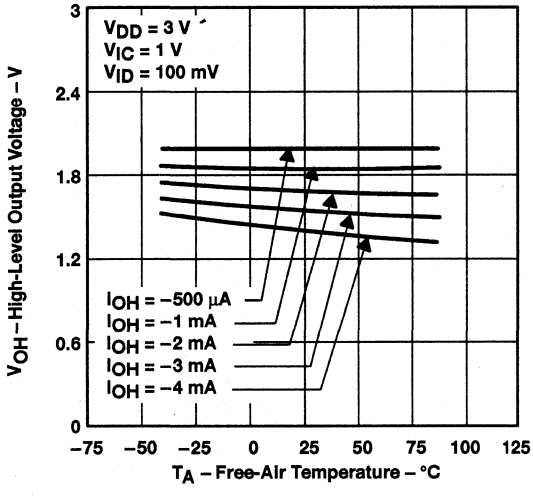


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

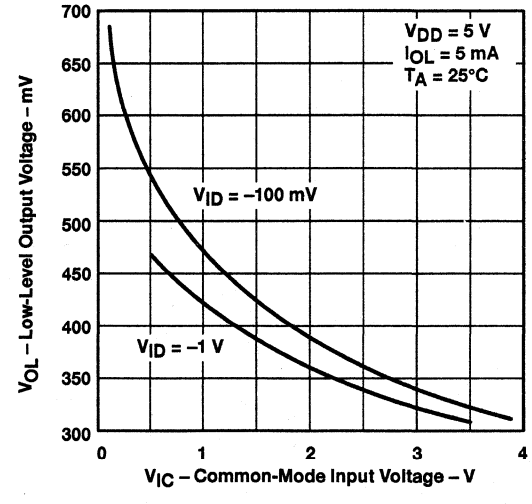


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

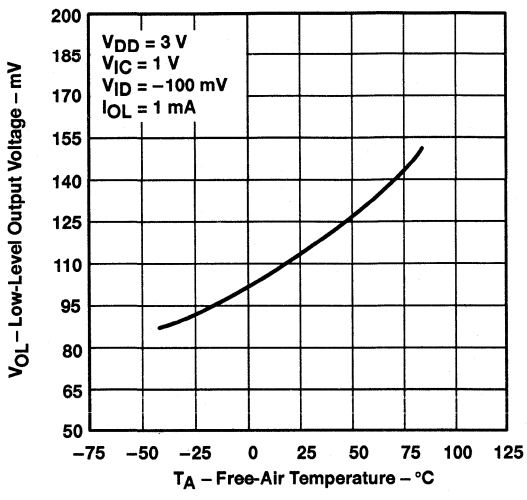


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

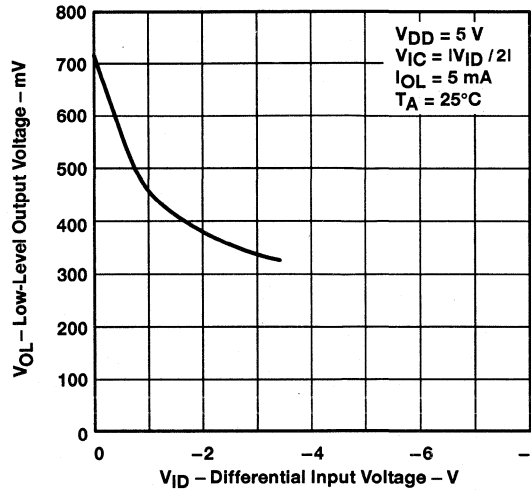


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

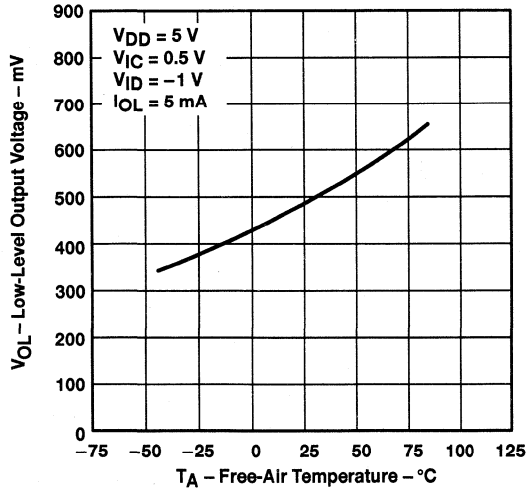


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

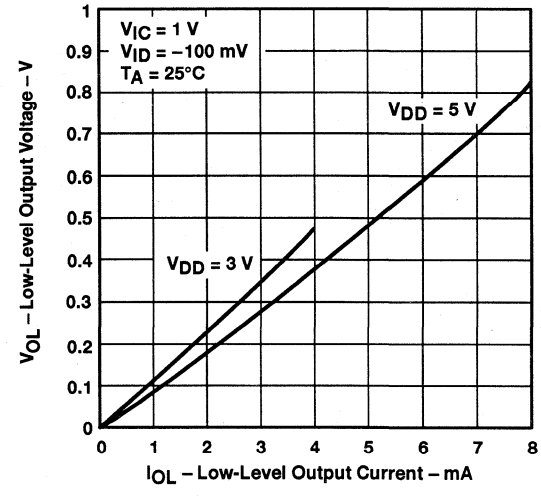


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

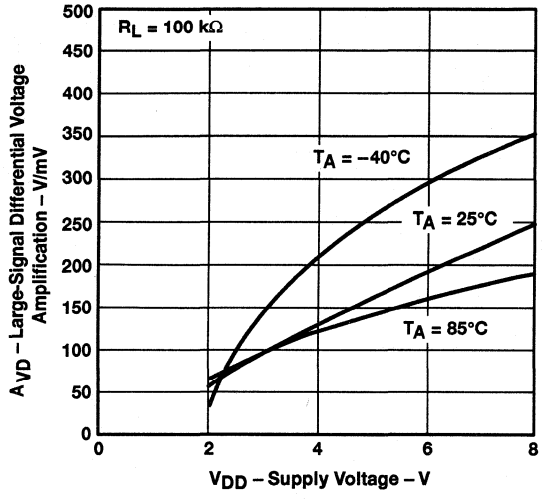


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

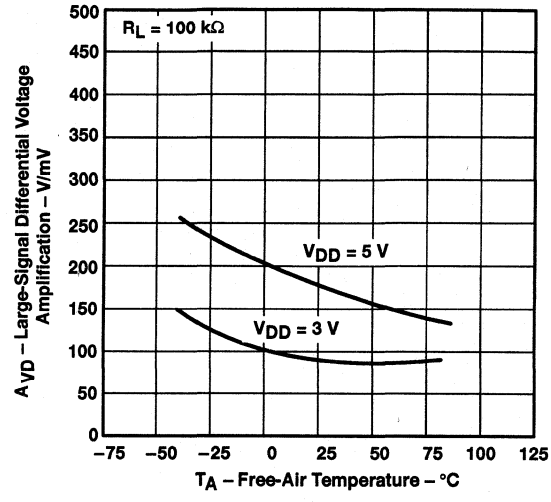


Figure 14

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

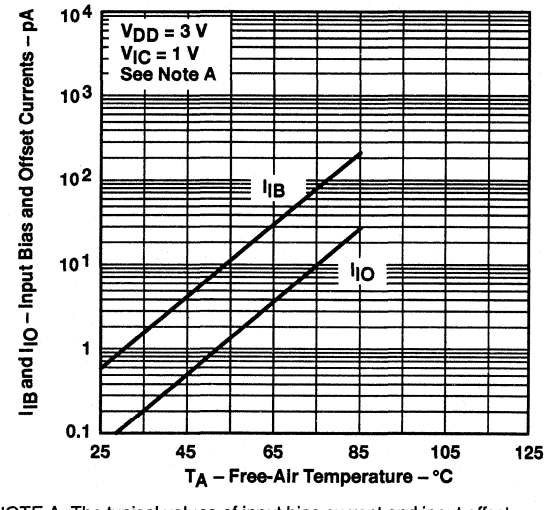


Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

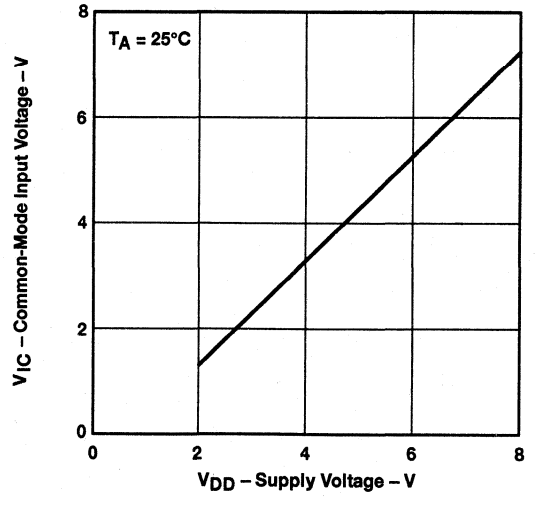


Figure 16

NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

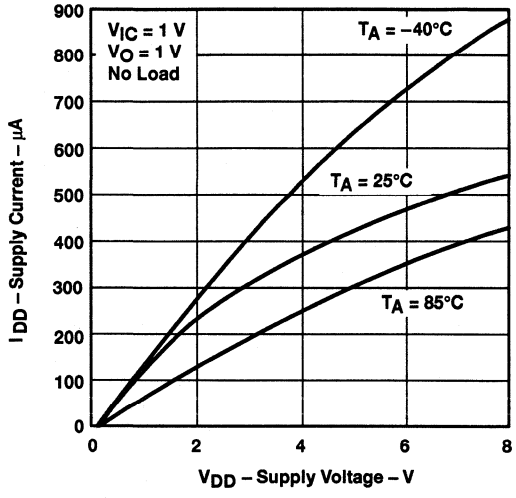


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

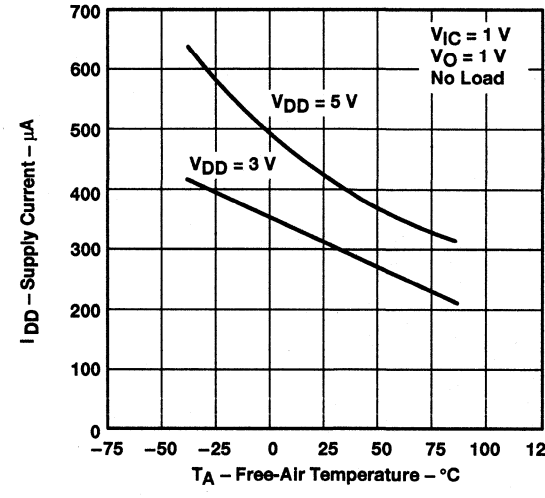


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

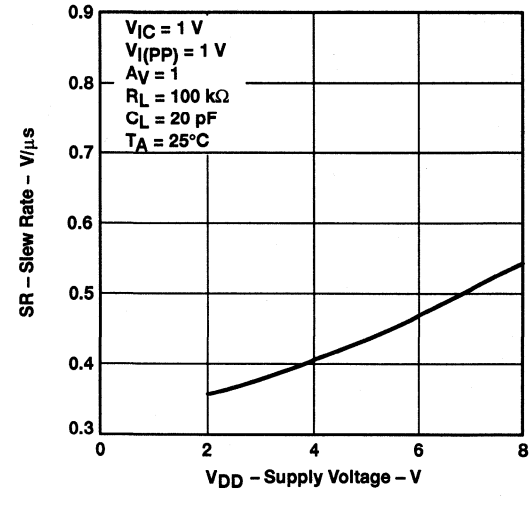


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

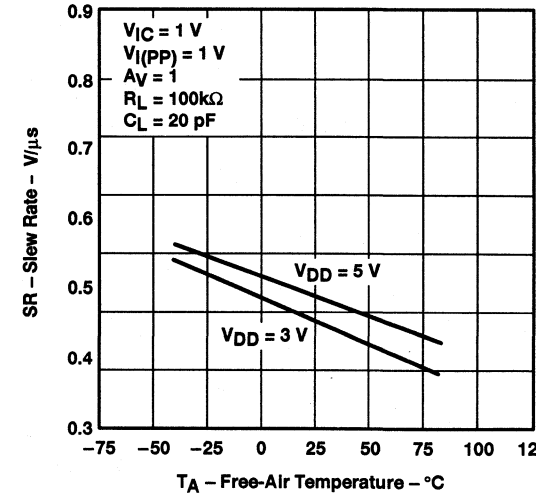


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

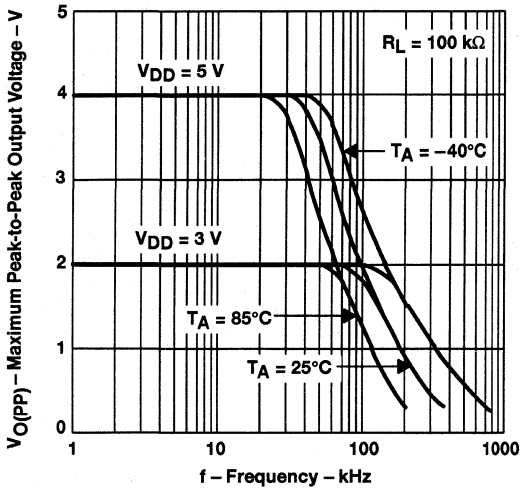


Figure 21

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

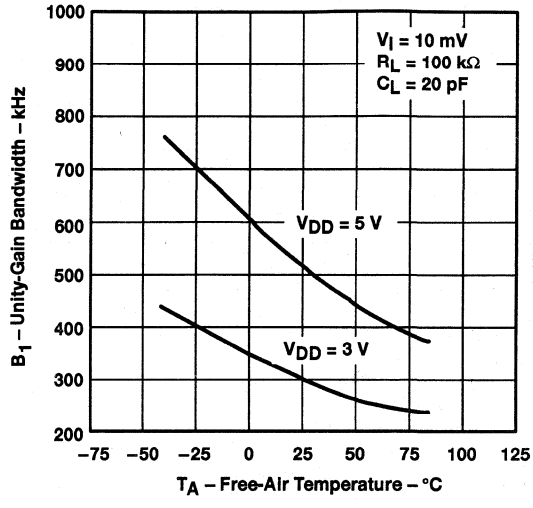


Figure 22

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

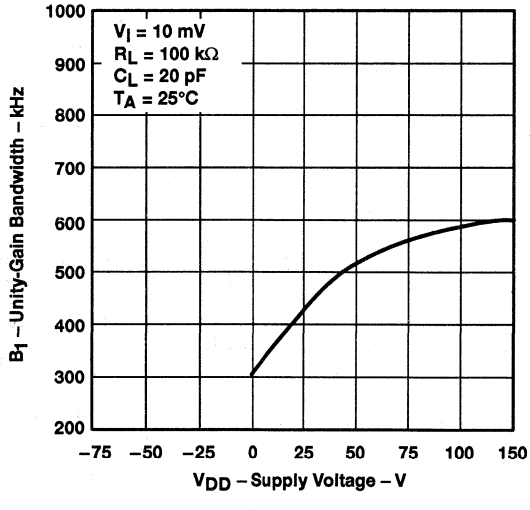


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

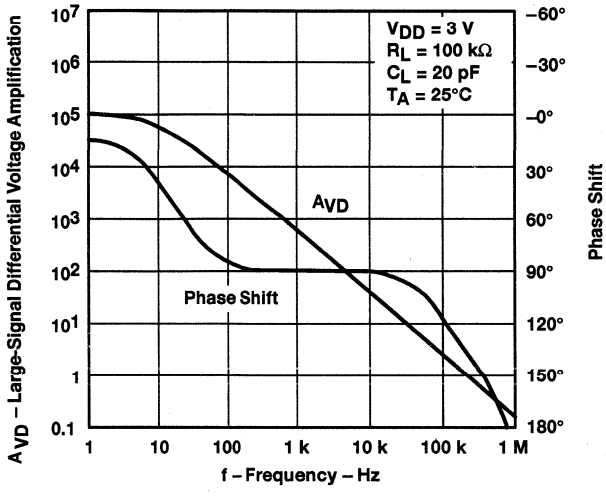


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

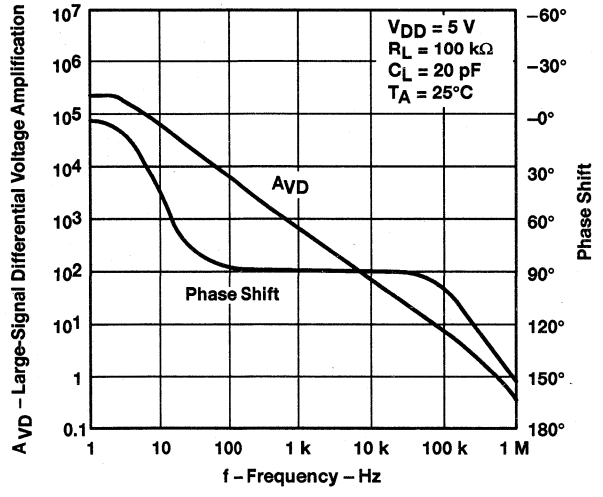


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

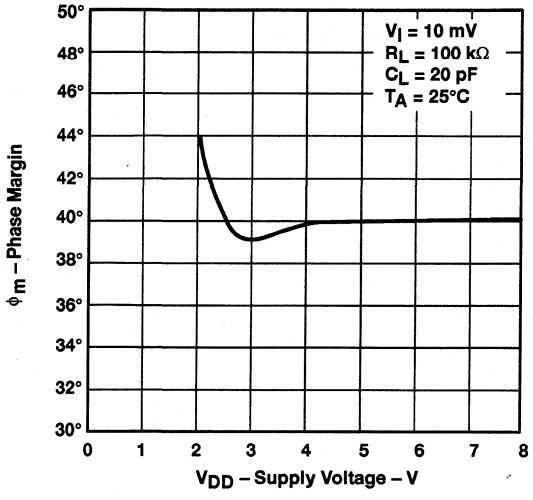


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

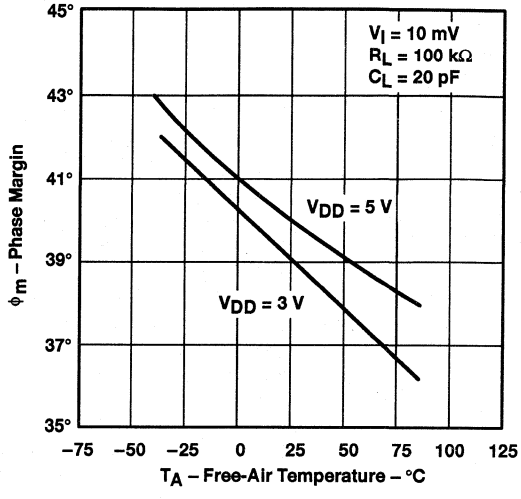


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

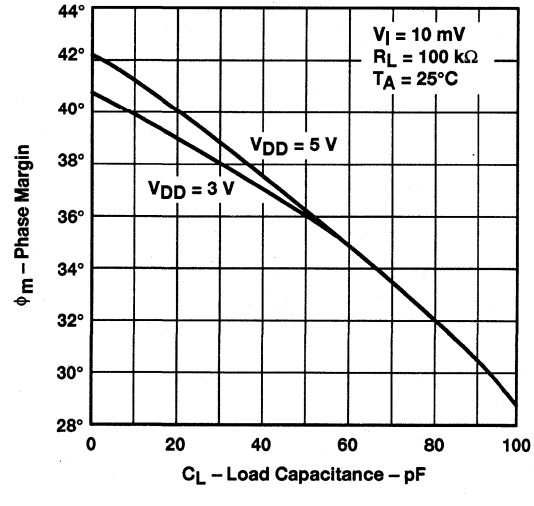


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

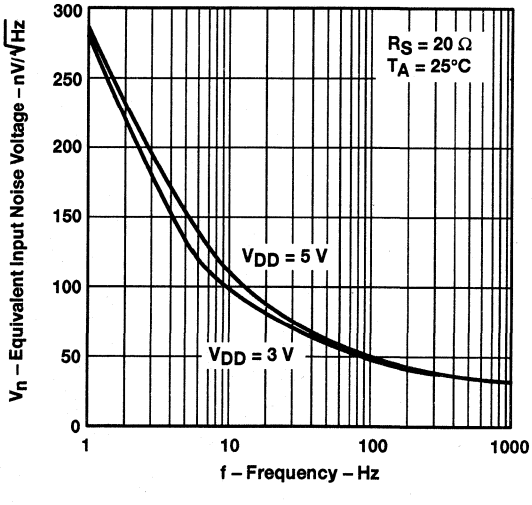


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2334 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

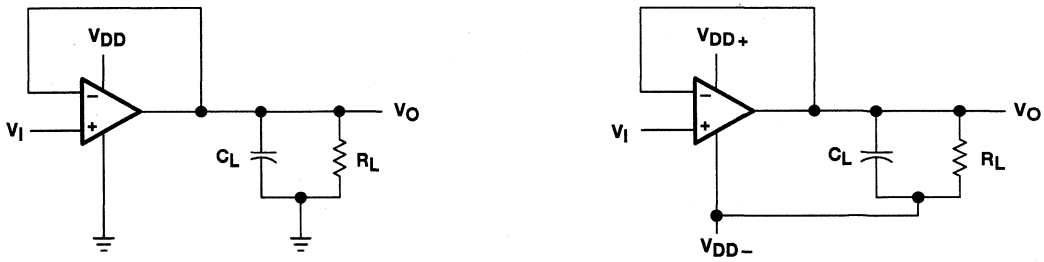


Figure 30. Unity-Gain Amplifier

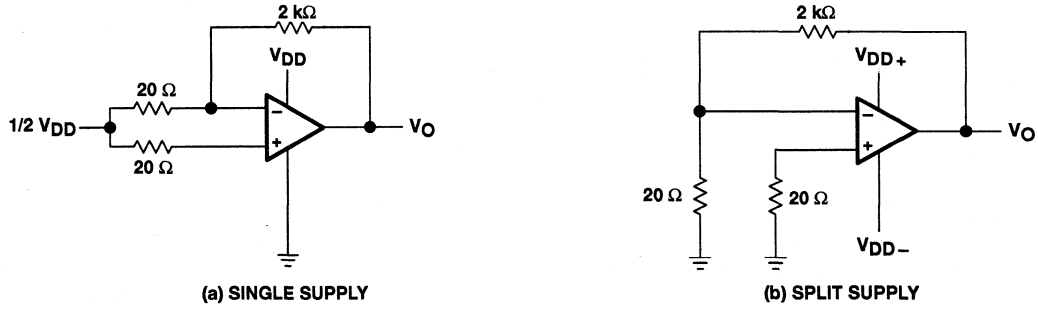


Figure 31. Noise-Test Circuit

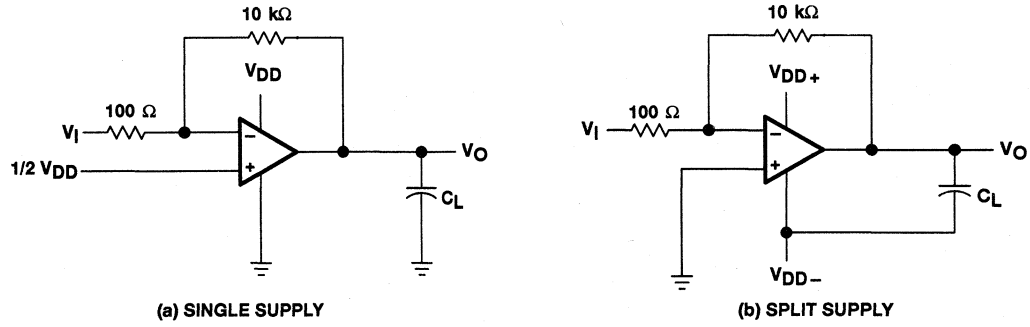


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2334 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.

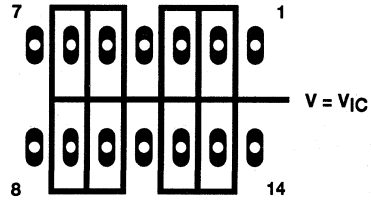


Figure 33. Isolation Metal Around Device Inputs (N package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

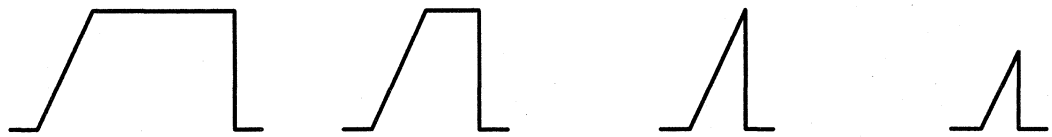


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2334 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

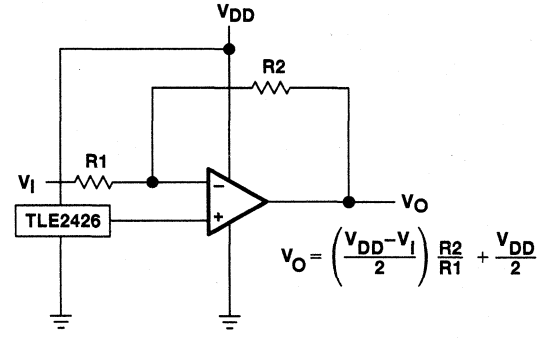


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2334 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

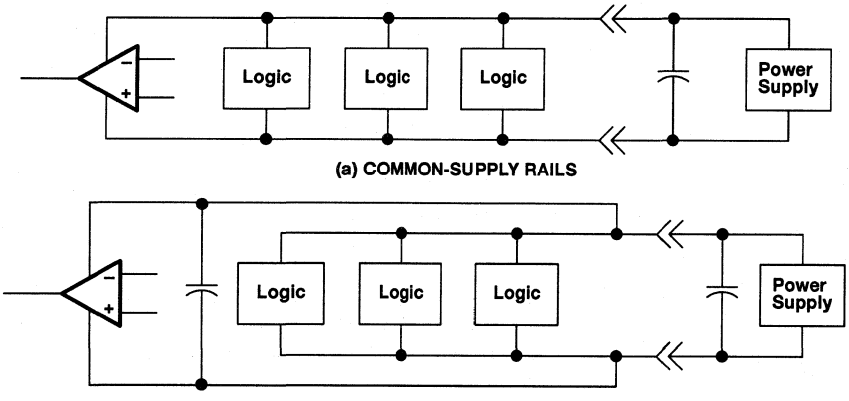


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2334 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD} –1.2 V at all other temperatures.

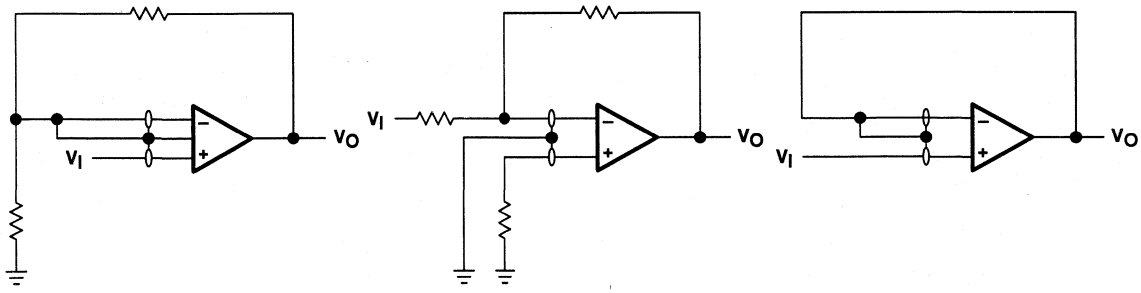
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2334 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2334 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level at the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2334 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

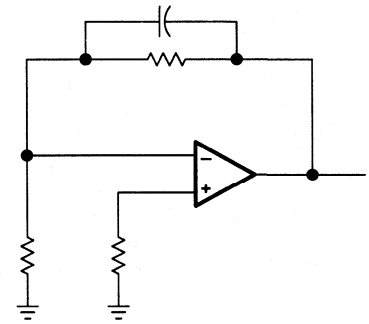


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2334 incorporates an internal electro-static-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2334 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal-protection diodes

APPLICATION INFORMATION

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2334 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2334 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

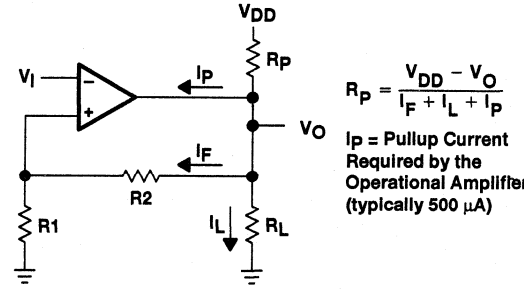


Figure 39. Resistive Pullup to Increase V_{OH}

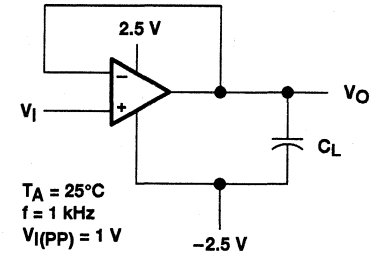
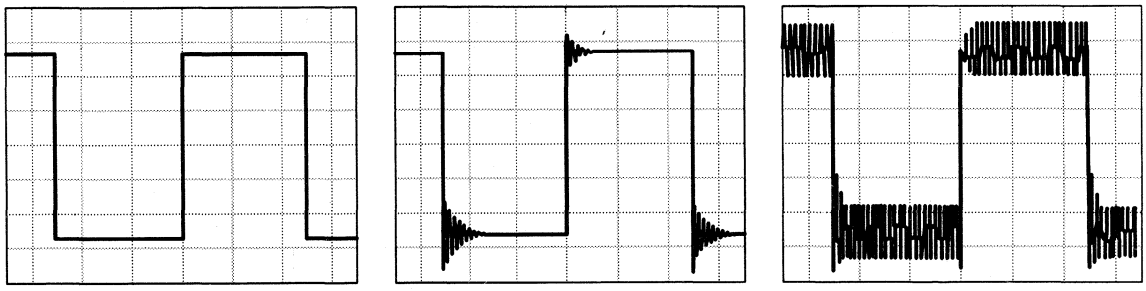


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2334 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

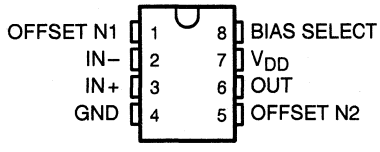
(b) C_L = 170 pF, R_L = NO LOAD

(c) C_L = 190 pF, R_L = NO LOAD

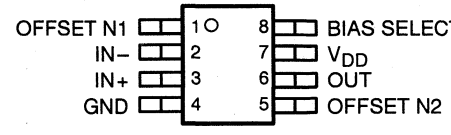
Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Low Noise . . . 25 nV/√Hz Typically at f = 1 kHz (High-Bias Mode)**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**
- **Bias-Select Feature Enables Maximum Supply Current Range From 17 μA to 1.5 mA at 25°C**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

The TLV2341 operational amplifier has been specifically developed for low-voltage, single-supply applications and is fully specified to operate over a voltage range of 2 V to 8 V. The device uses the Texas Instruments silicon-gate LinCMOS™ technology to facilitate low-power, low-voltage operation and excellent offset-voltage stability. LinCMOS™ technology also enables extremely high input impedance and low bias currents allowing direct interface to high-impedance sources.

The TLV2341 offers a bias-select feature, which allows the device to be programmed with a wide range of different supply currents and therefore different levels of ac performance. The supply current can be set at 17 μA, 250 μA, or 1.5 mA, which results in slew-rate specifications between 0.02 and 2.1 V/μs (at 3 V).

The TLV2341 operational amplifiers are especially well suited to single-supply applications and are fully specified and characterized at 3-V and 5-V power supplies. This low-voltage single-supply operation combined with low power consumption makes this device a good choice for remote, inaccessible, or portable battery-powered applications. The common-mode input range includes the negative rail.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2341 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD 883 C, Methods 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	8 mV	TLV2341ID	TLV2341IP	TLV2341IPWLE	TLV2341Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2341IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2341IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

bias-select feature

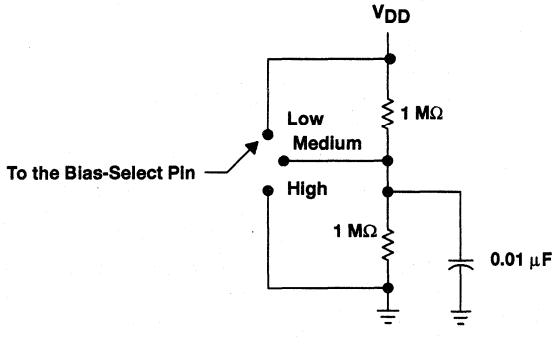
The TLV2342 offers a bias-select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The tradeoffs between bias levels involve ac performance and power dissipation (see Table 1).

Table 1. Effect of Bias Selection on Performance

TYPICAL PARAMETER VALUES T_A = 25°C, V_{DD} = 3 V		MODE			UNIT
		HIGH BIAS R_L = 10 kΩ	MEDIUM BIAS R_L = 100 kΩ	LOW BIAS R_L = 1 MΩ	
P_D	Power dissipation	975	195	15	μW
SR	Slew rate	2.1	0.38	0.02	V/μs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	790	300	27	kHz
ϕ_m	Phase margin	46°	39°	34°	
A_{VD}	Large-signal differential voltage amplification	11	83	400	V/mV

bias selection

Bias selection is achieved by connecting BIAS SELECT to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS-SELECT VOLTAGE (single supply)
Low	V_{DD}
Medium	1 V to V_{DD} – 1 V
High	GND

Figure 1. Bias Selection for Single-Supply Applications

high-bias mode

In the high-bias mode, the TLV2341 series feature low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices but at only a fraction of the power dissipation.

medium-bias mode

The TLV2341 in the medium-bias mode features a low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

In the low-bias mode, the TLV2341 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

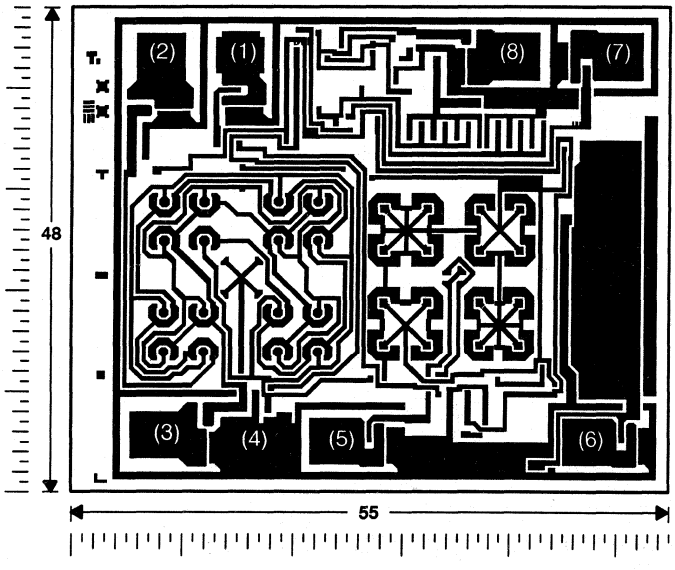
ORDER OF CONTENTS

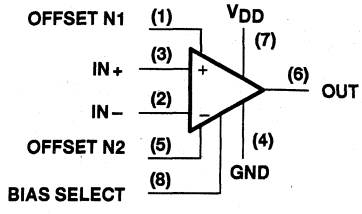
TOPIC	BIAS MODE
Schematic	all
Absolute maximum ratings	all
Recommended operating conditions	all
Electrical characteristics Operating characteristics Typical characteristics	high (Figures 2 – 31)
Electrical characteristics Operating characteristics Typical characteristics	medium (Figures 32 – 61)
Electrical characteristics Operating characteristics Typical characteristics	low (Figures 62 – 91)
Parameter measurement information	all
Application information	all

TLV2341Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2341. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

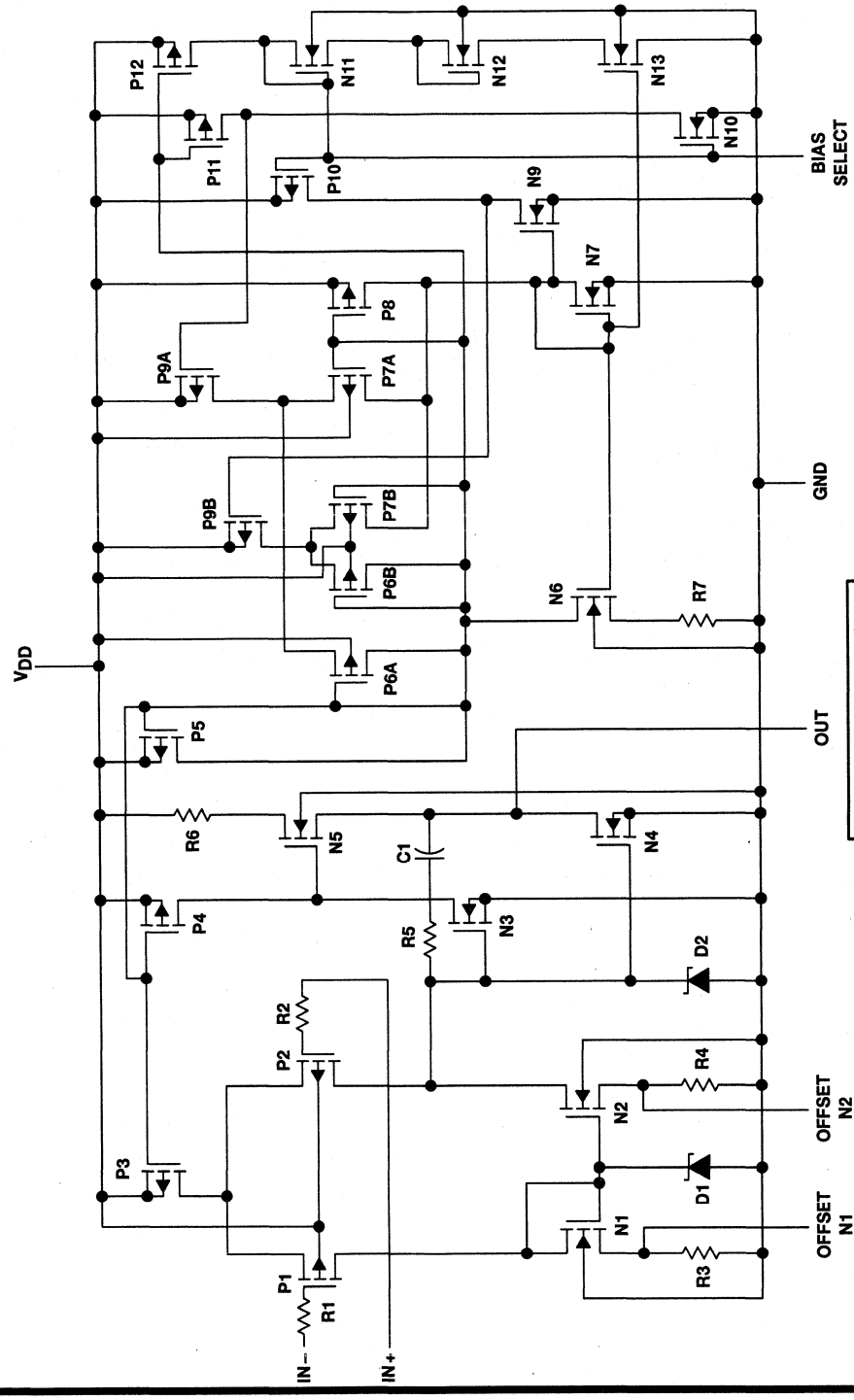
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic



COMPONENT COUNT†	
Transistors	27
Diodes	2
Resistors	7
Capacitors	1

† Includes the amplifier and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2341I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		−1.2			−1.4		μA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		325	1500		675	1600	μA
			Full range			2000			2200	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

HIGH-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, See Figure 92	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = kHz, See Figure 93	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 92	25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 94	25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 1 MΩ,	−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 92	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 93	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 92	25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 94	25°C		1.7		MHz
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 10 kΩ,	−40°C		49°		
				25°C		46°		
				85°C		43°		

HIGH-BIAS MODE

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2341I						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		50	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	95		70	95		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0		−1.2			−1.4		μA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		325	1500		675	1600	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2,3
α_{VIO}	Input offset voltage temperature coefficient	Distribution	4,5
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	6 7 8
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	9 10, 12 11 13
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature vs Frequency	14 15 26, 27
I_{IB}	Input bias current	vs Temperature	16
I_{IO}	Input offset current	vs Temperature	16
V_{IC}	Common-mode input voltage	vs Supply voltage	17
I_{DD}	Supply current	vs Supply voltage vs Temperature	18 19
SR	Slew rate	vs Supply voltage vs Temperature	20 21
	Bias select current	vs Supply voltage	22
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	23
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	24 25
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	28 29 30
V_n	Equivalent input noise voltage	vs Frequency	31
	Phase shift	vs Frequency	26, 27

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

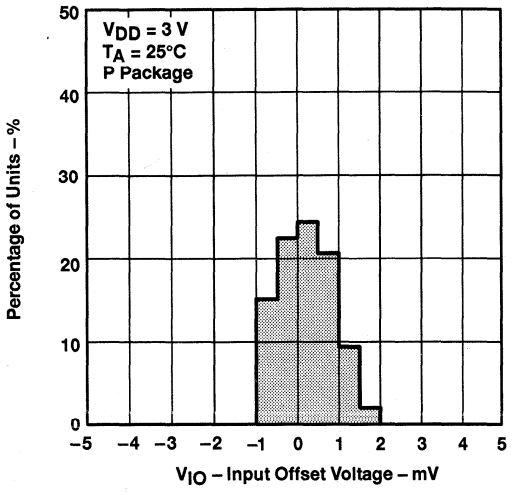


Figure 2

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

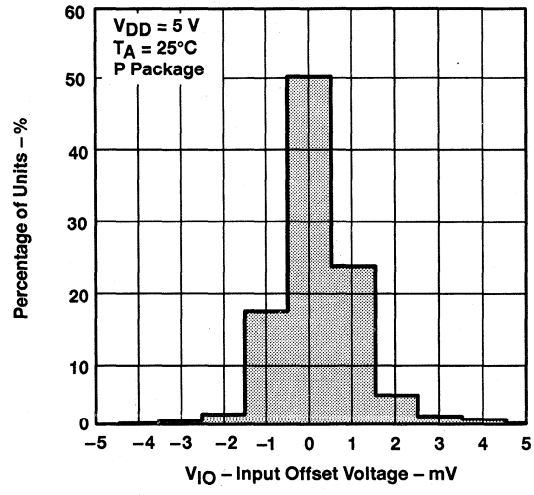


Figure 3

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

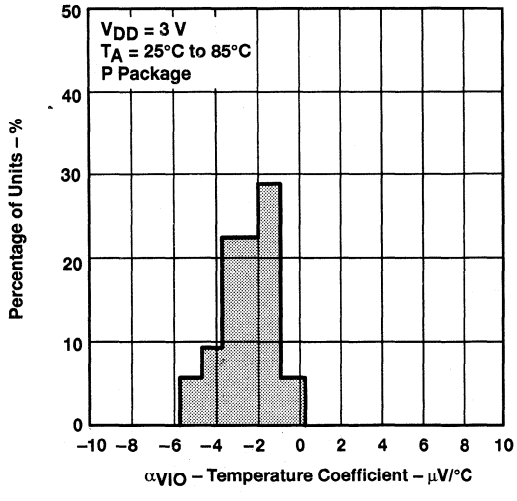


Figure 4

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

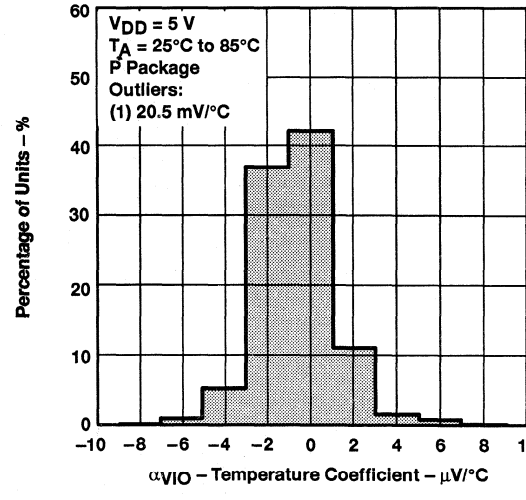


Figure 5

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

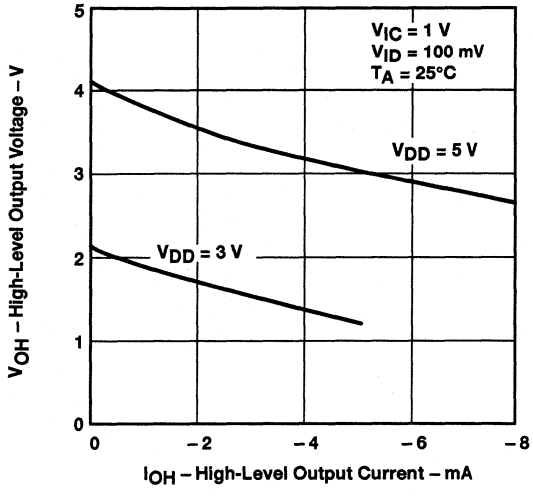


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

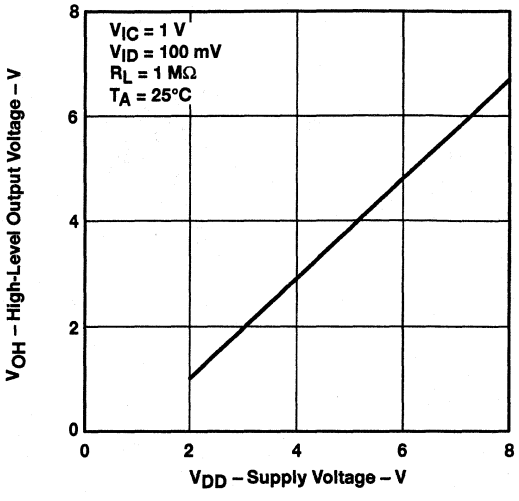


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

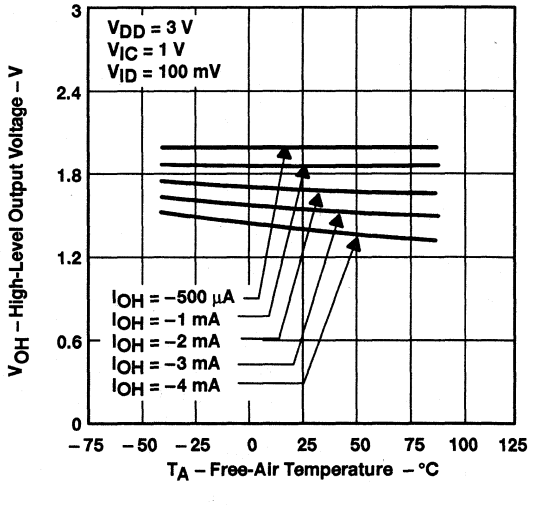


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

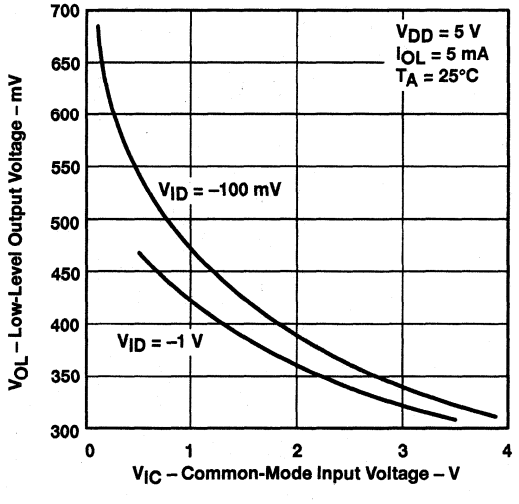


Figure 9

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

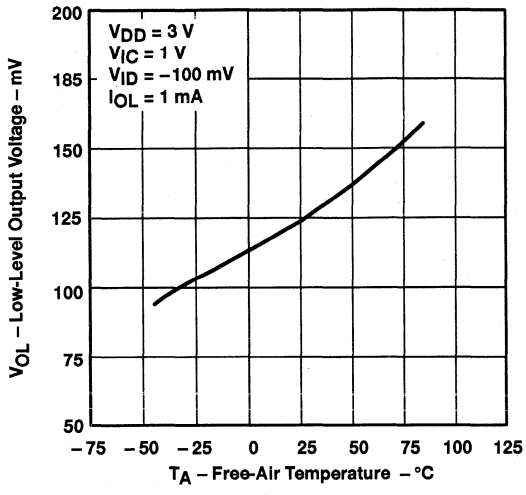


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

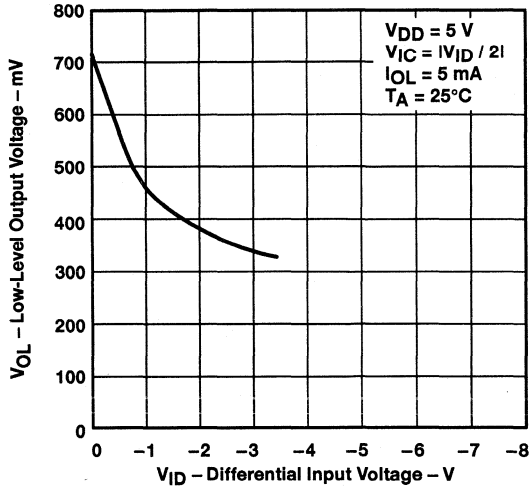


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

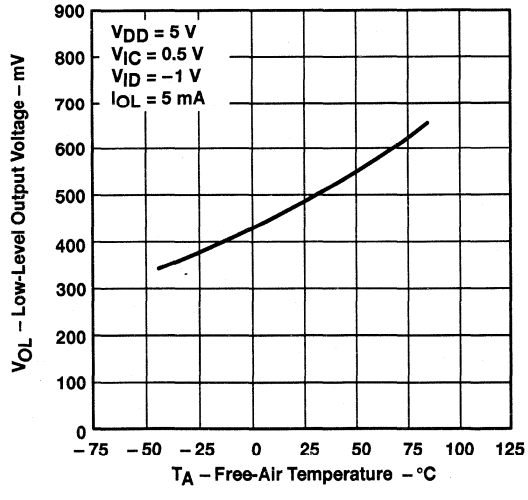


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

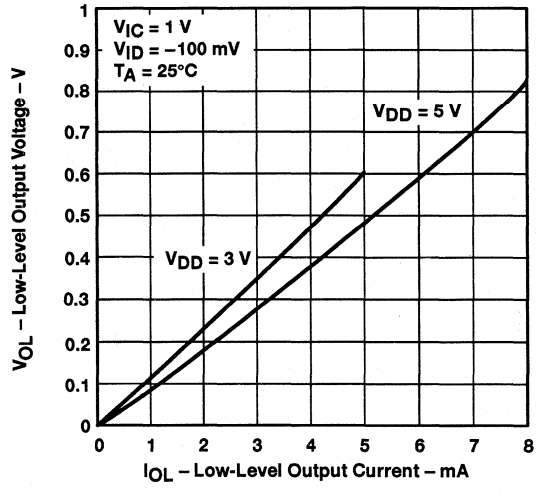


Figure 13

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

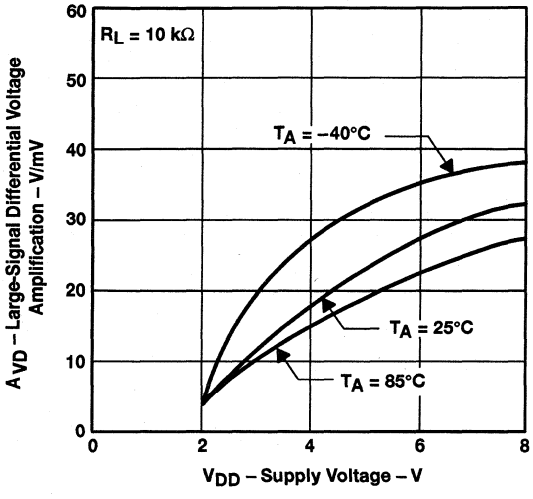


Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

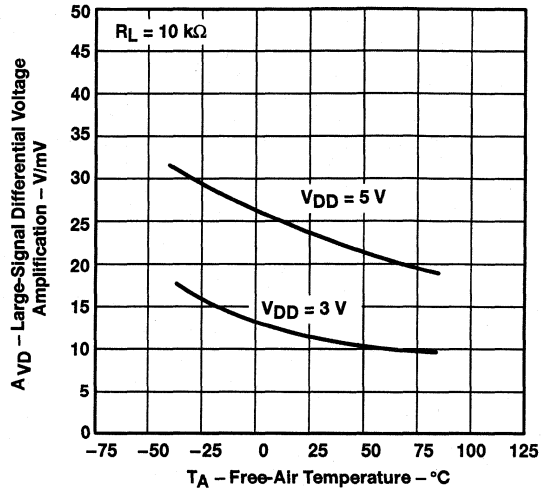
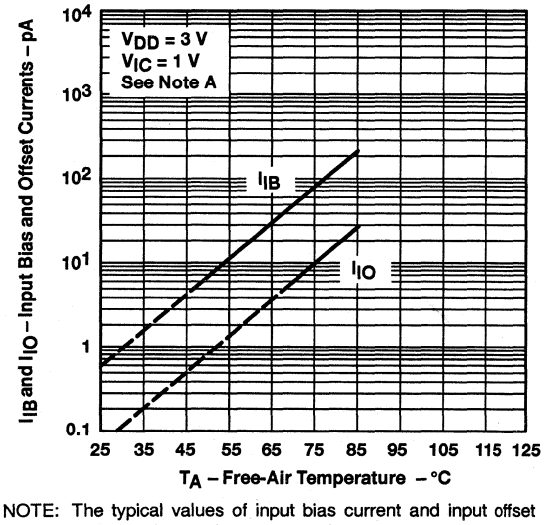


Figure 15

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 16

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

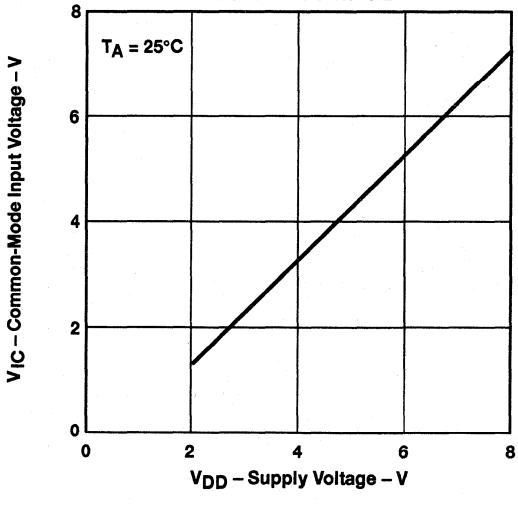


Figure 17

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

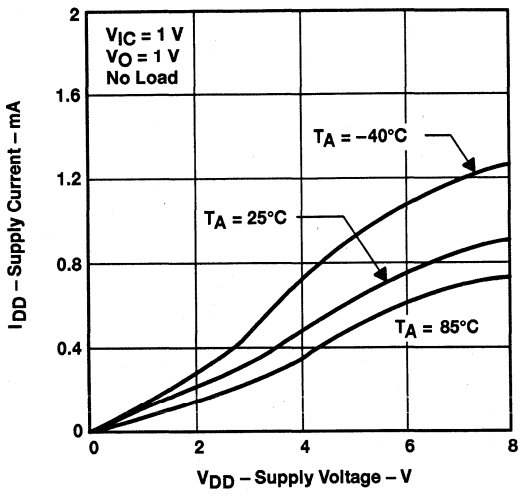


Figure 18

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

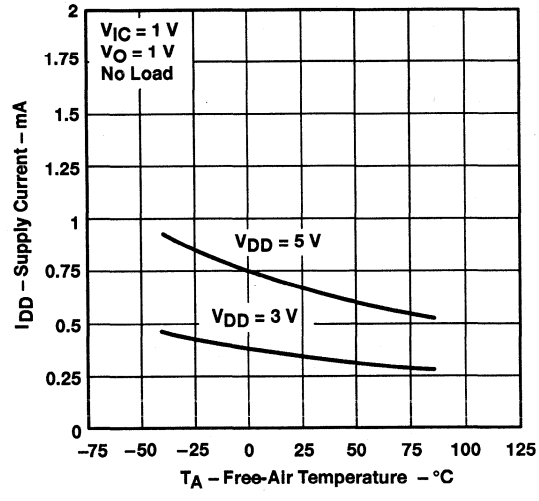


Figure 19

SLEW RATE
vs
SUPPLY VOLTAGE

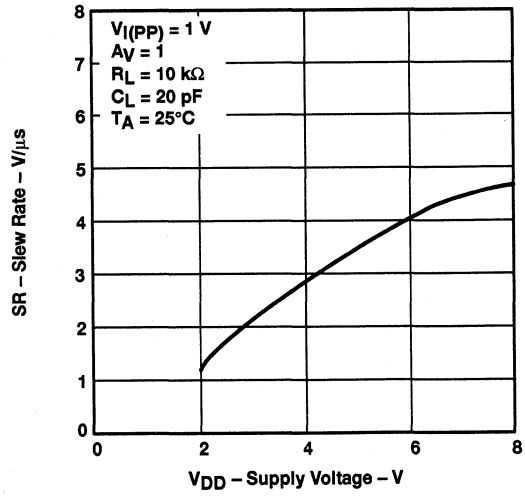


Figure 20

SLEW RATE
vs
FREE-AIR TEMPERATURE

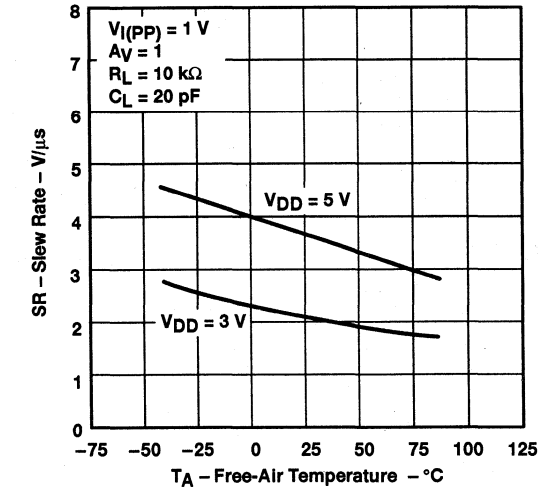


Figure 21

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

BIAS SELECT CURRENT vs SUPPLY VOLTAGE

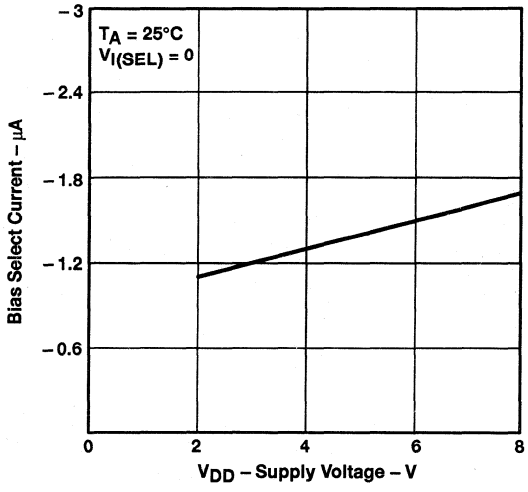


Figure 22

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

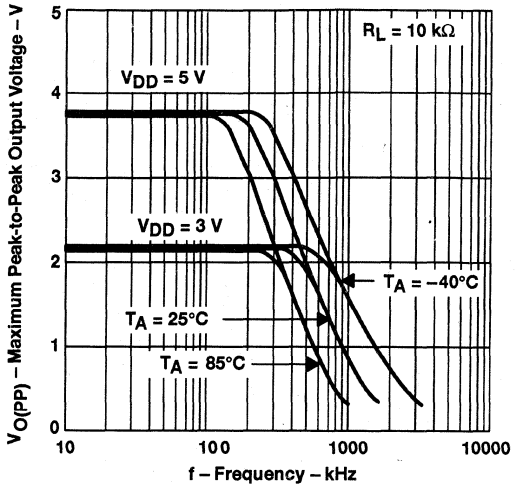


Figure 23

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

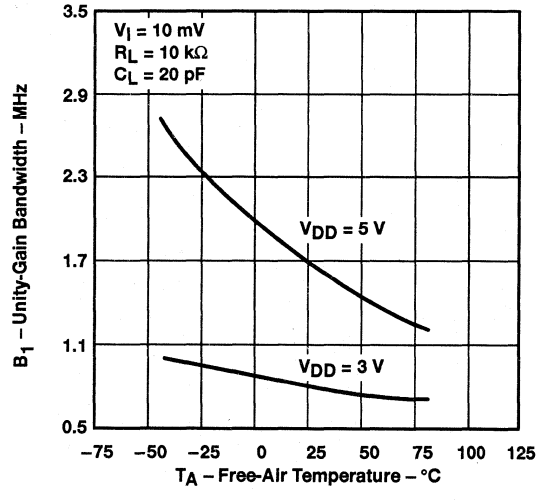


Figure 24

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

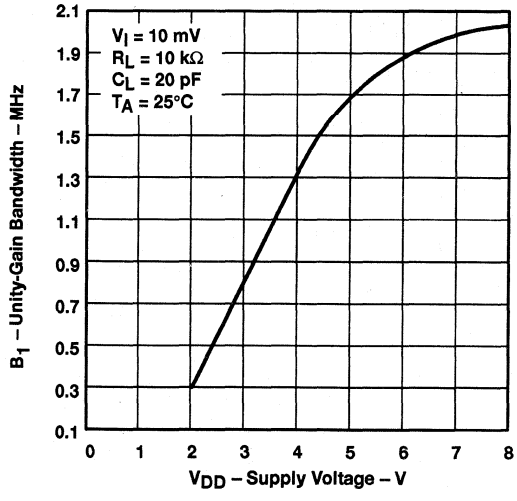


Figure 25

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

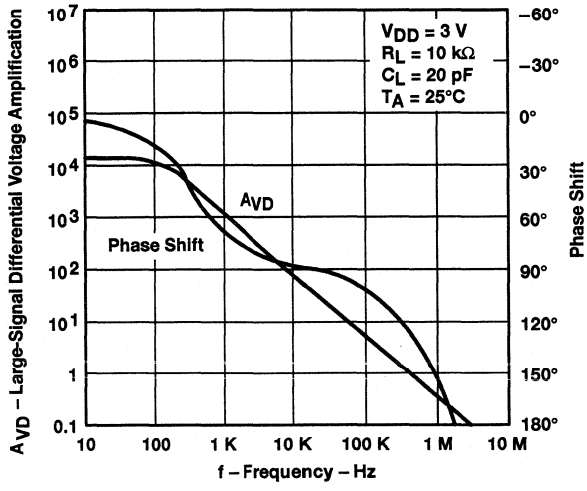


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

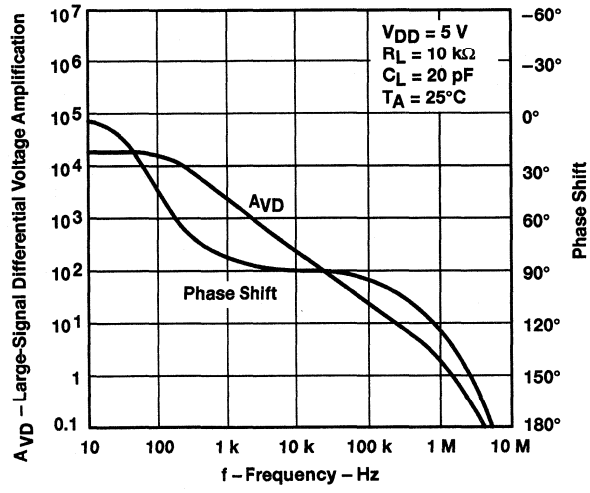


Figure 27

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

PHASE MARGIN vs SUPPLY VOLTAGE

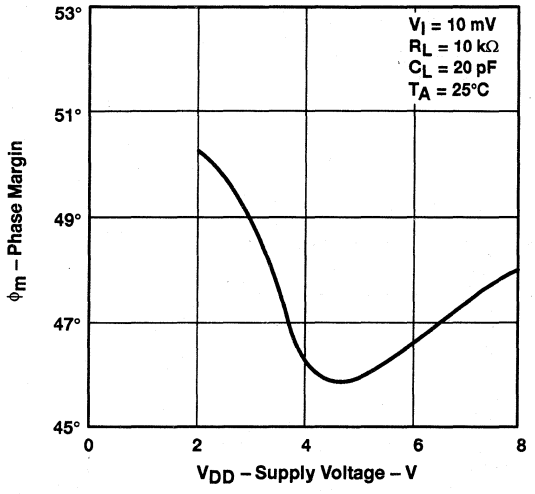


Figure 28

PHASE MARGIN vs FREE-AIR TEMPERATURE

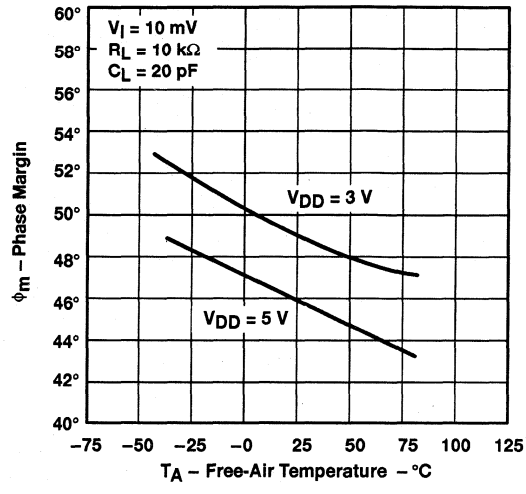


Figure 29

PHASE MARGIN vs LOAD CAPACITANCE

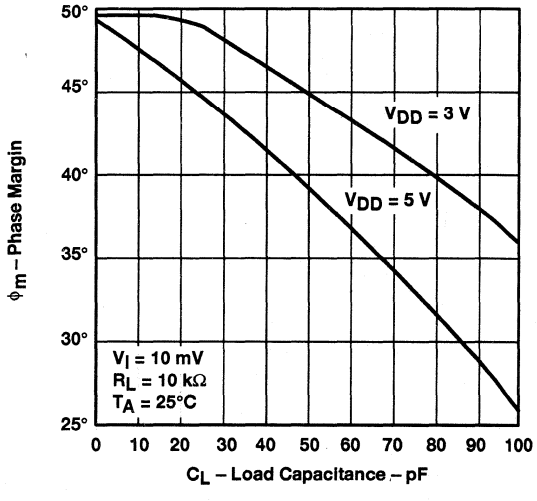


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

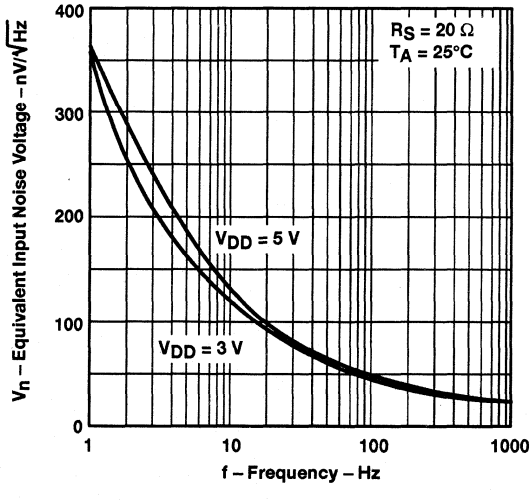


Figure 31

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2341I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		−100			−130		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		65	250		105	280	μA
			Full range			360			400	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, See Figure 92	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = kHz, See Figure 93	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 92	25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 94	25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 100 kΩ,	−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 92	$V_{I(PP)}$ = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			$V_{I(PP)}$ = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f =1 kHz, See Figure 93	R_S = 20 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 92	25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 100 kΩ,	C_L = 20 pF, See Figure 94	25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 100 kΩ,	−40°C		43°		
				25°C		40°		
				85°C		38°		

MEDIUM-BIAS MODE

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2341I						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	94		70	94		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0		−100			−130		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		65	250		105	280	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

Table of Graphs

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α_{VIO}	Input offset voltage temperature coefficient	Distribution	34, 35
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	36 37 38
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	39 40, 42 41 43
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SR	Slew rate	vs Supply voltage vs Temperature	50 51
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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	53
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	54 55
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	58 59 60
V_n	Equivalent input noise voltage	vs Frequency	61
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TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

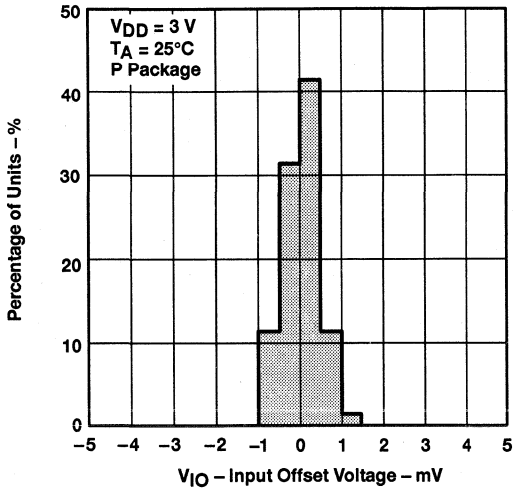


Figure 32

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

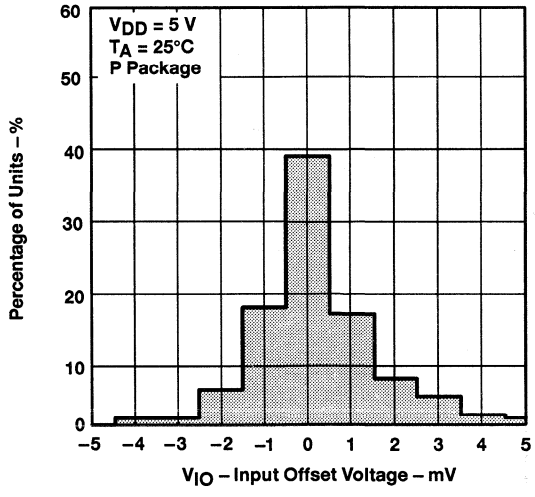


Figure 33

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

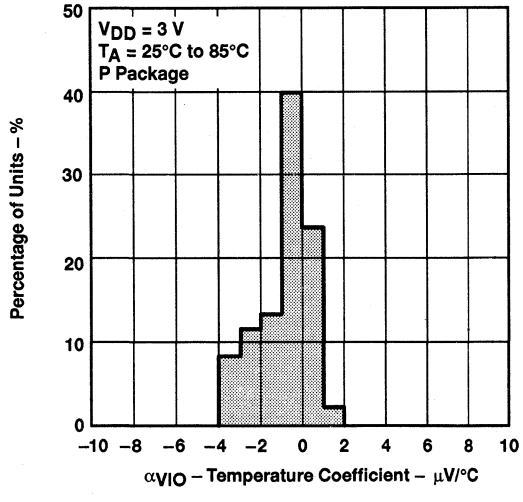


Figure 34

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

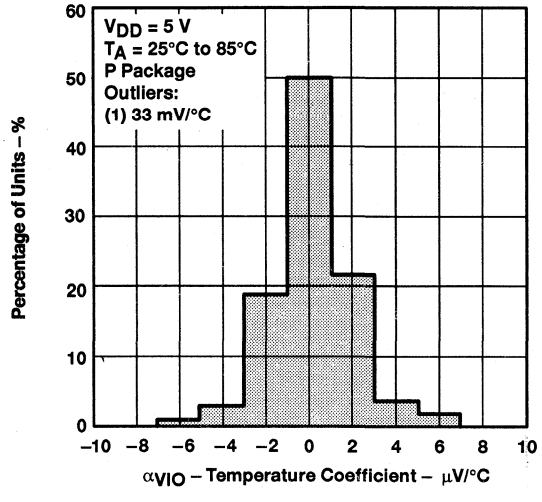


Figure 35

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

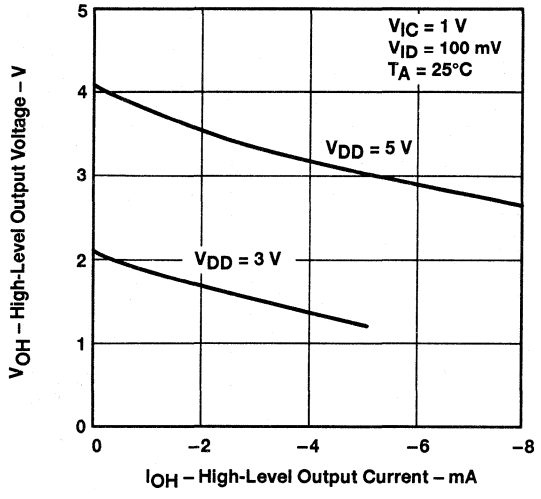


Figure 36

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

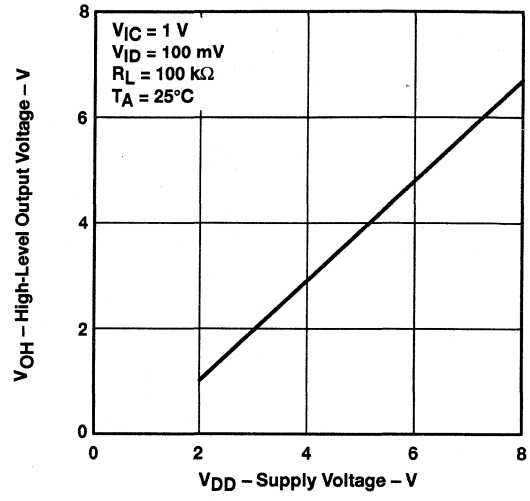


Figure 37

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

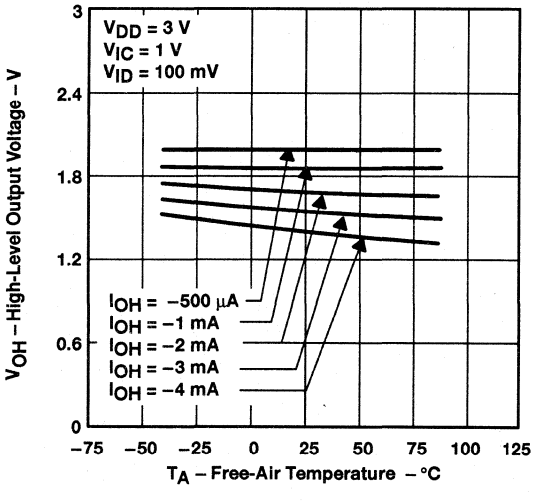


Figure 38

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

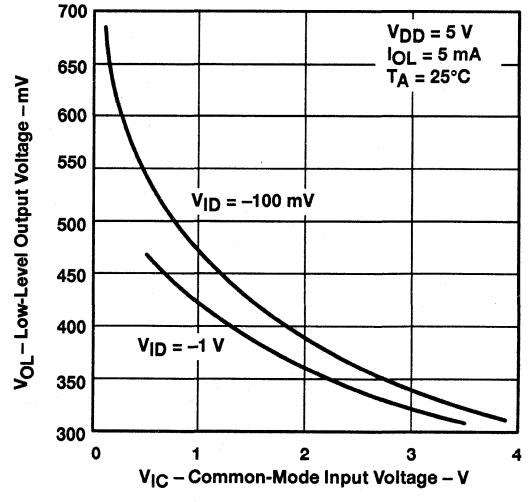


Figure 39

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

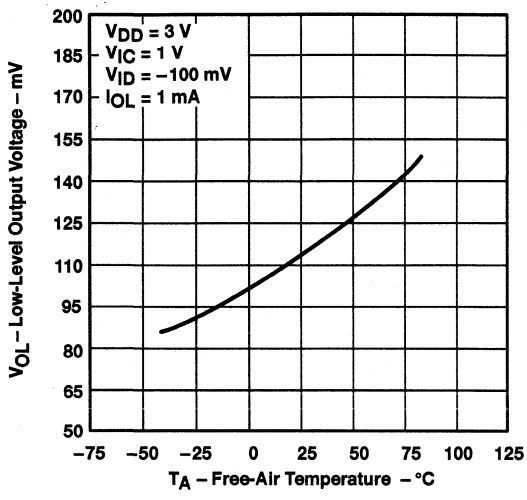


Figure 40

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

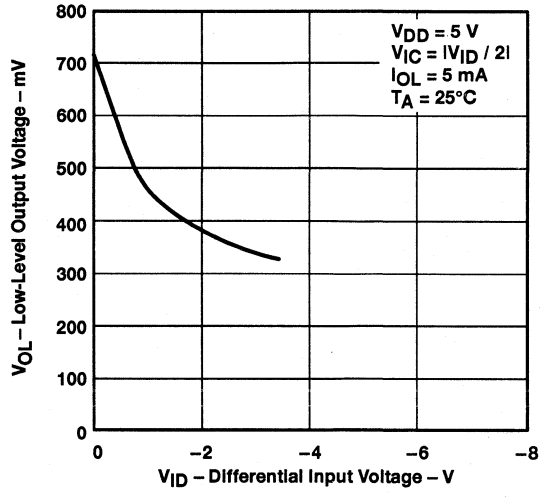


Figure 41

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

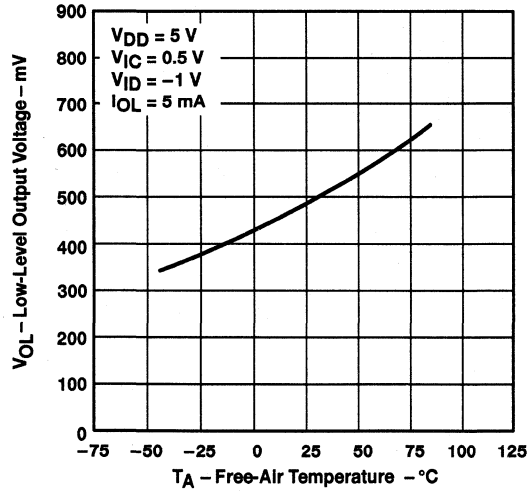


Figure 42

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

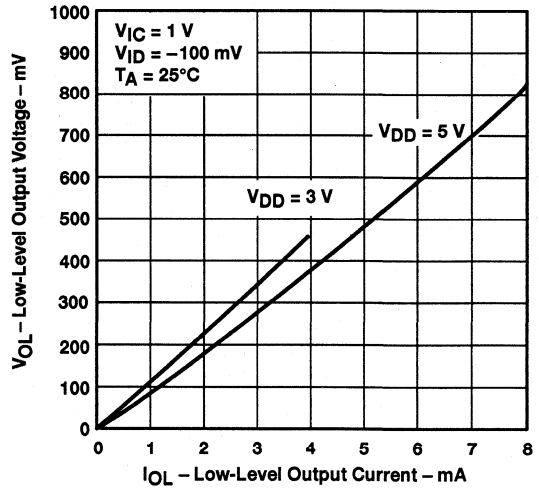


Figure 43

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

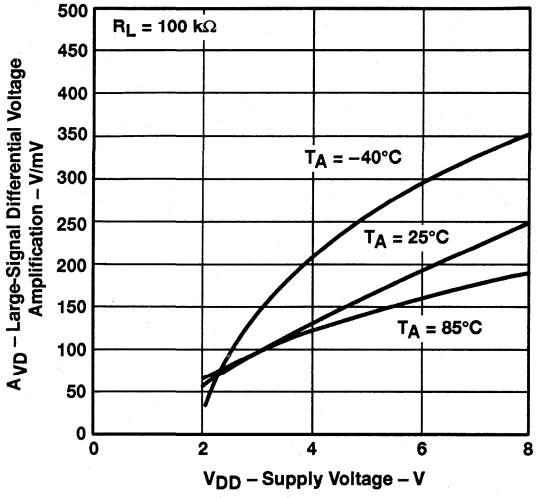


Figure 44

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

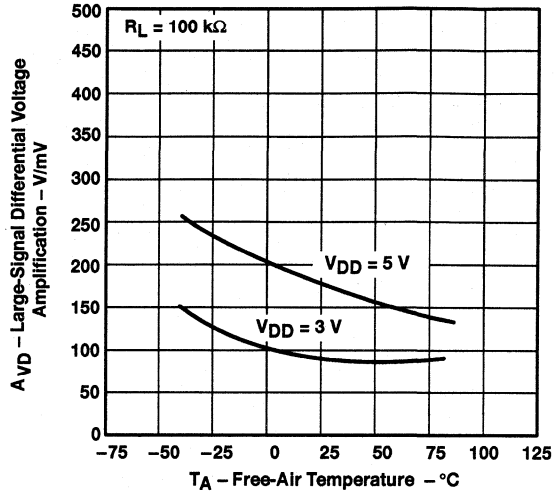
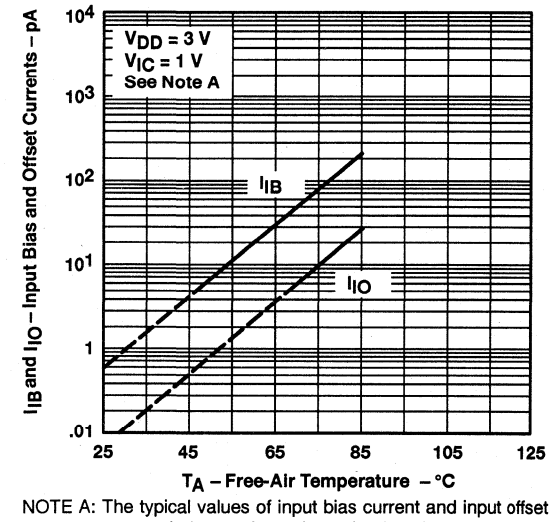


Figure 45

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

Figure 46

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

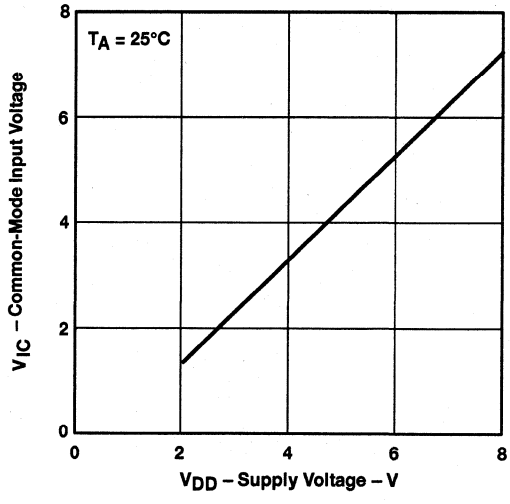


Figure 47

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

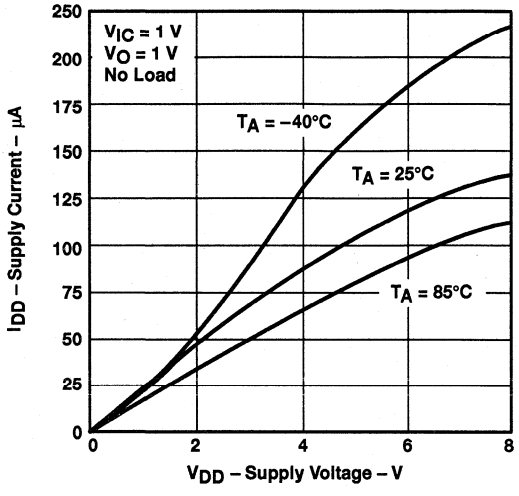


Figure 48

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

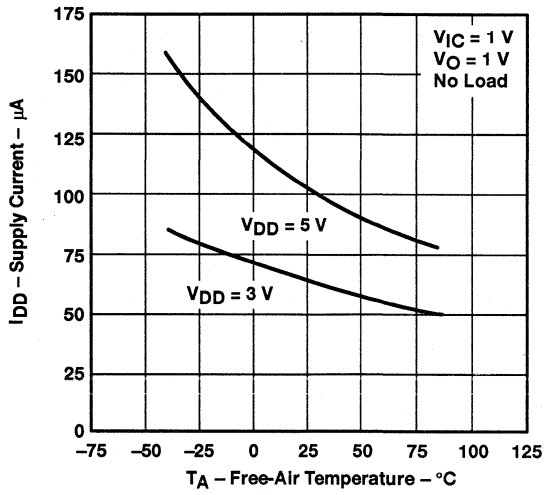


Figure 49

SLEW RATE
vs
SUPPLY VOLTAGE

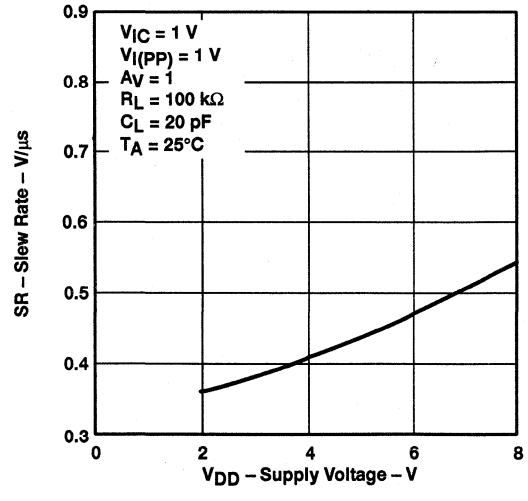


Figure 50

SLEW RATE
vs
FREE-AIR TEMPERATURE

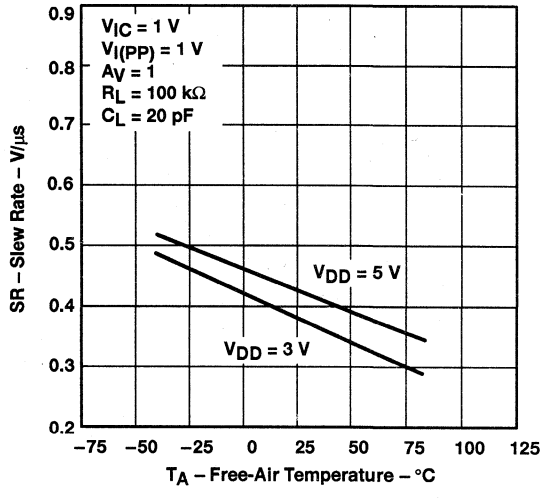


Figure 51

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

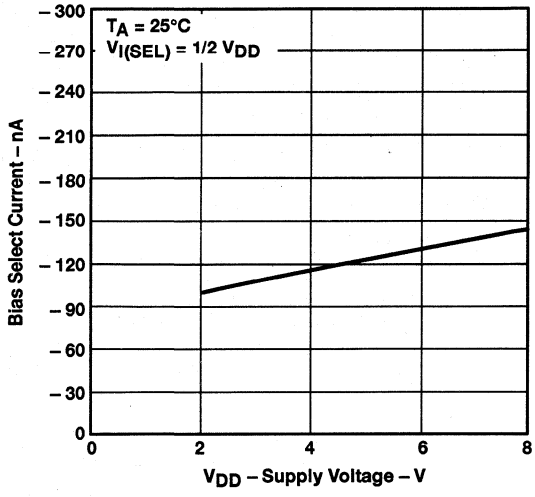


Figure 52

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

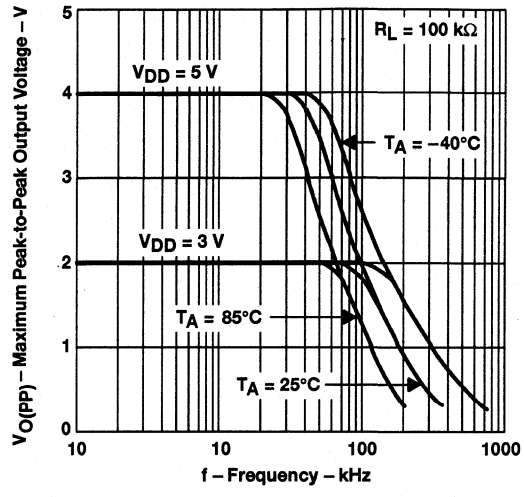


Figure 53

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

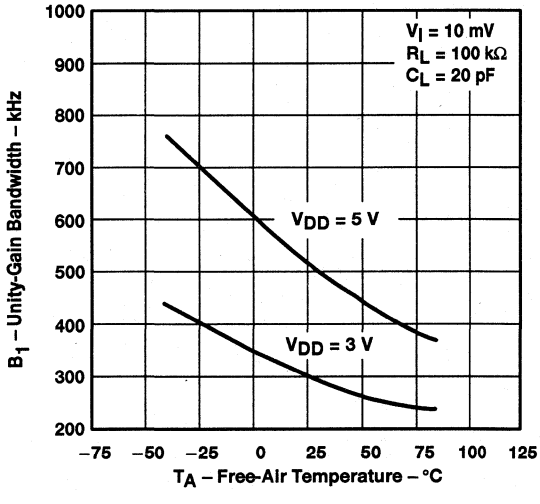


Figure 54

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

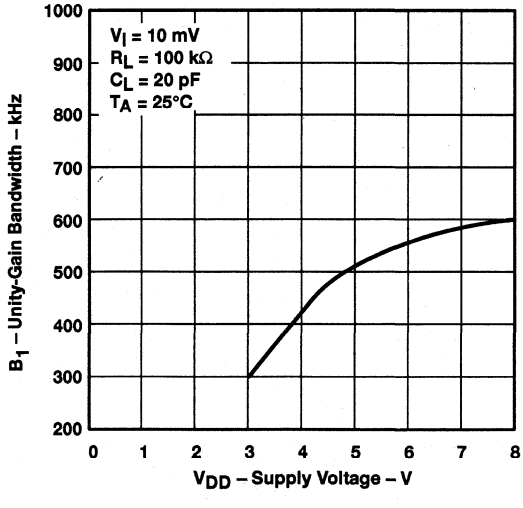


Figure 55

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

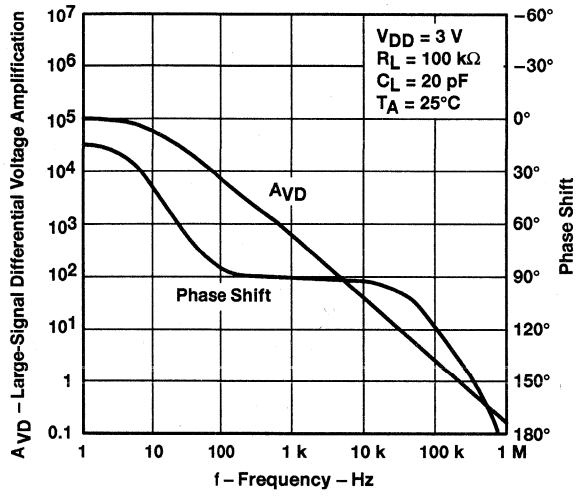


Figure 56

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

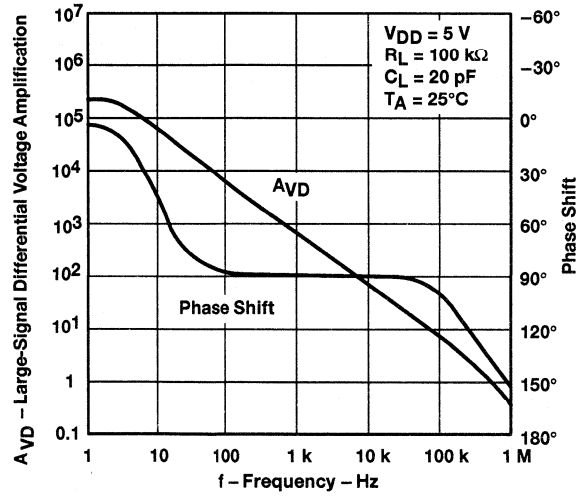


Figure 57

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

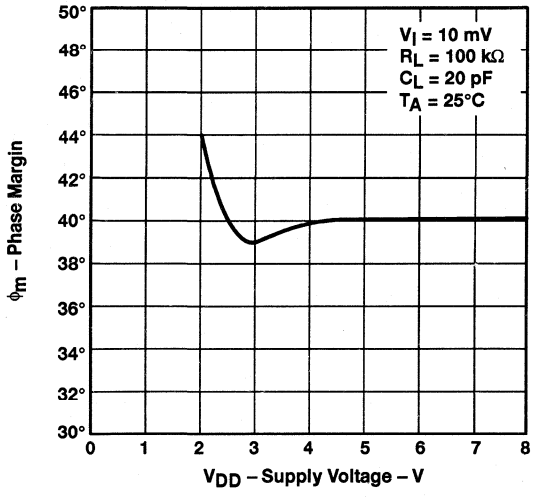


Figure 58

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

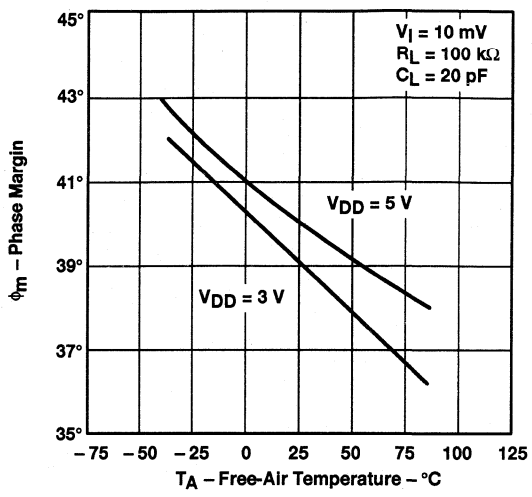


Figure 59

PHASE MARGIN
vs
LOAD CAPACITANCE

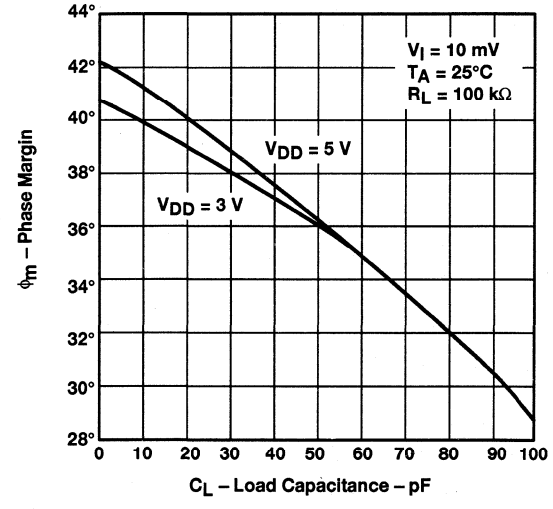


Figure 60

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

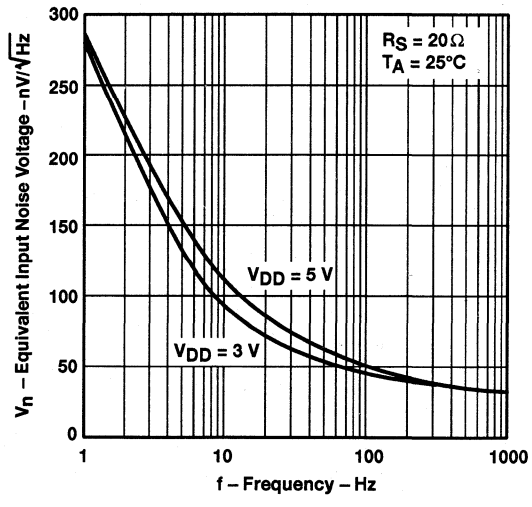


Figure 61

LOW-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2341I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		10			65		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		5	17		10	17	μA
			Full range			27			27	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

LOW-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 92	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = kHz, See Figure 93	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 92	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 94	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2341I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 92	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f =1 kHz, See Figure 93	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 92	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 94	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 94	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

LOW-BIAS MODE

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2341Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 1 MΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = −1 mA	V_{ID} = 100 mV,	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = −100 mV,		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 1 MΩ,	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_{DD} = 3 V to 5 V, V_O = 1 V,	V_{IC} = 1 V, R_S = 50 Ω	70	86		70	86		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0			10			65		nA
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		5	17		10	17	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	62, 63
α_{VIO}	Input offset voltage temperature coefficient	Distribution	64, 65
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	66 67 68
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	69 70, 72 71 73
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature vs Frequency	74 75 86, 87
I_{IB}	Input bias current	vs Temperature	76
I_{IO}	Input offset current	vs Temperature	76
V_{IC}	Common-mode input voltage	vs Supply voltage	77
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SR	Slew rate	vs Supply voltage vs Temperature	80 81
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$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	83
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ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	88 89 90
V_n	Equivalent input noise voltage	vs Frequency	91
	Phase shift	vs Frequency	86, 87

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

**DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE**

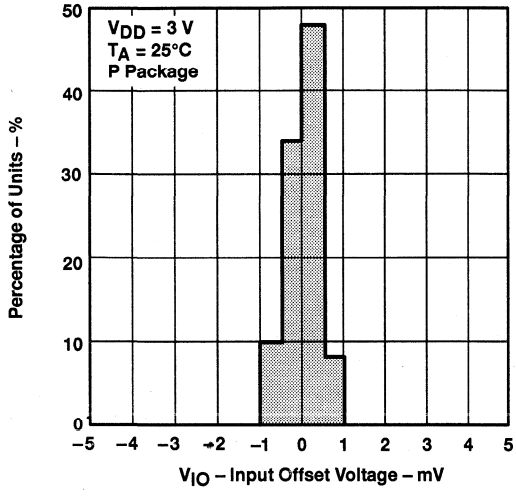


Figure 62

**DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE**

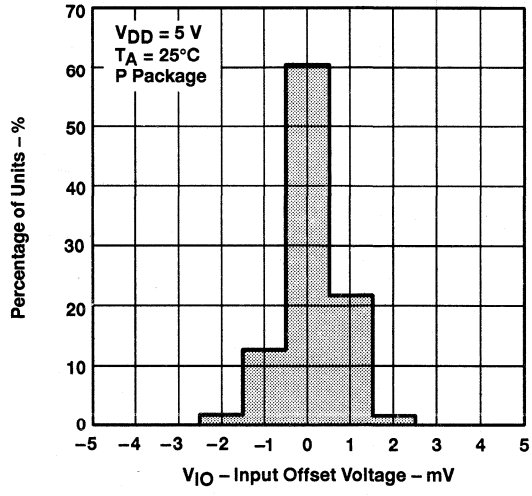


Figure 63

**DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

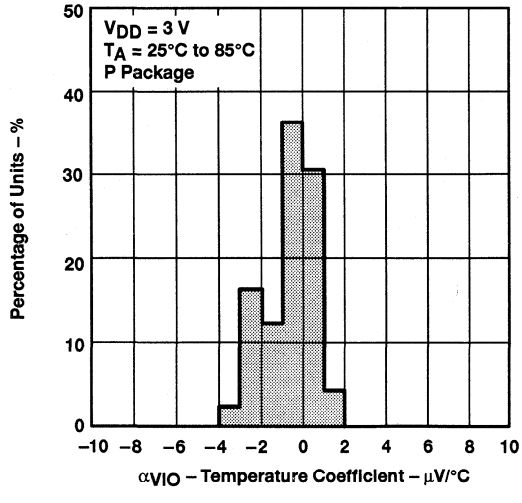


Figure 64

**DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

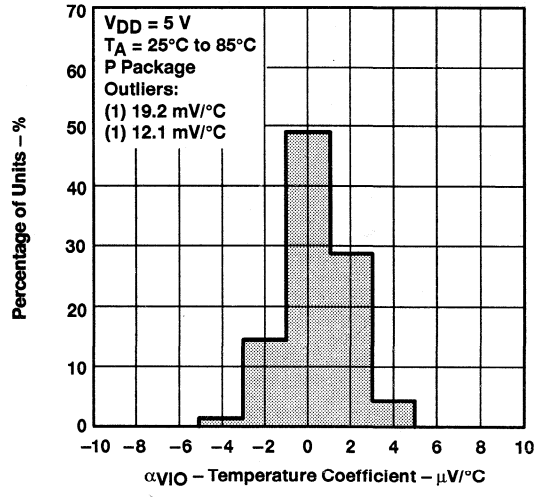


Figure 65

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

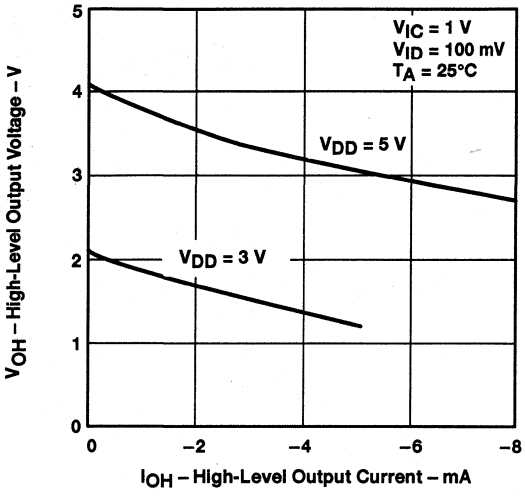


Figure 66

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

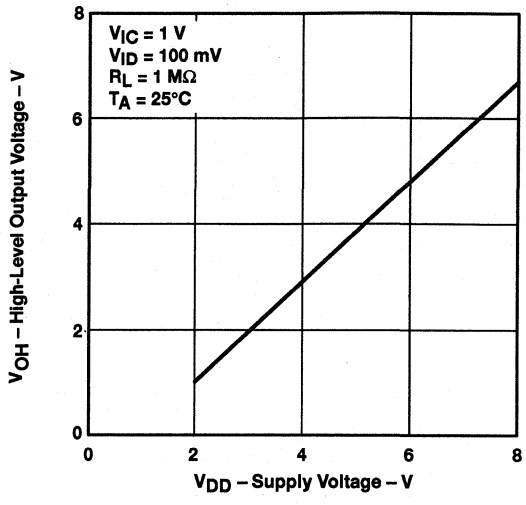


Figure 67

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

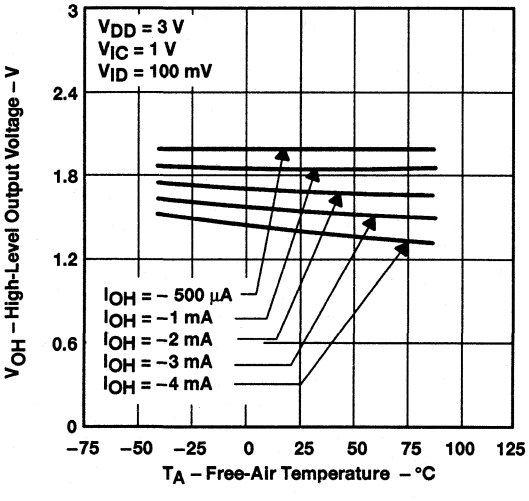


Figure 68

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

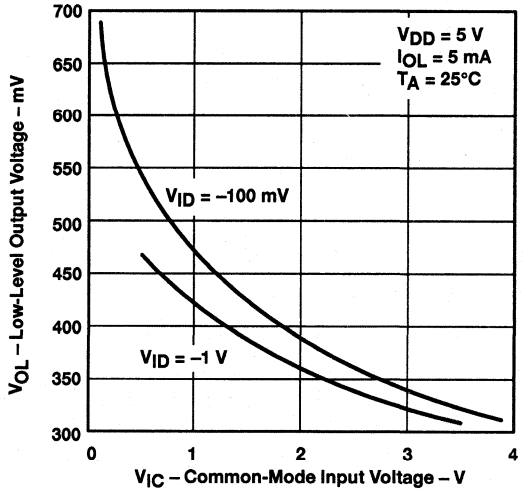


Figure 69

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

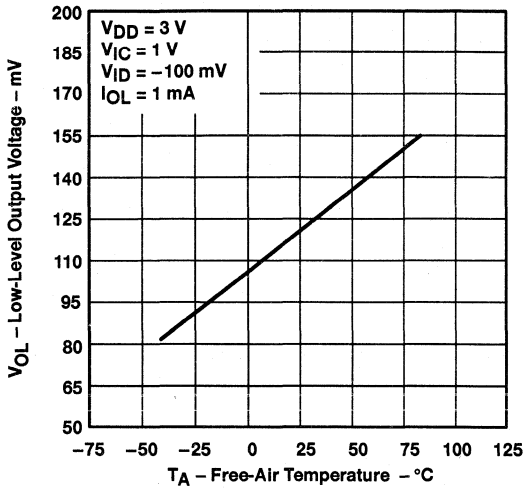


Figure 70

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

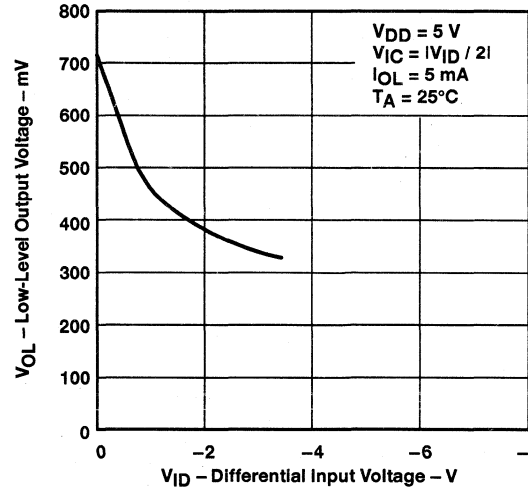


Figure 71

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

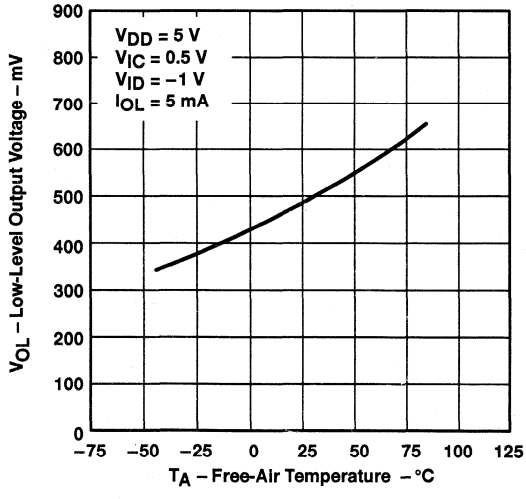


Figure 72

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

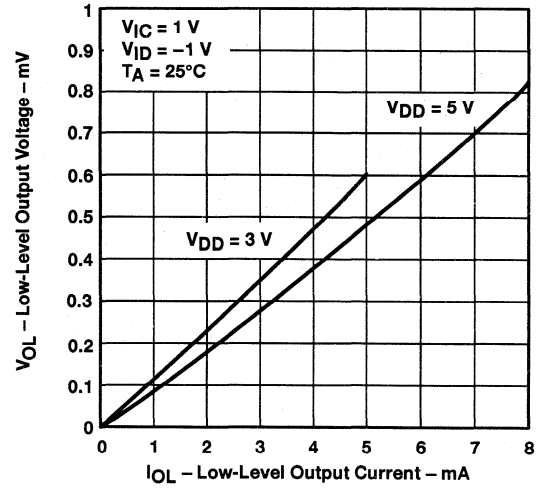


Figure 73

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

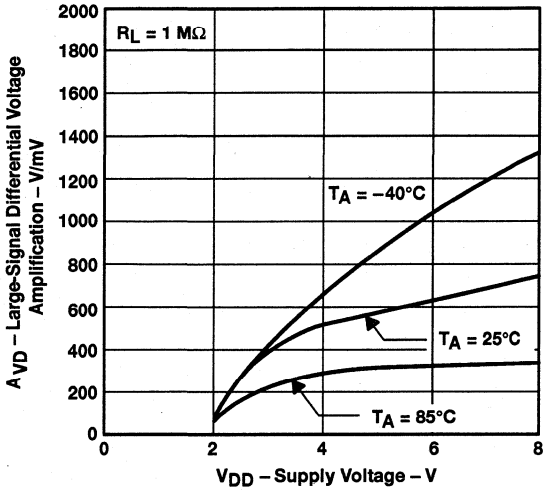


Figure 74

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

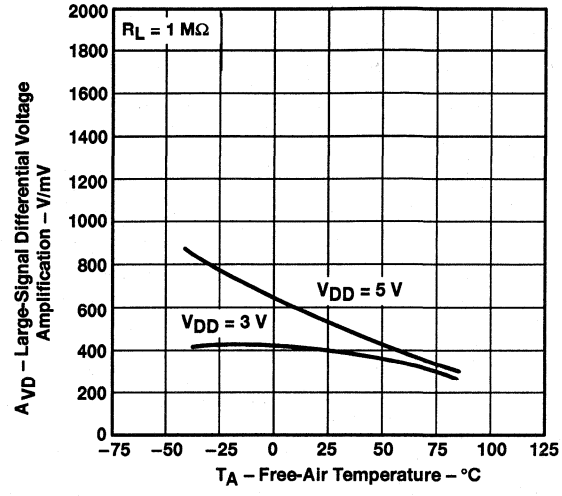
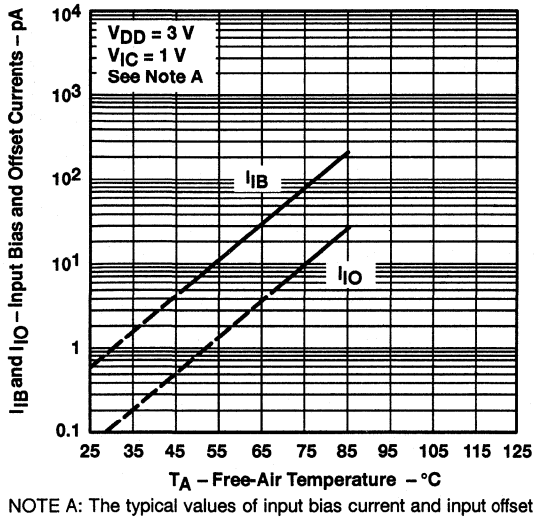


Figure 75

INPUT BIAS CURRENT AND INPUT OFFSET
CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA are determined mathematically.

Figure 76

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

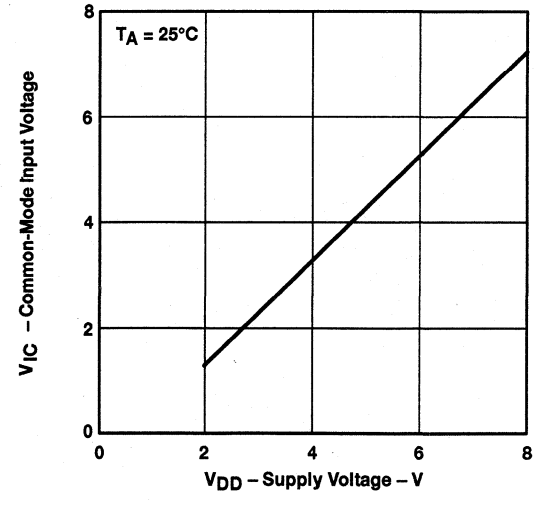


Figure 77

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

SUPPLY CURRENT vs SUPPLY VOLTAGE

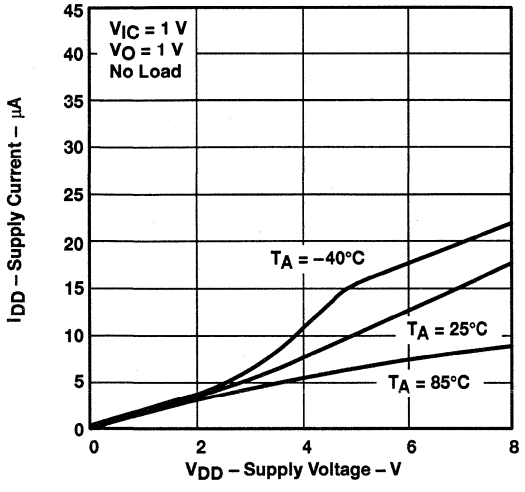


Figure 78

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

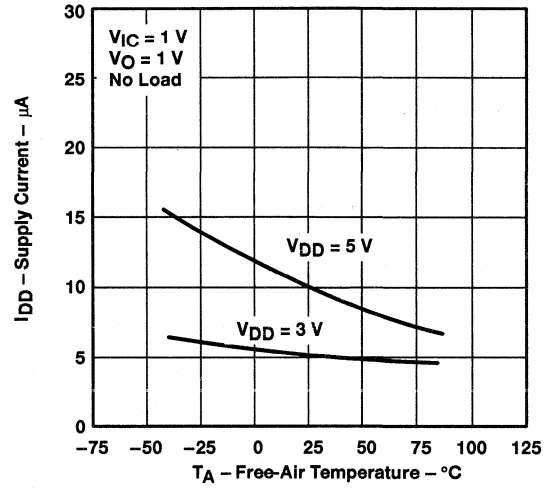


Figure 79

SLEW RATE vs SUPPLY VOLTAGE

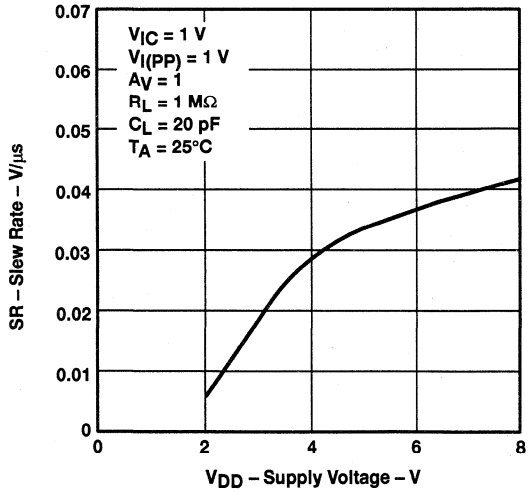


Figure 80

SLEW RATE vs FREE-AIR TEMPERATURE

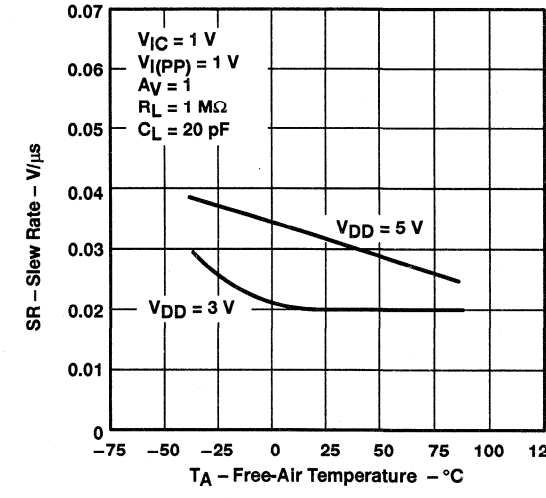


Figure 81

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

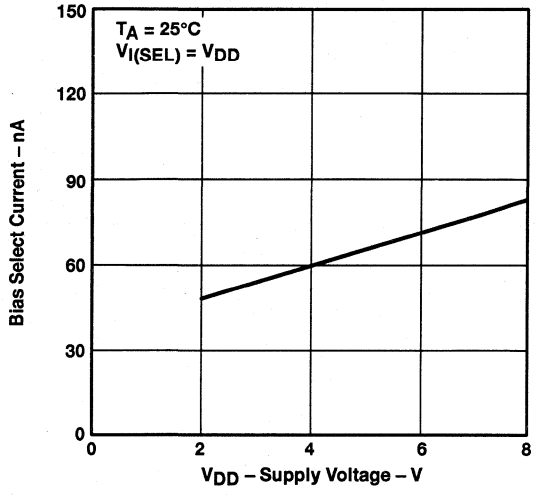


Figure 82

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

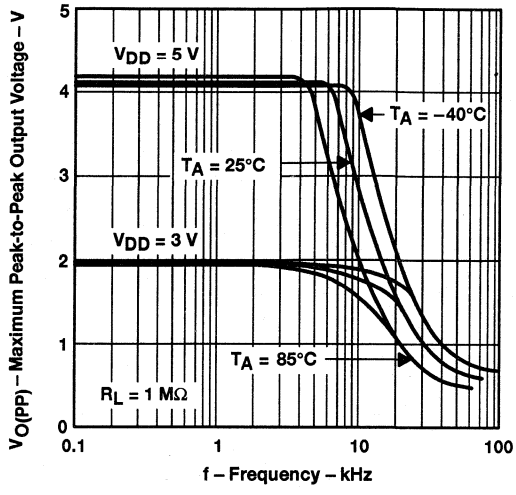


Figure 83

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

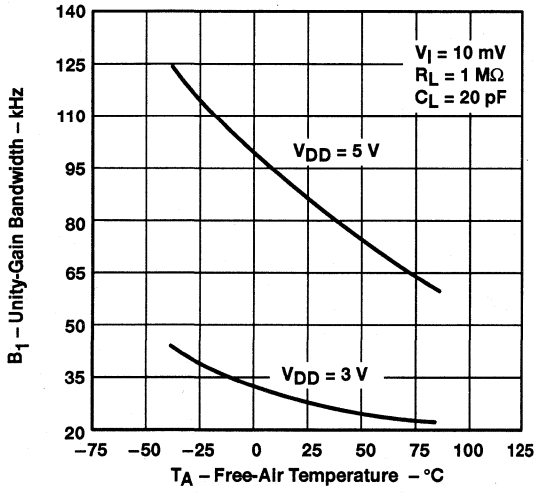


Figure 84

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

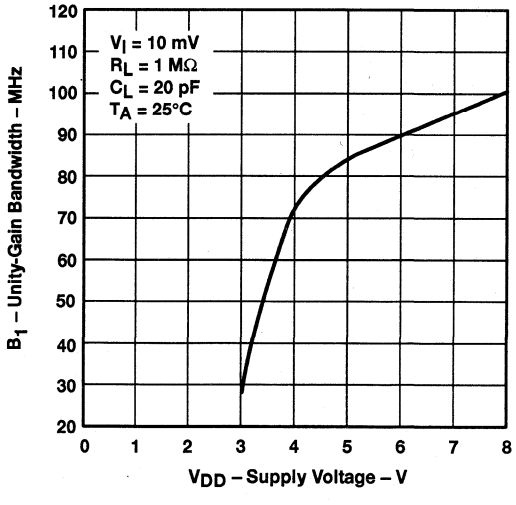


Figure 85

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

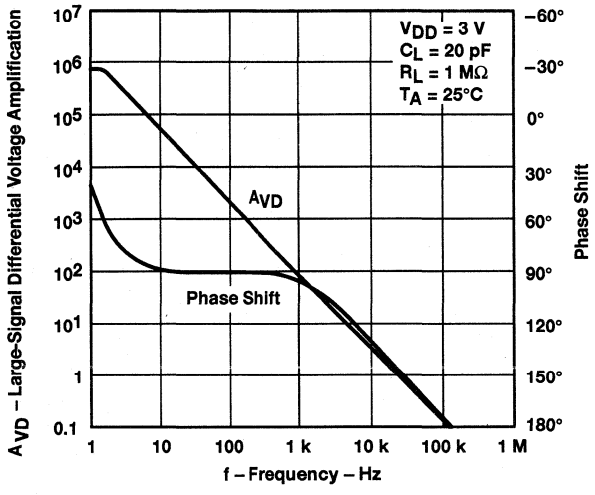


Figure 86

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

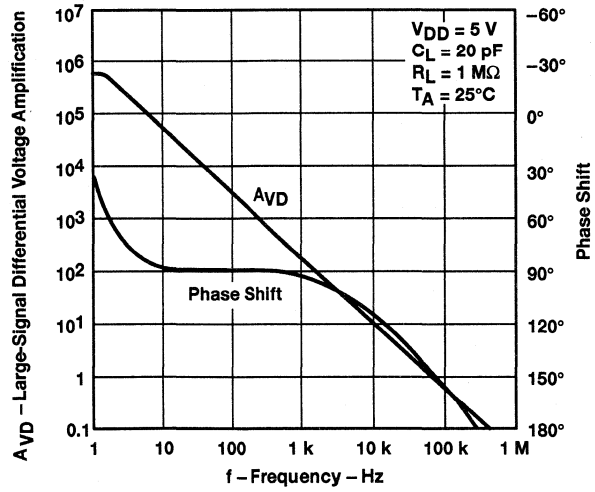


Figure 87

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

PHASE MARGIN
vs
SUPPLY VOLTAGE

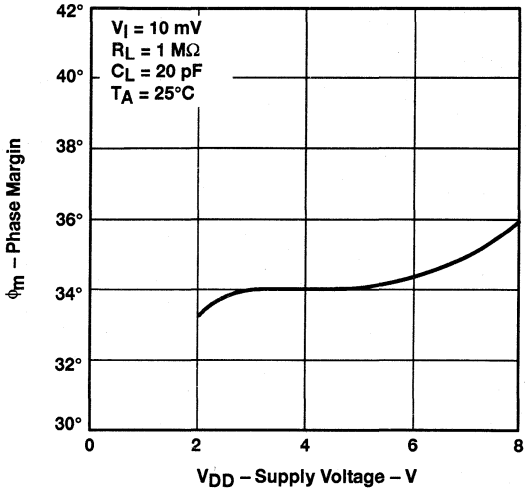


Figure 88

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

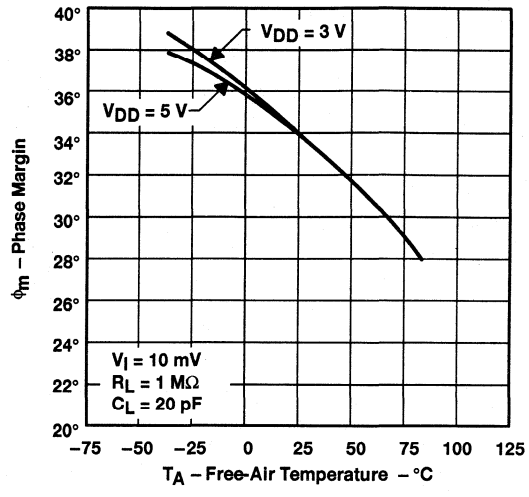


Figure 89

PHASE MARGIN
vs
LOAD CAPACITANCE

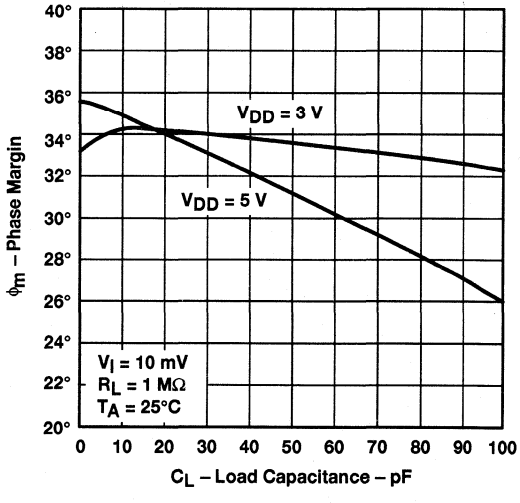


Figure 90

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

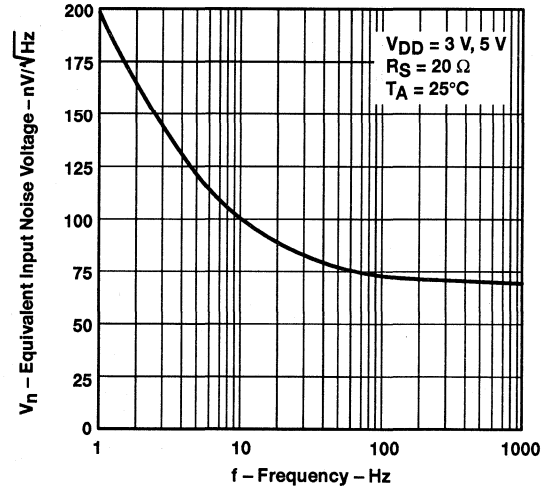


Figure 91

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2341 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

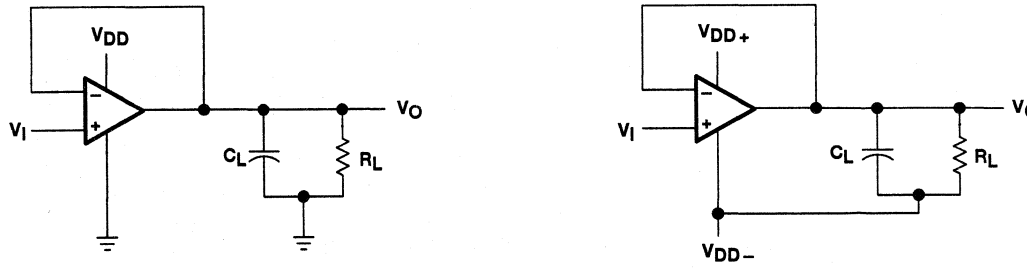


Figure 92. Unity-Gain Amplifier

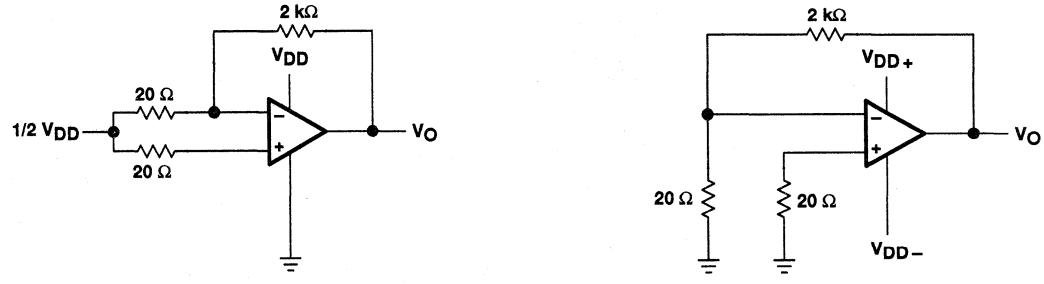


Figure 93. Noise-Test Circuits

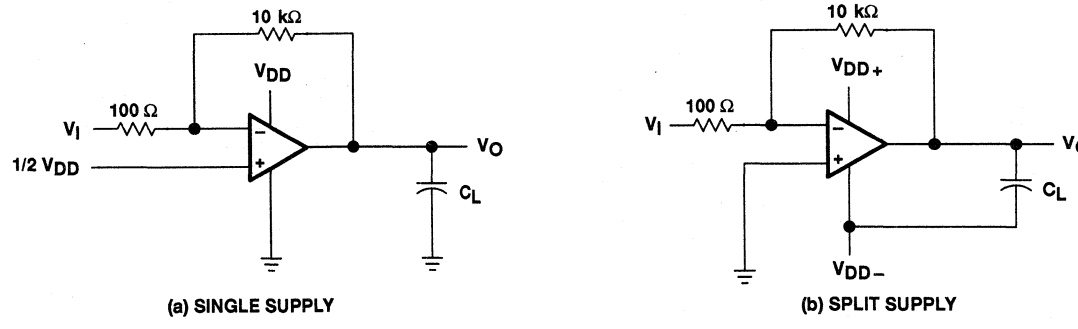


Figure 94. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2341 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 95). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

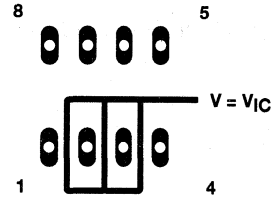


Figure 95. Isolation Metal Around Device Inputs (P package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those qucted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 92. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 96). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

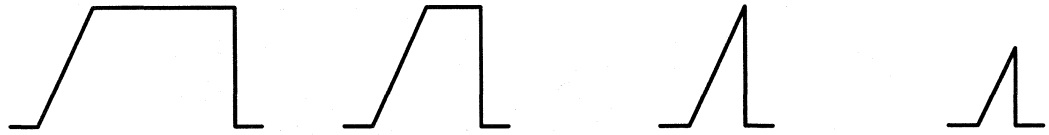


Figure 96. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2341 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

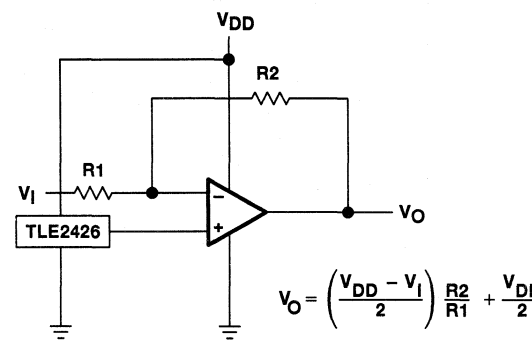


Figure 97. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2341 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 98); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

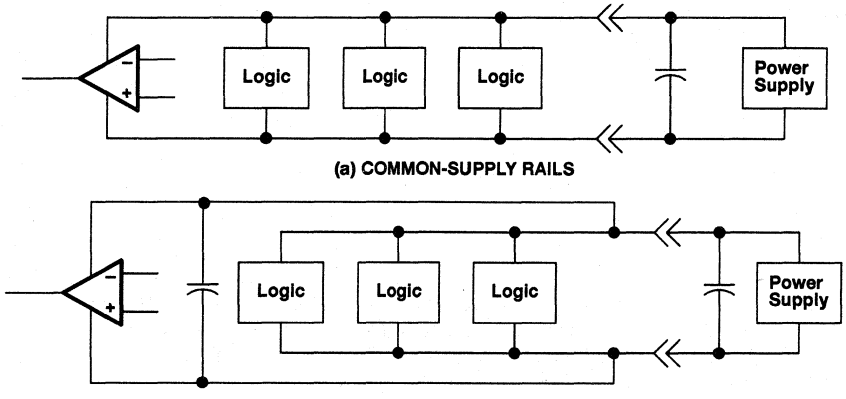


Figure 98. Common Versus Separate Supply Rails

input offset voltage nulling

The TLV2341 offers external input offset null control. Nulling of the input offset voltage can be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 99. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range allows the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.

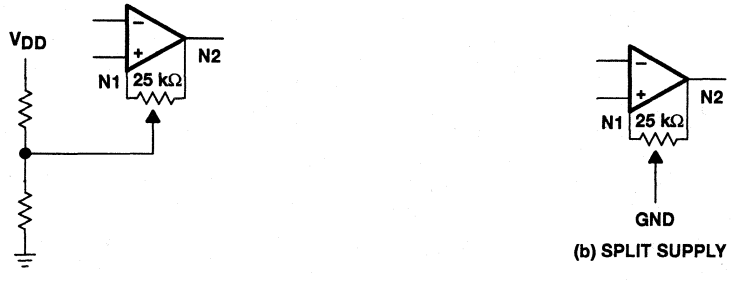
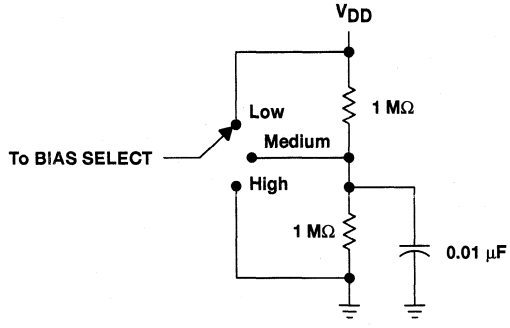


Figure 99. Input Offset Voltage Null Circuit

APPLICATION INFORMATION

bias selection

Bias selection is achieved by connecting the bias-select pin to one of the three voltage levels (see Figure 100). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode necessitates using a voltage divider as indicated. The use of large-value resistors in the voltage divider reduces the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS-SELECT VOLTAGE (single supply)
Low	V_{DD}
Medium	1 V to V_{DD} –1 V
High	GND

Figure 100. Bias Selection for Single-Supply Applications

input characteristics

The TLV2341 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD} –1.2 V at all other temperatures.

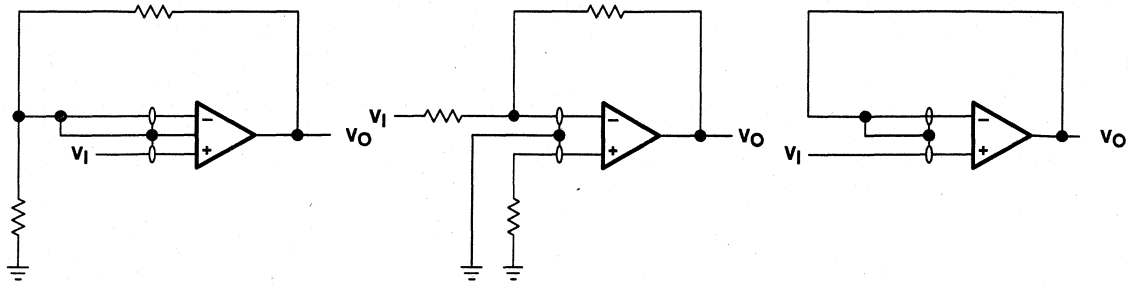
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2341 good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2341 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 95 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 101).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 101. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2341 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 102). The value of this capacitor is optimized empirically.

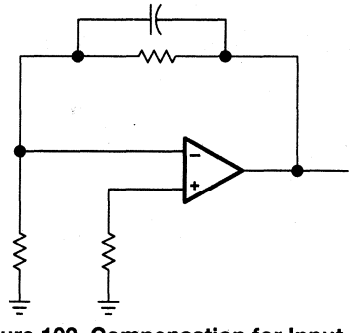


Figure 102. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2341 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2341 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by

APPLICATION INFORMATION

design be forward biased. Applied input and output voltage should not exceed the supply voltage by more that 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2341 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2341 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 103). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

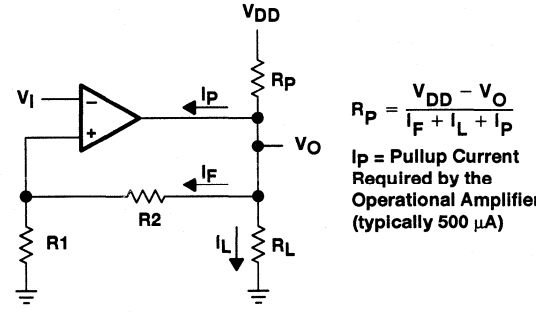


Figure 103. Resistive Pullup to Increase V_{OH}

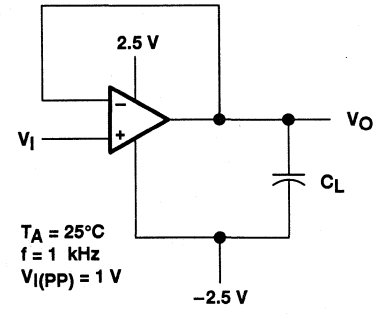
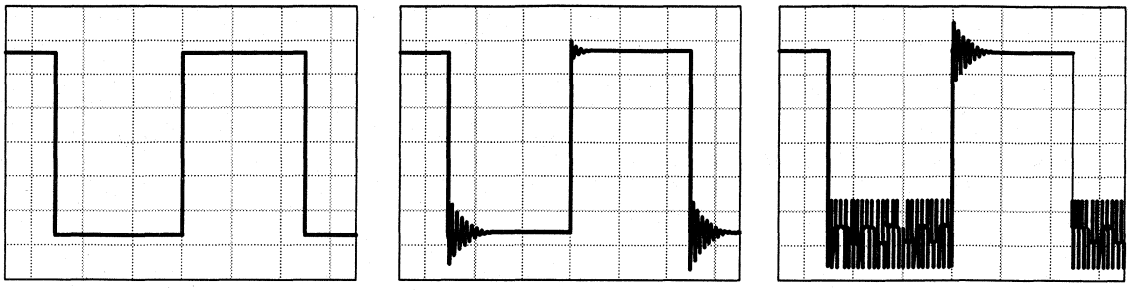


Figure 104. Test Circuit for Output Characteristics

All operating characteristics of the TLV2341 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figures 105, 106 and 107). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

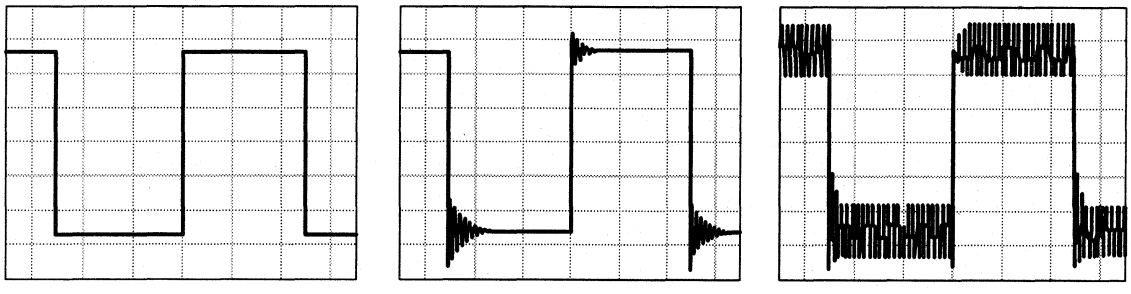
APPLICATION INFORMATION

output characteristics (continued)



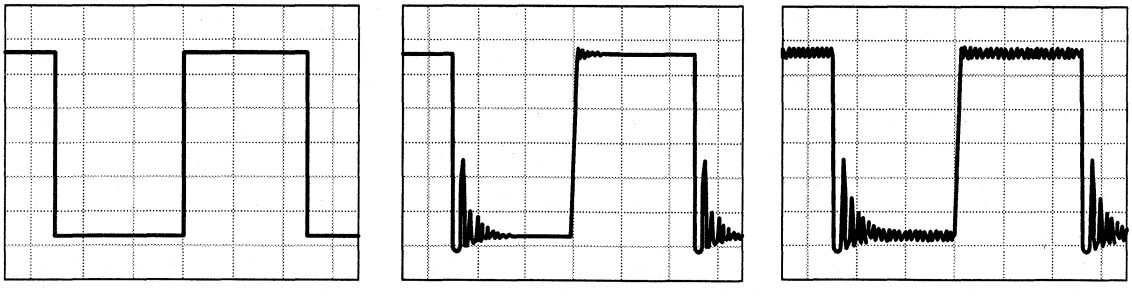
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 105. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 106. Effect of Capacitive Loads in Medium-Bias Mode

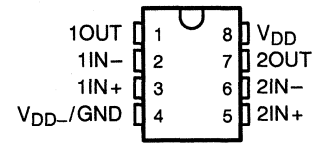


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

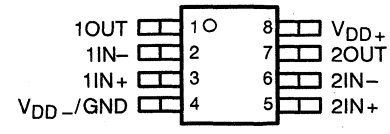
Figure 107. Effect of Capacitive Loads in Low-Bias Mode

- **Wide Range of Supply Voltages Over Specified Temperature Range: −40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and Latch-Up to V_{DD} −1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

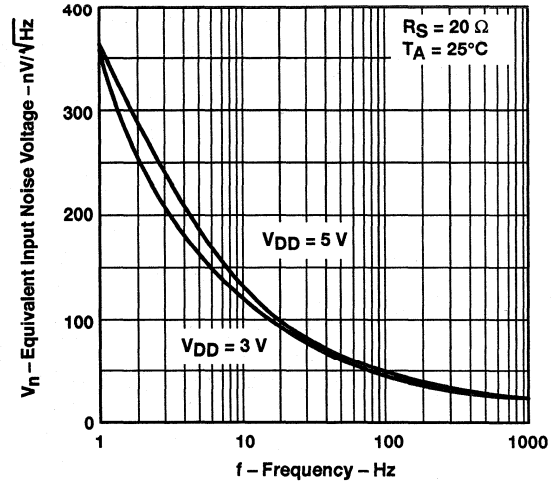


description

The TLV2342 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2342 was developed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2342 has a typical slew rate of 2.1 V/μs and 790-kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V and is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of −40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



Low-voltage and low-power operation has been made possible by using Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2342 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
−40°C to 85°C	9 mV	TLV2342ID	TLV2342IP	TLV2342IPWLE	TLV2342Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2342IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2342IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

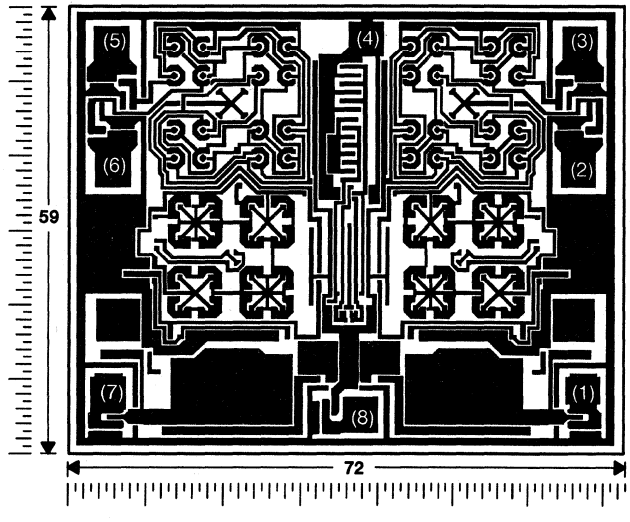
To facilitate the design of small portable equipment, the TLV2342 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

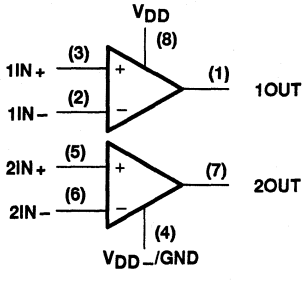
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2342 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

TLV2342Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2342. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

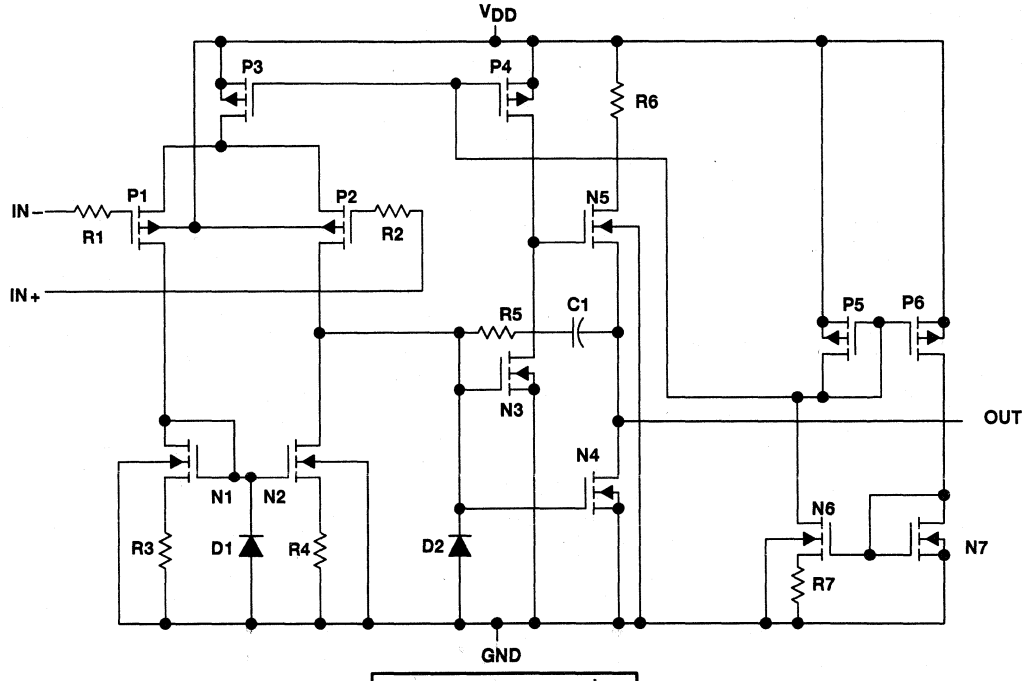
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	725 mV	5.8 mW/°C	377 mW
P	1000 mV	8.0 mW/°C	520 mW
PW	525 mV	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2342I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.6	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		0.65	3		1.4	3.2	mA
			Full range			4			4.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2342I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2342I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		1.7		kHz
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		49°		
				25°C		46°		
				85°C		43°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2342Y						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		0.6	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		5	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	95		70	95		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		0.65	3		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	5 6 7
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	8 9, 11 10 12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature vs Frequency	13 14 24, 25
I_{IB}	Input bias current	vs Temperature	15
I_{IO}	Input offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage vs Temperature	17 18
SR	Slew rate	vs Supply voltage vs Temperature	19 20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	22 23
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	26 27 28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE

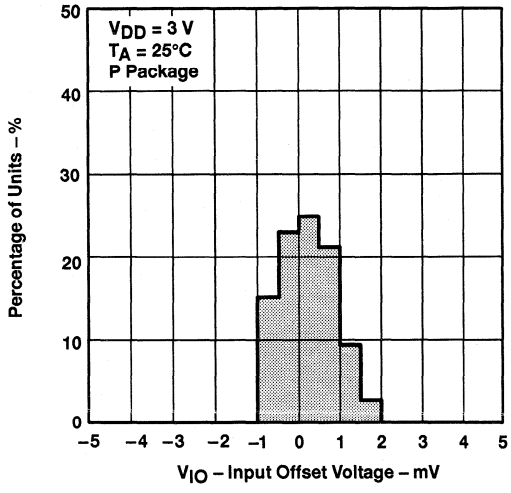


Figure 1

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE

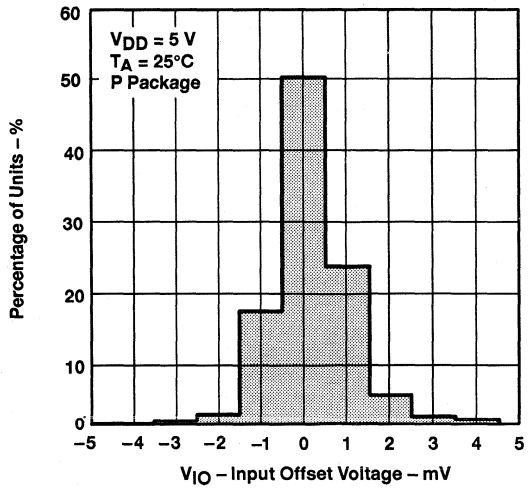


Figure 2

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

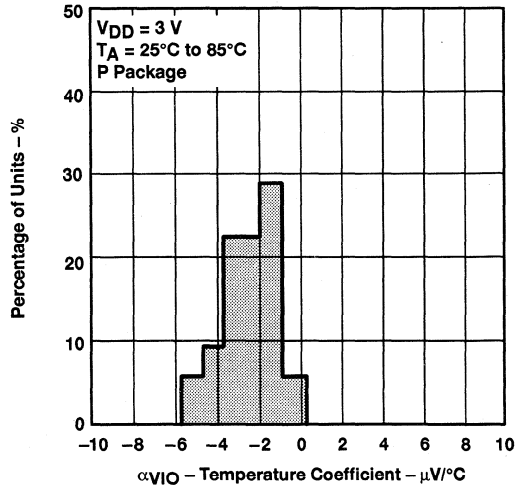


Figure 3

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

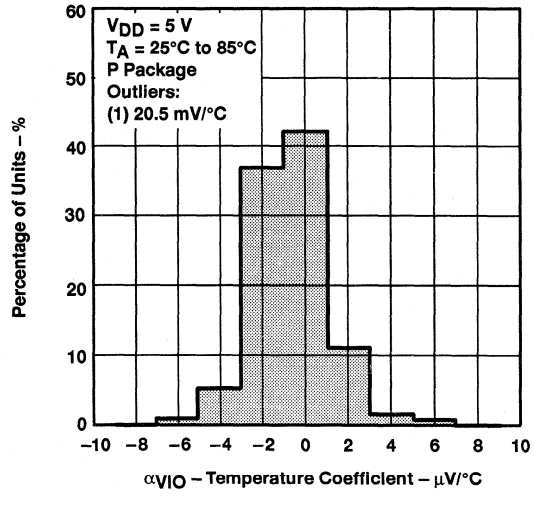


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

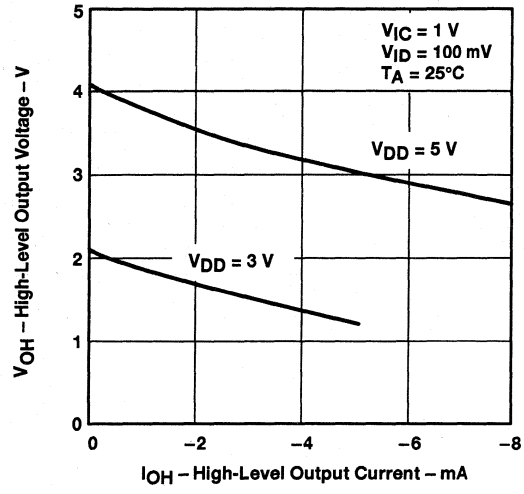


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

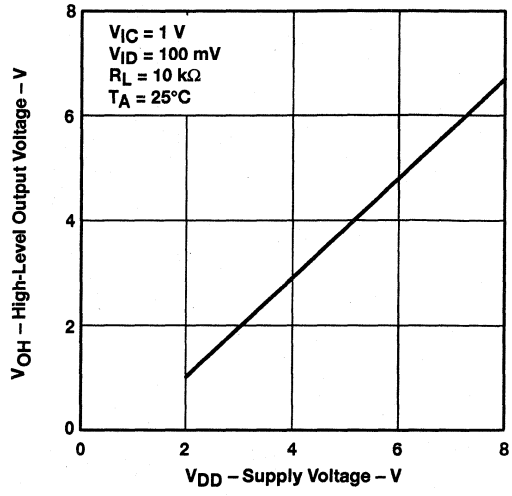


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

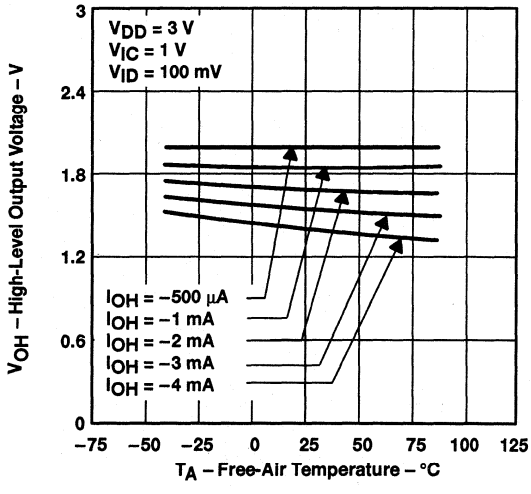


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

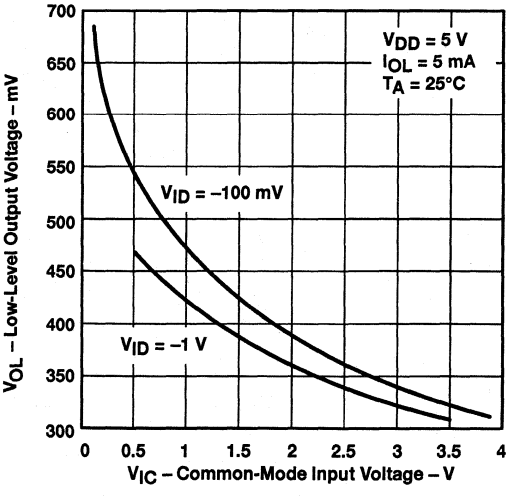


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

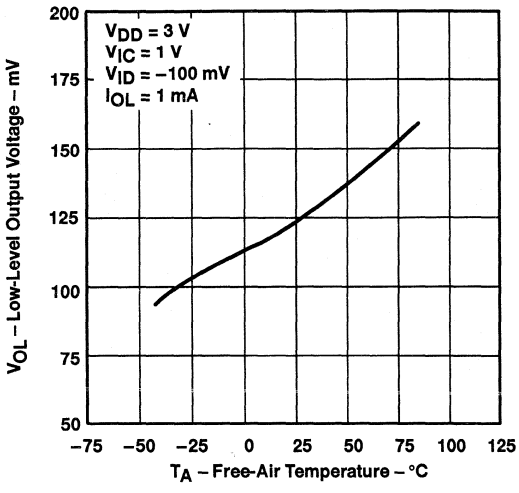


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

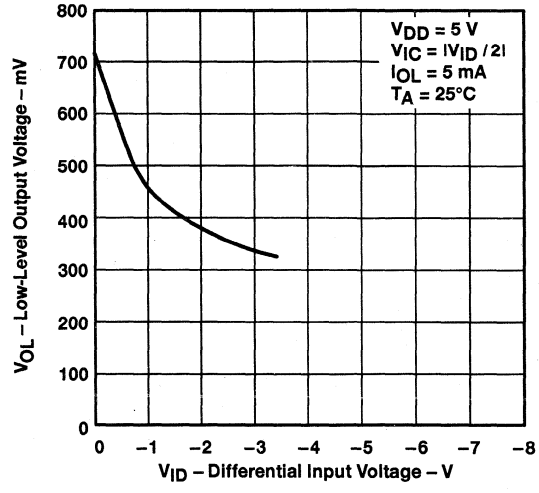


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

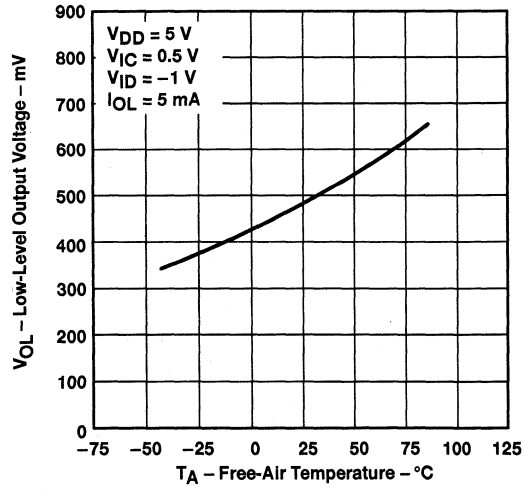


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

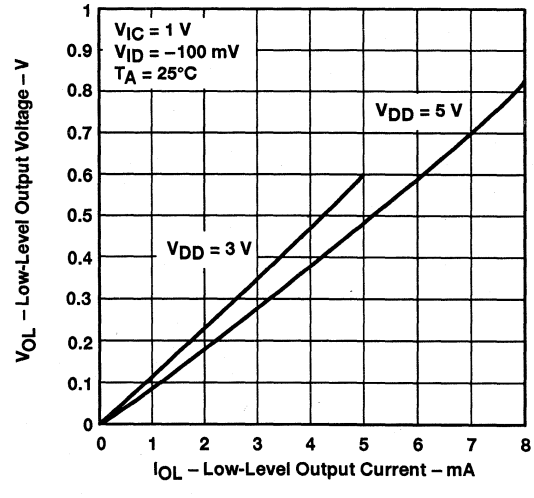


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

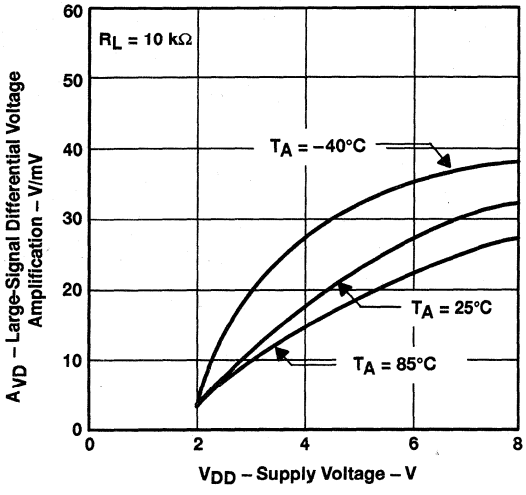


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

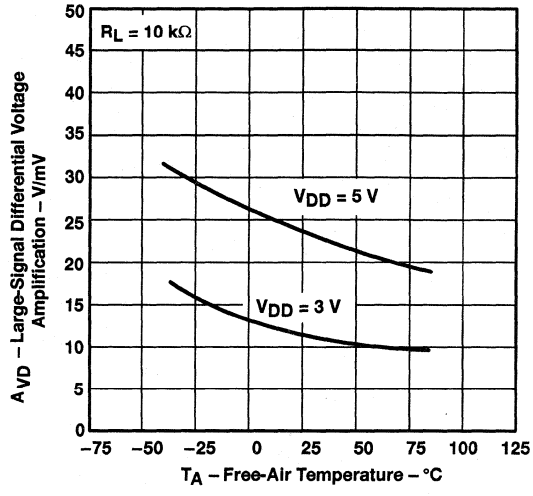
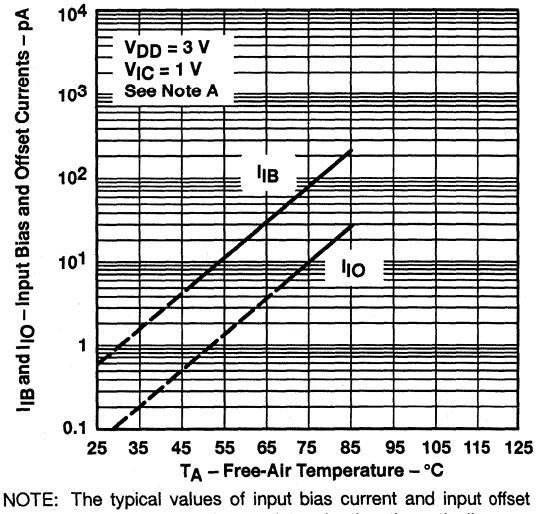


Figure 14

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

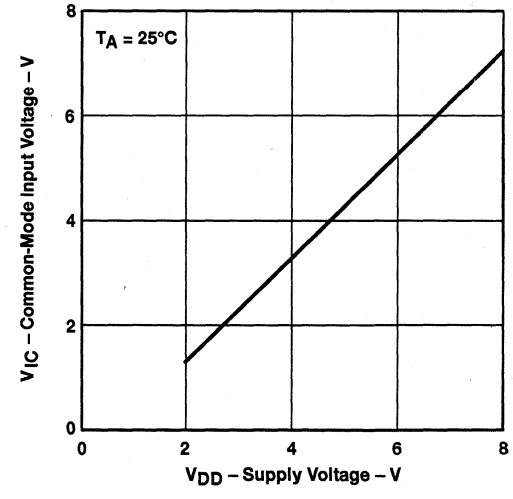


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

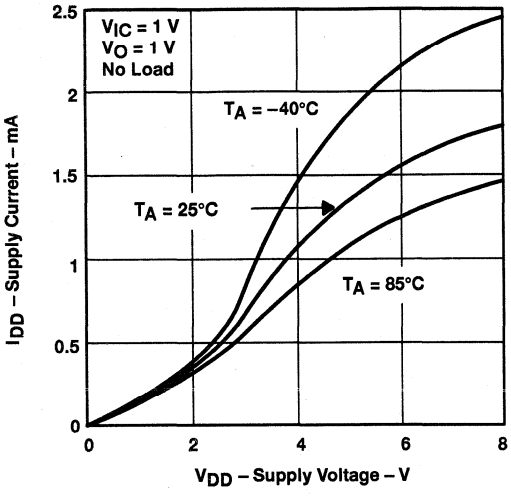


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

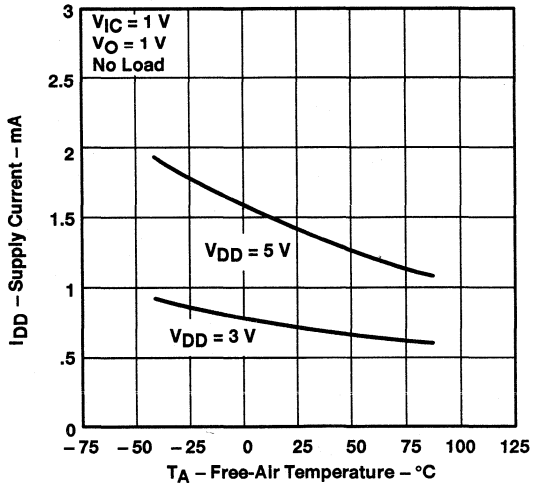


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

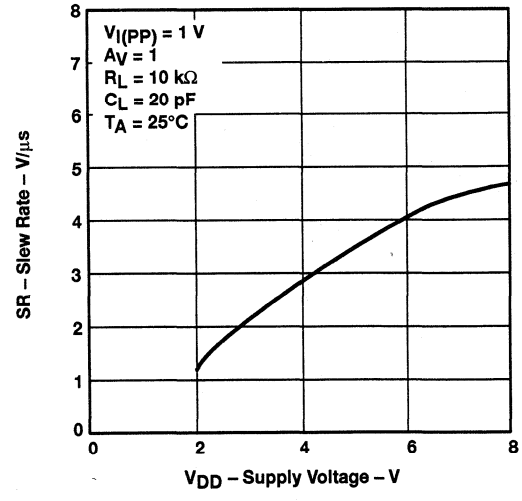


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

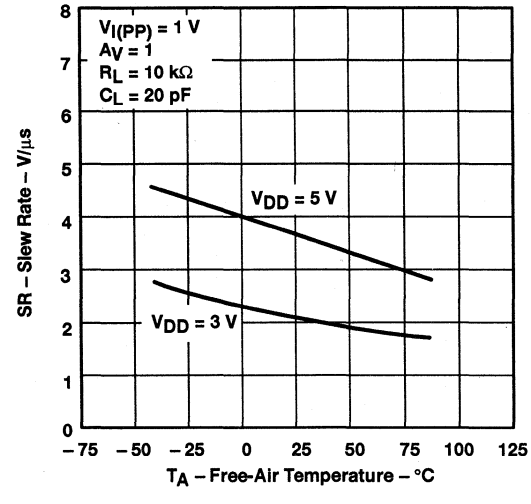


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

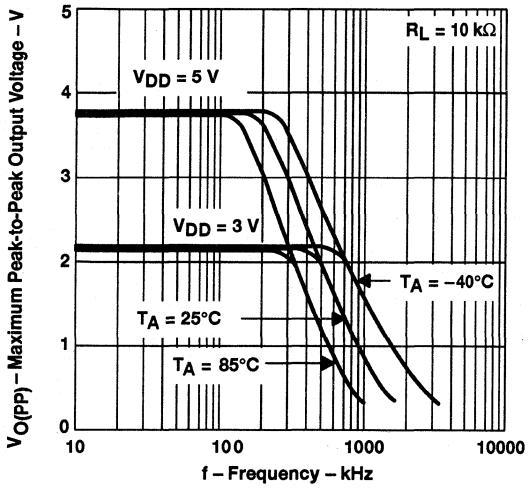


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

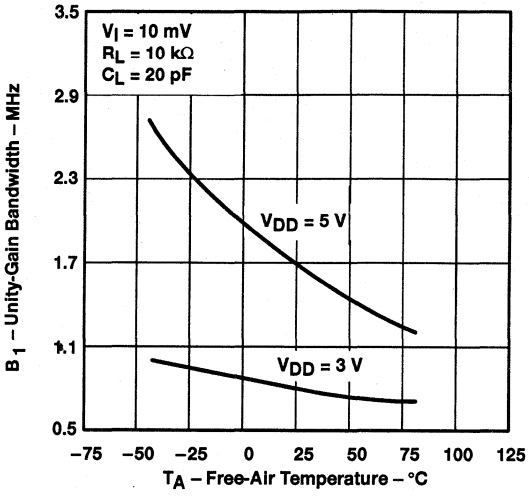


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

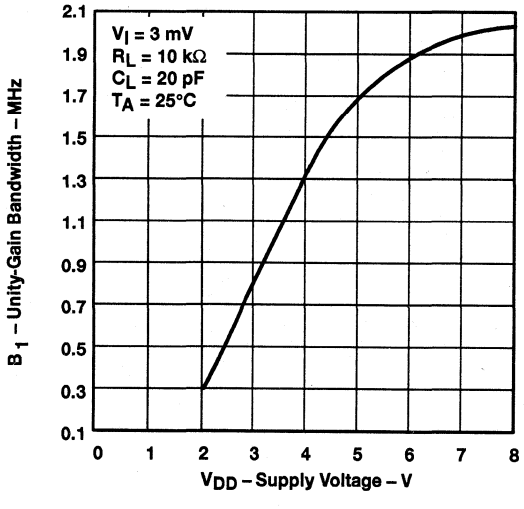


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

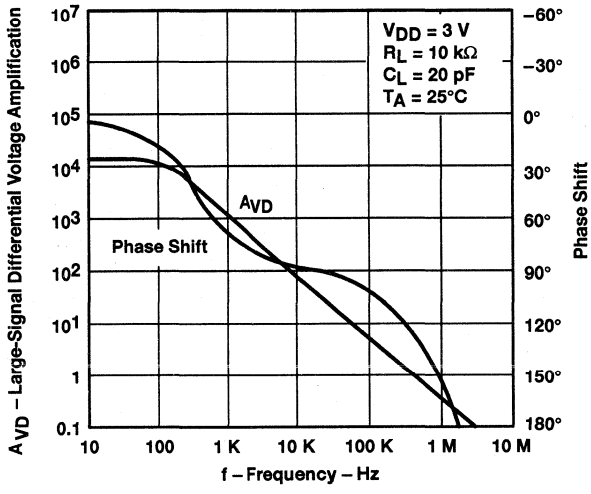


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

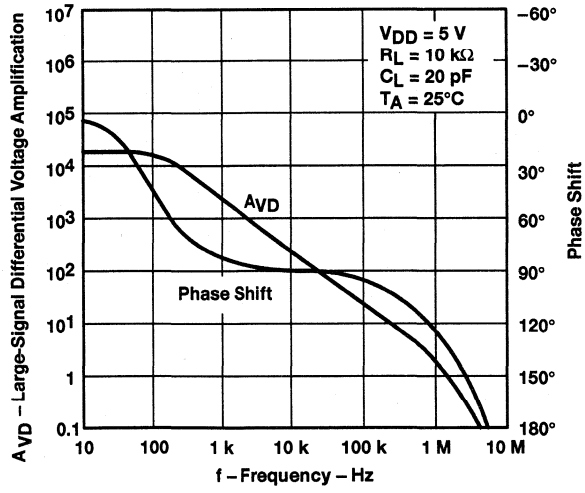


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

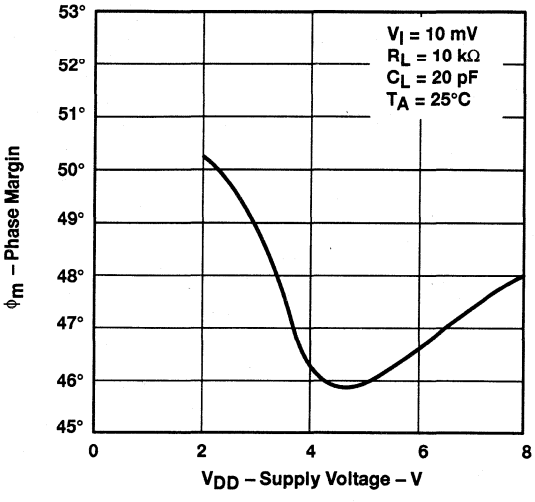


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

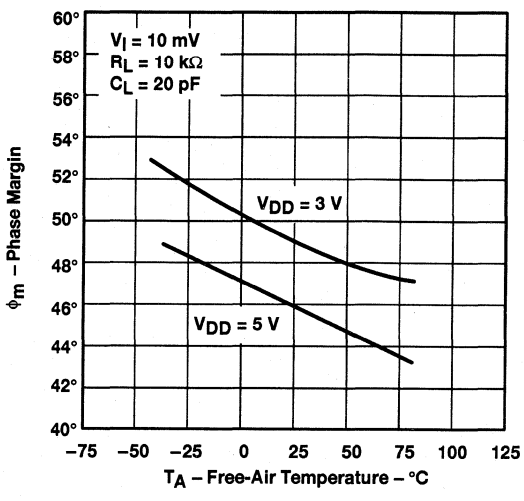


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

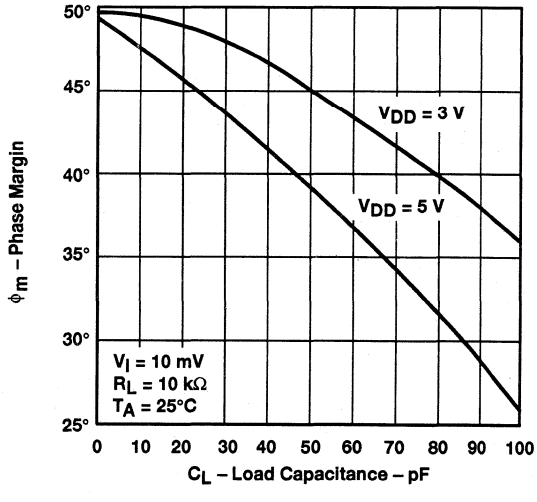


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

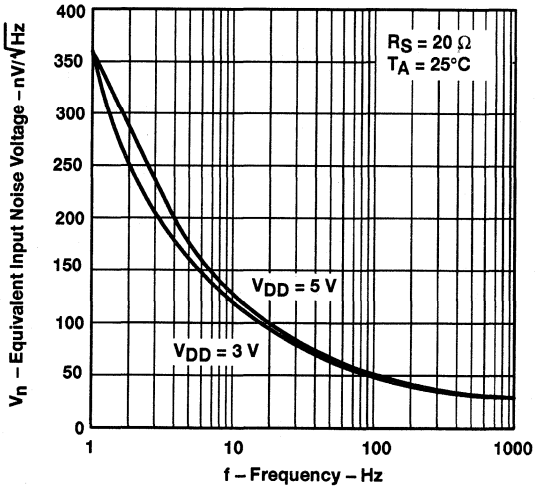


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2342 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

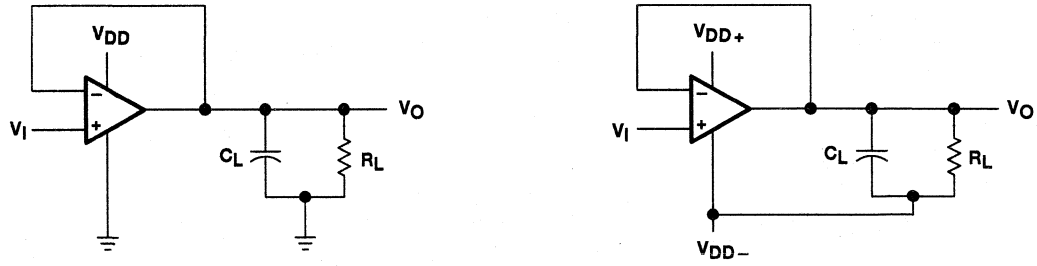


Figure 30. Unity-Gain Amplifier

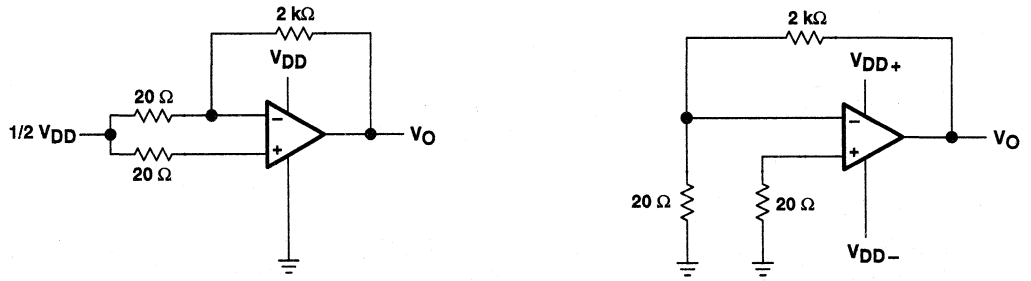


Figure 31. Noise-Test Circuits

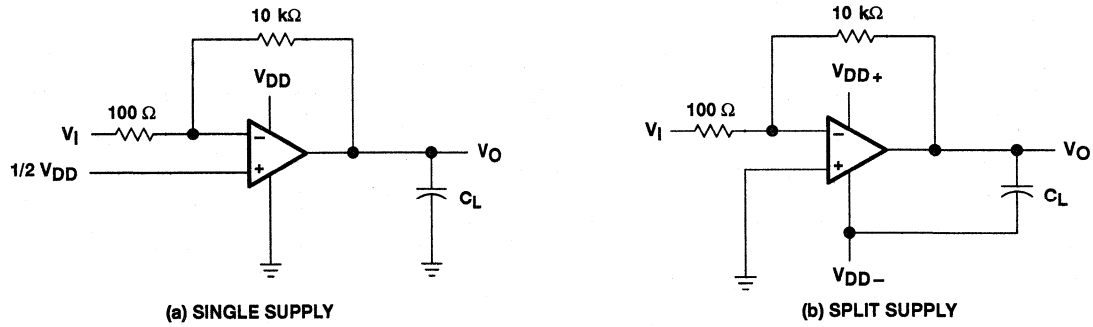


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2342 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.

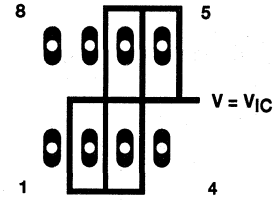


Figure 33. Isolation Metal Around Device Inputs (P package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

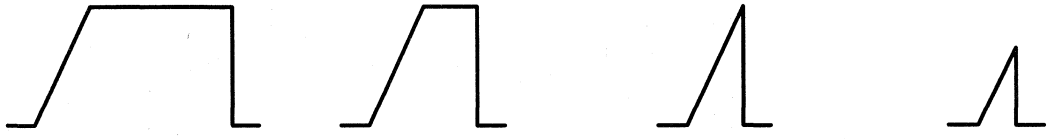


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2342 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

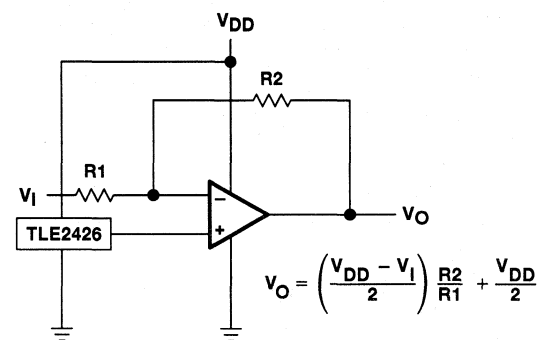


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2342 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

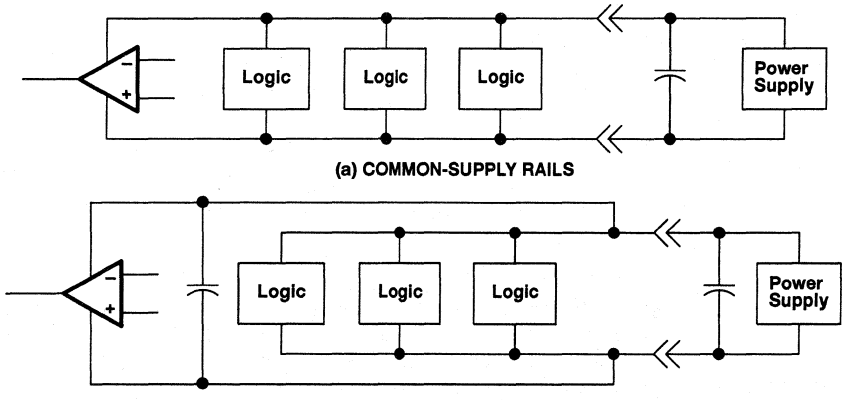


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2342 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD}– 1.2 V at all other temperatures.

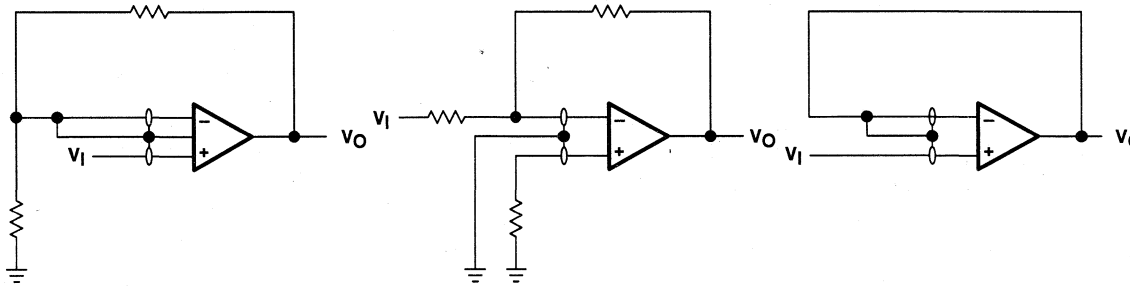
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2342 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2342 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifiers circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2342 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

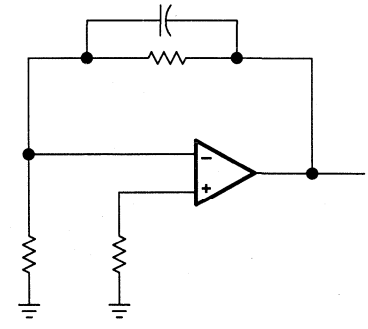


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2342 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2342 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

APPLICATION INFORMATION

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2342 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2342 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

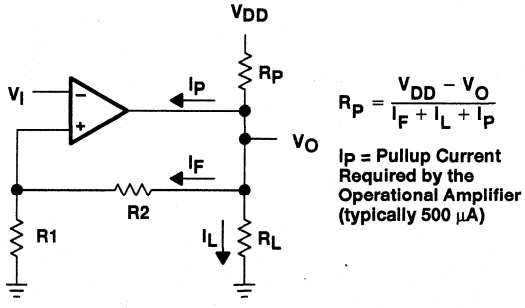


Figure 39. Resistive Pullup to Increase V_{OH}

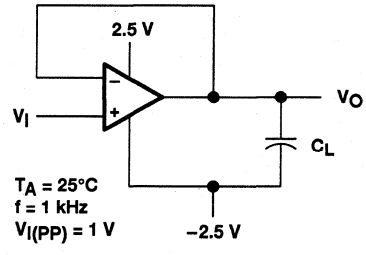
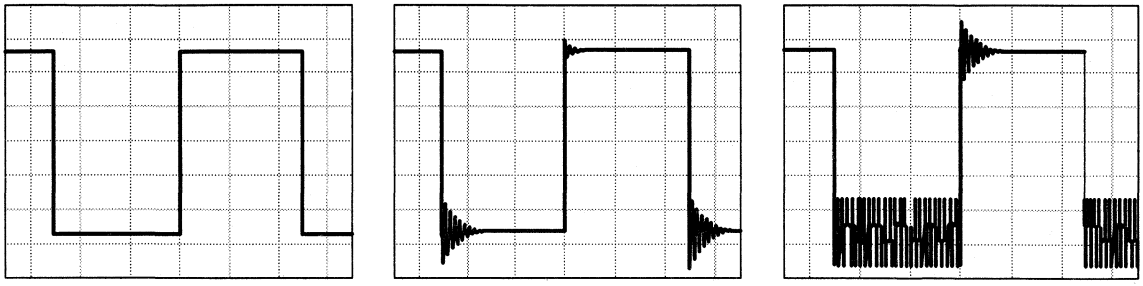


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2342 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figures 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

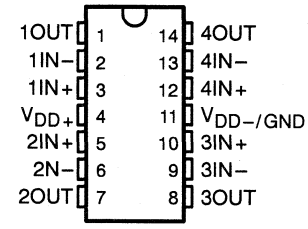
(b) C_L = 130 pF, R_L = NO LOAD

(c) C_L = 150 pF, R_L = NO LOAD

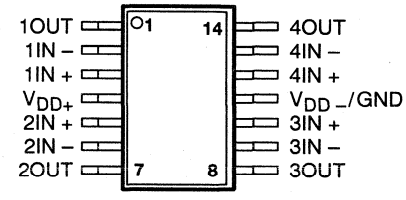
Figure 41. Effect of Capacitive Loads

- **Wide Range of Supply Voltages Over Specified Temperature Range: –40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

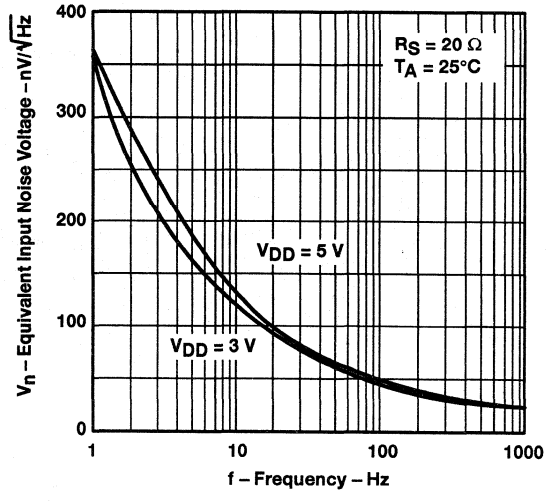


description

The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2344 is designed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2344 has a typical slew rate of 2.1 V/μs and 790-kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of –40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	10 mV	TLV2344ID	TLV2344IN	TLV2344IPWLE	TLV2344Y

Available in tape and reel. Add R suffix to the device type when ordering (e.g., TLV2344IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2344IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

description (continued)

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2344 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

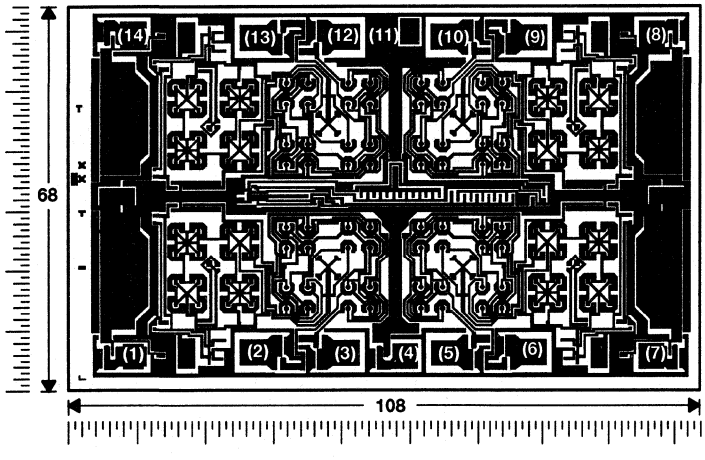
To facilitate the design of small portable equipment, the TLV2344 is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

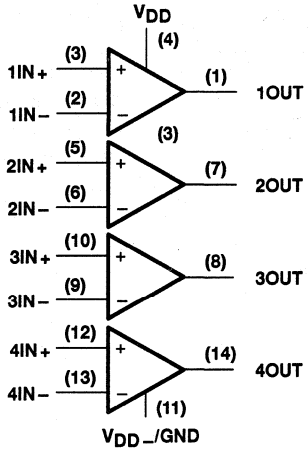
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2344 incorporates internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2344Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2344. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

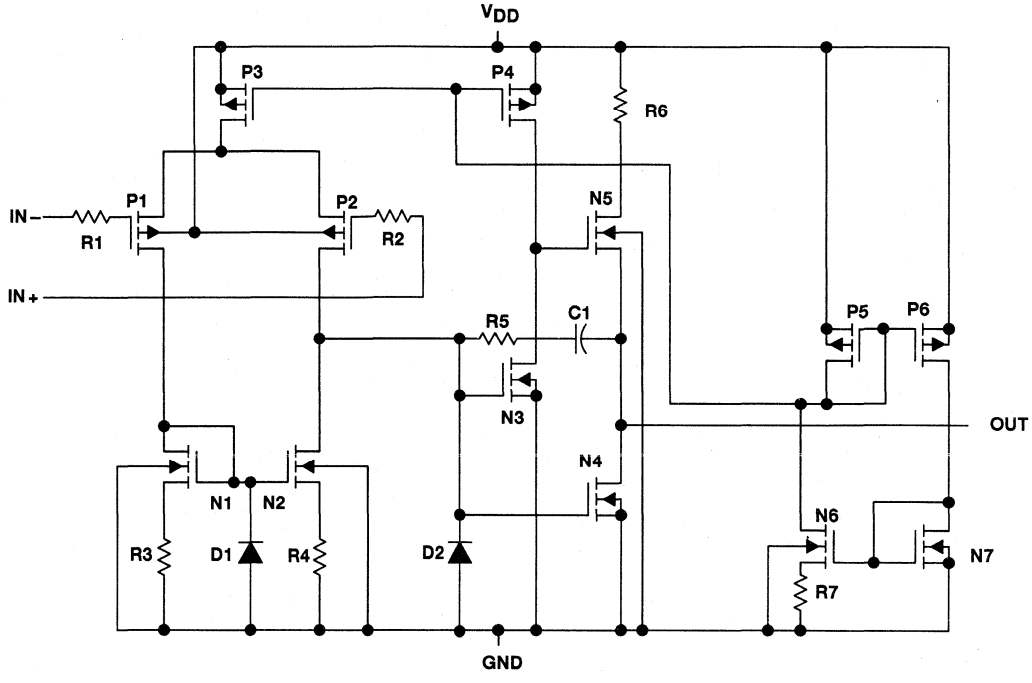
BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

equivalent schematic (each amplifier)



COMPONENT COUNT†	
Transistors	8
Diodes	28
Resistors	4
Capacitors	108

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... $V_{DD\pm}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O ..... ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application selection).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1575 mW	5.6 mW/°C	364 mW
PW	700 mW	12.6 mW/°C	819 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	−0.2	1.8	V
	V_{DD} = 5 V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2344I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/MV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		1.3	6		2.7	6.4	mA
			Full range			8			8.8	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2344I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, See Figure 30	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2344I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 31	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 30	25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 10 kΩ,	C_L = 20 pF, See Figure 32	25°C		1.7		MHz
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 32	f = B_1, R_L = 10 kΩ,	−40°C		49°		
				25°C		46°		
				85°C		43°		

electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2344Y						UNIT
			V_{DD} = 3 V			V_{DD} = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		1.1	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		5	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	70	95		70	95		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		1.3	6		2.7	6.4	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Temperature	5 6 7
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Temperature vs Differential input voltage vs Low-level output current	8 9, 11 10 12
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Temperature vs Frequency	13 14 24, 25
I_{IB}	Input bias current	vs Temperature	15
I_{IO}	Input offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage vs Temperature	17 18
SR	Slew rate	vs Supply voltage vs Temperature	19 20
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Unity-gain bandwidth	vs Temperature vs Supply voltage	22 23
ϕ_m	Phase margin	vs Supply voltage vs Temperature vs Load capacitance	26 27 28
V_n	Equivalent input noise voltage	vs Frequency	29
	Phase shift	vs Frequency	24, 25

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE

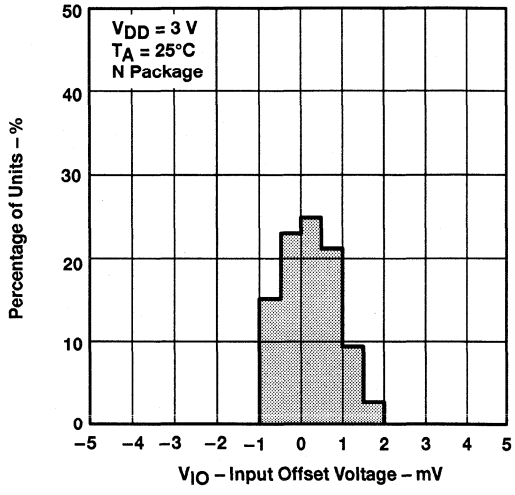


Figure 1

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE

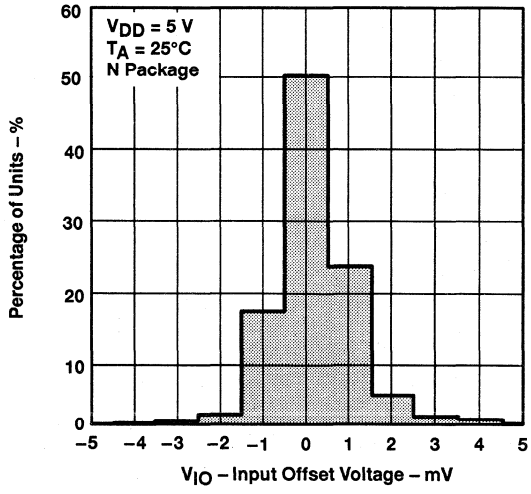


Figure 2

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

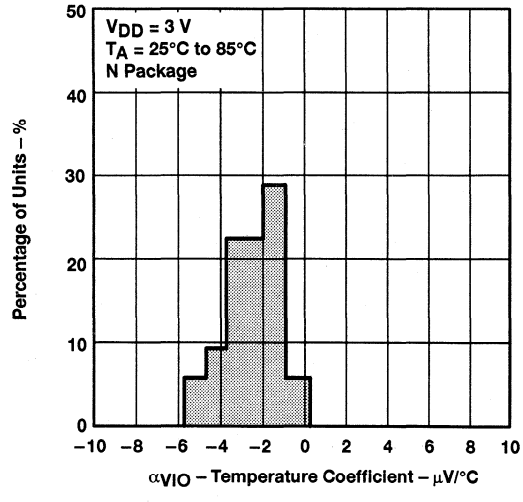


Figure 3

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

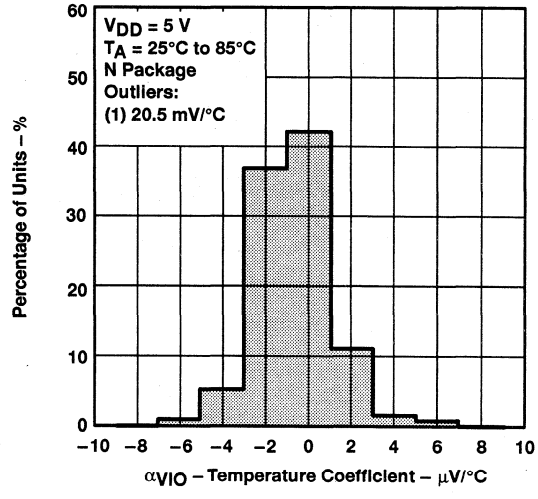


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

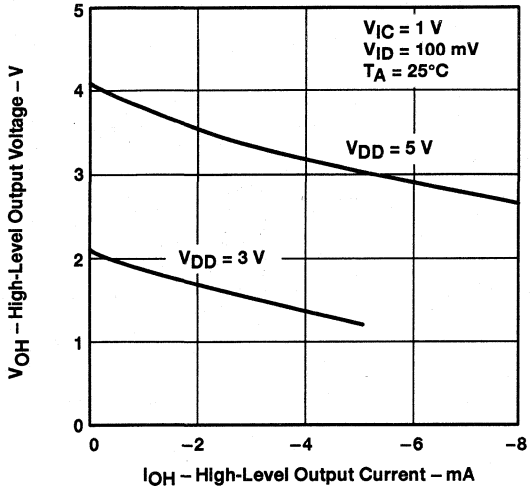


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

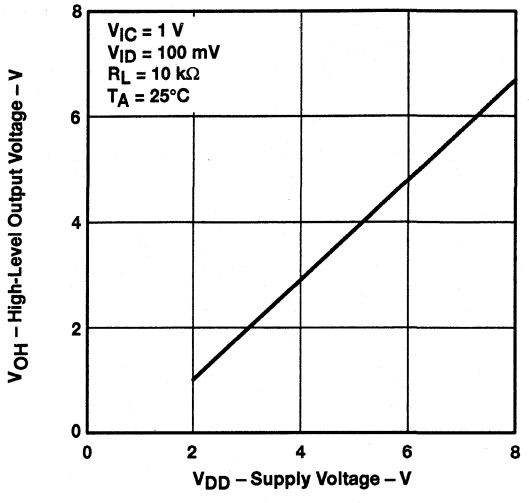


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

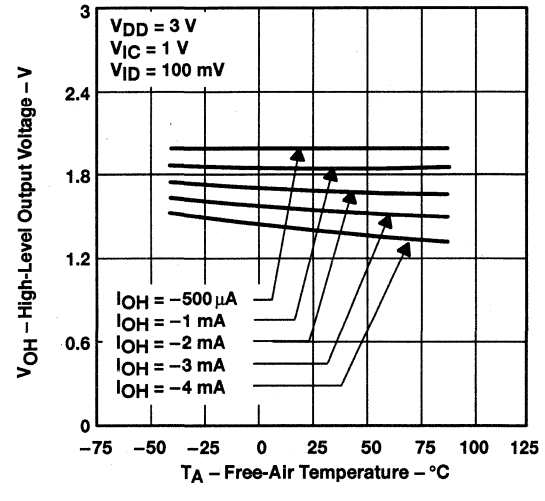


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

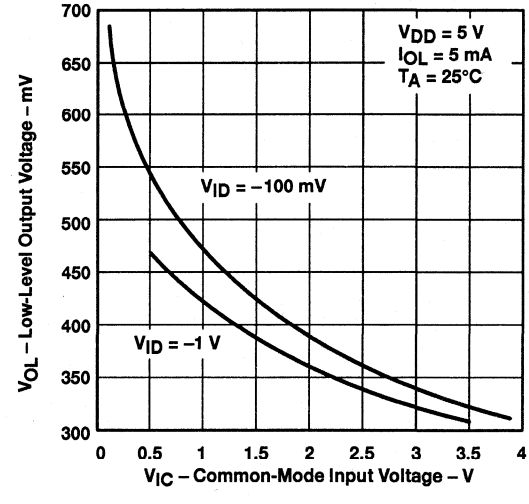


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

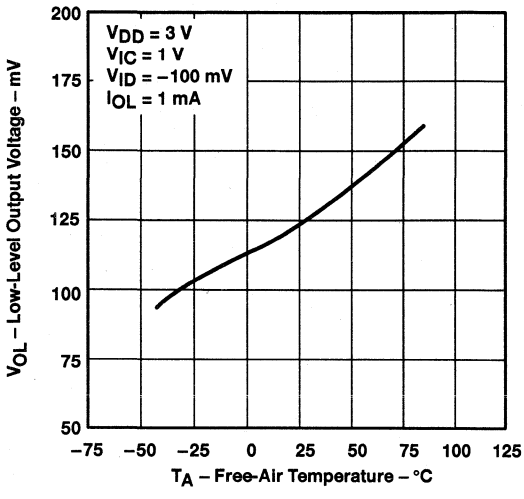


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

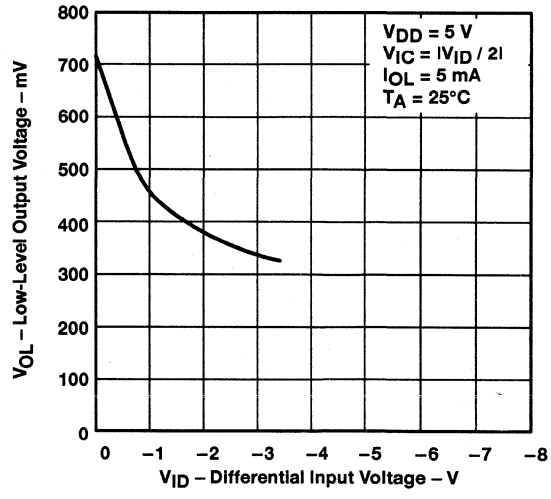


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

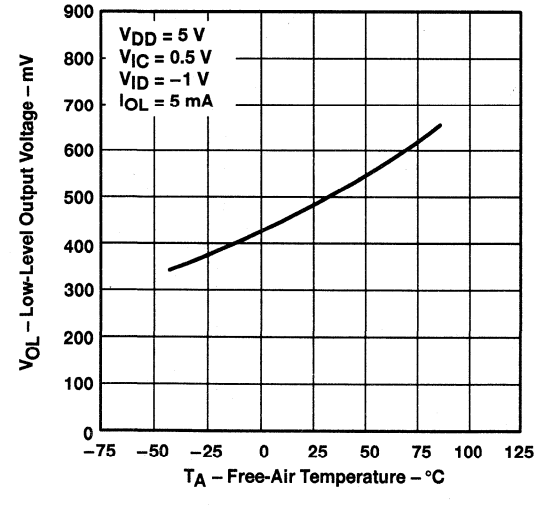


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

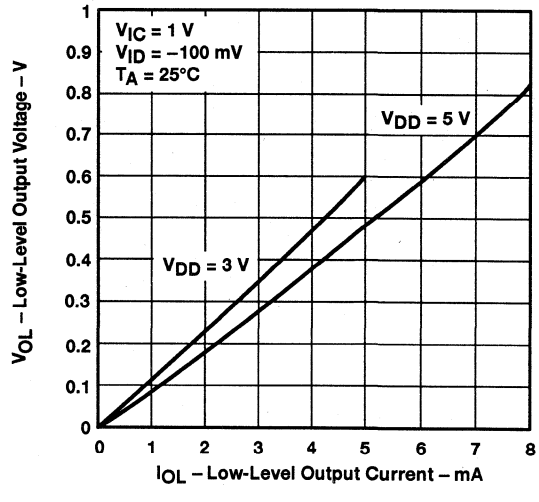


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

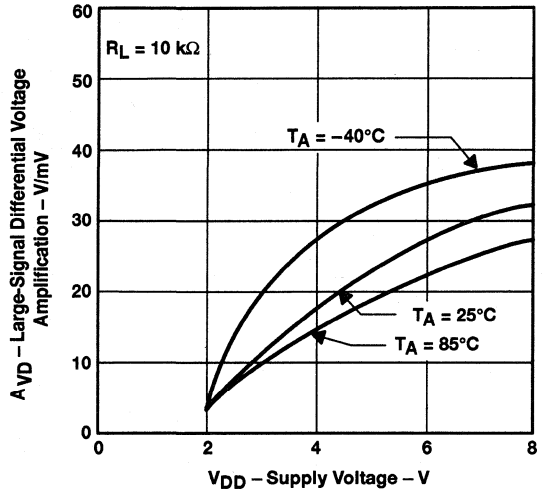


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

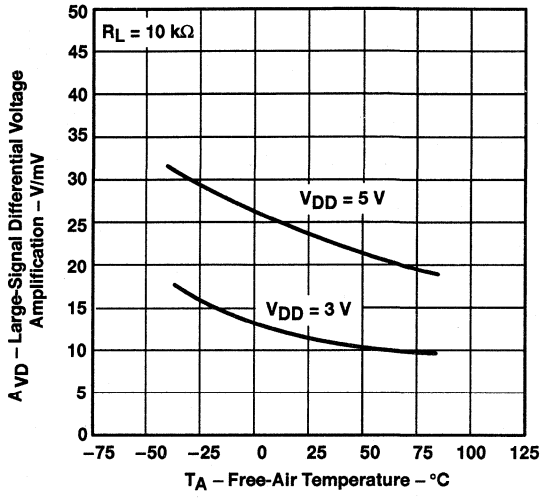
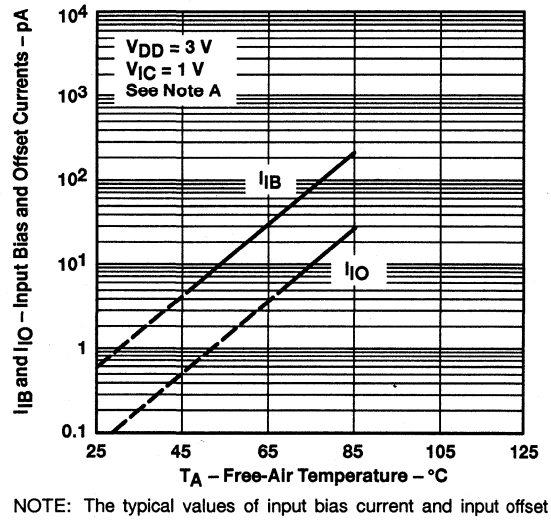


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET
CURRENT
vs
FREE-AIR TEMPERATURE



NOTE: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

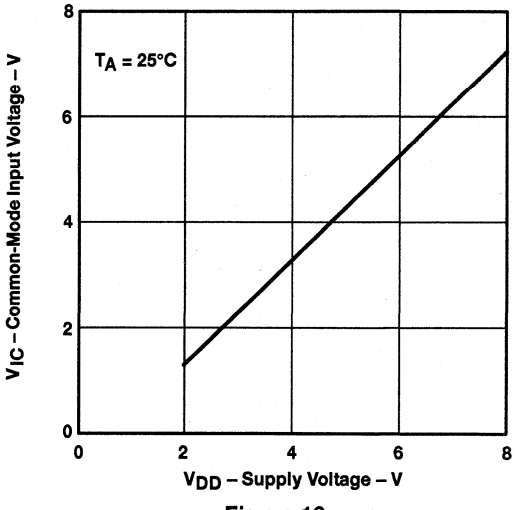


Figure 16

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

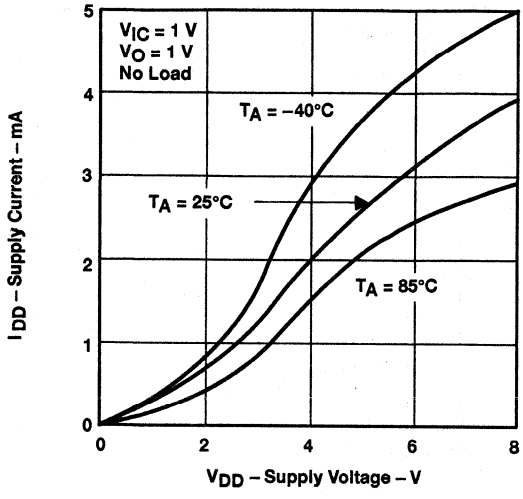


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

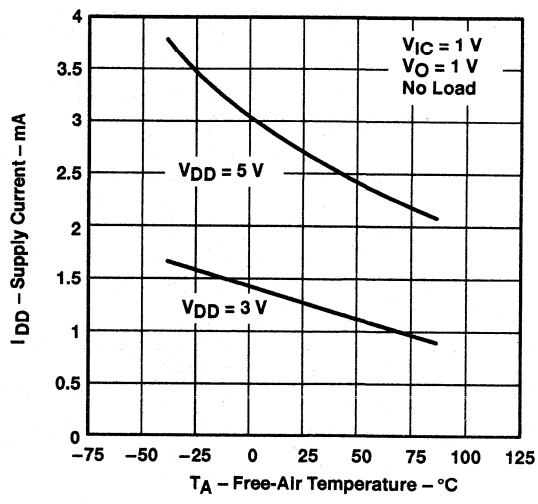


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

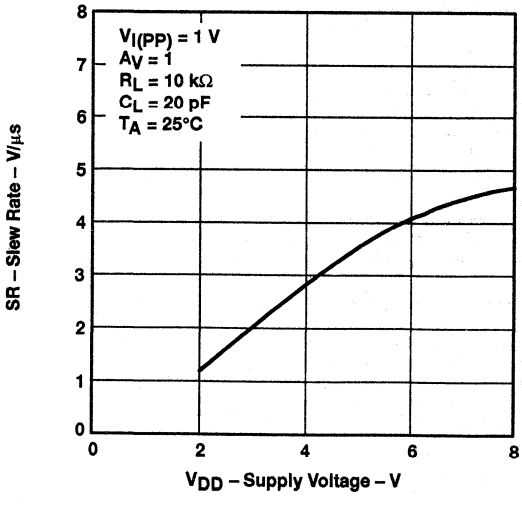


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

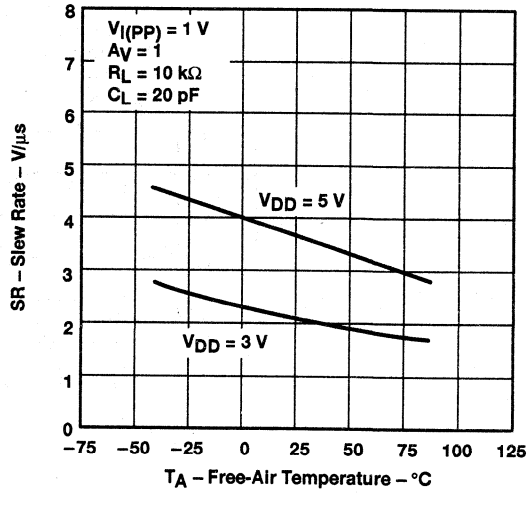


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

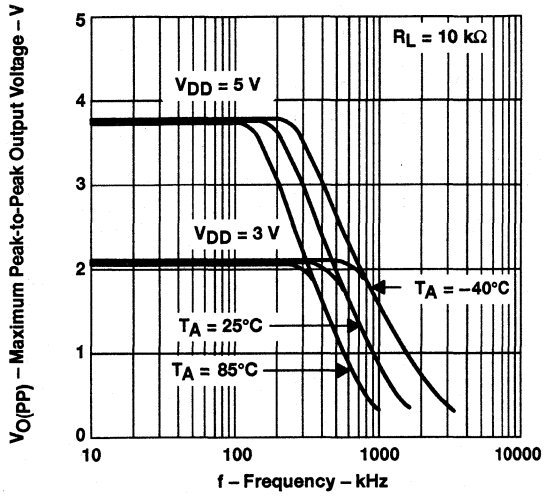


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

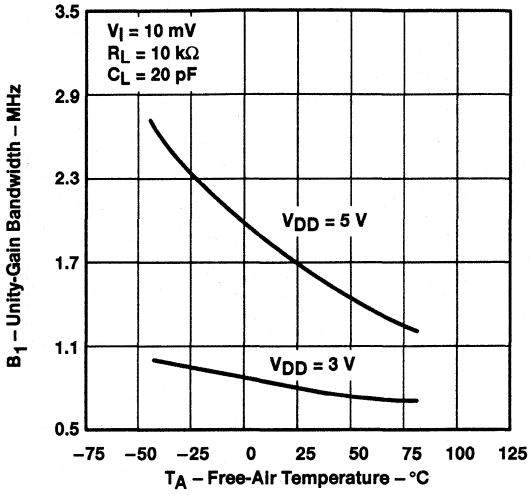


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

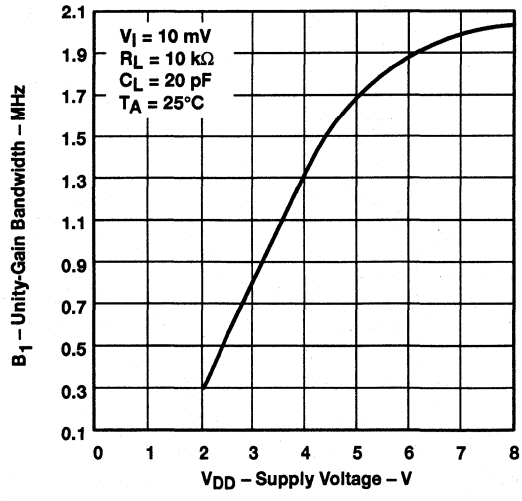


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

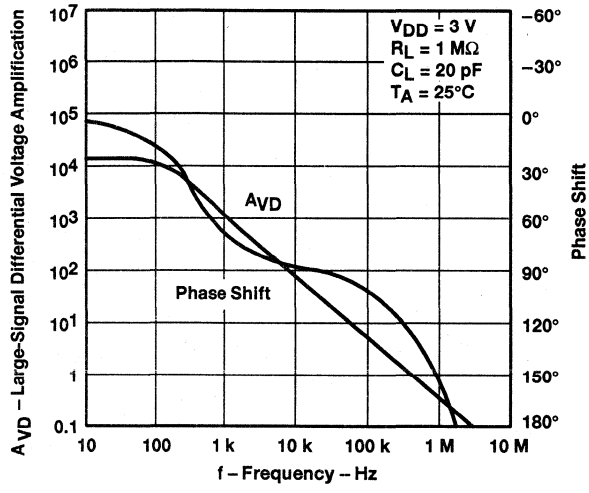


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

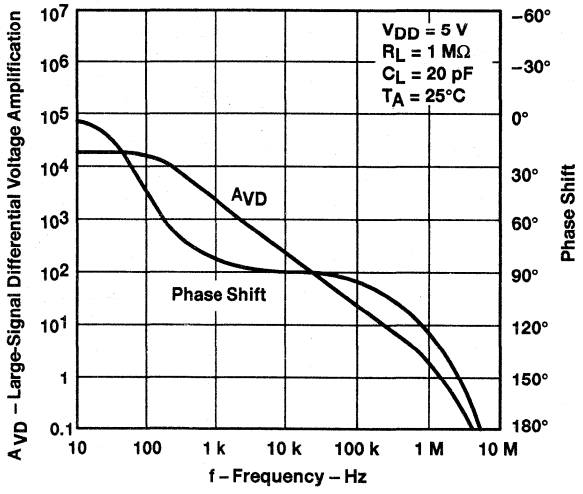


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

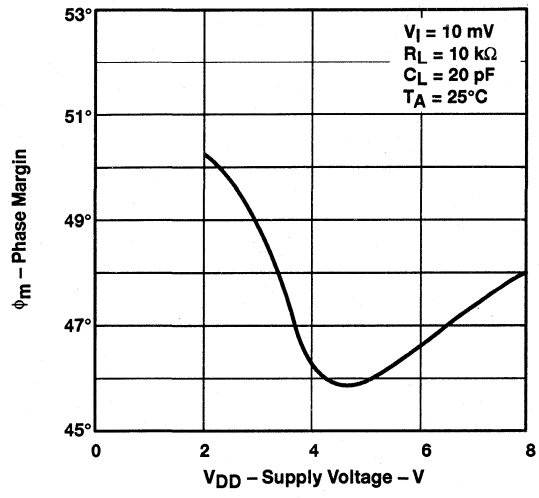


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

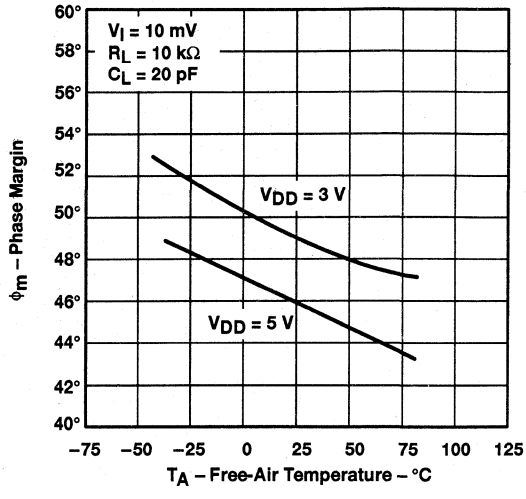


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

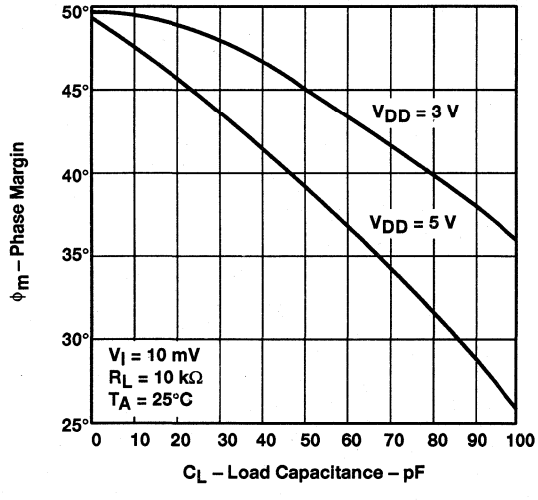


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

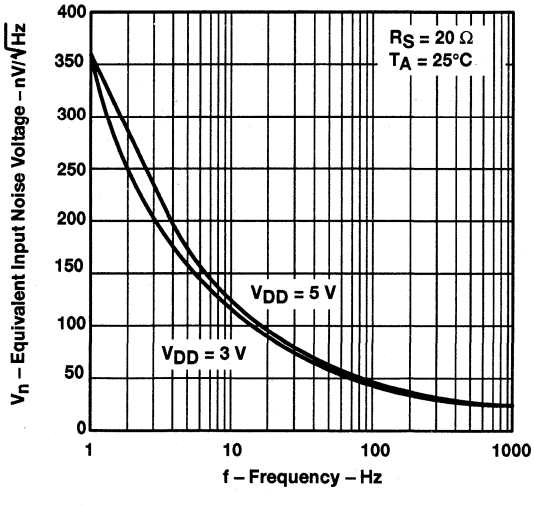


Figure 29

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2344 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

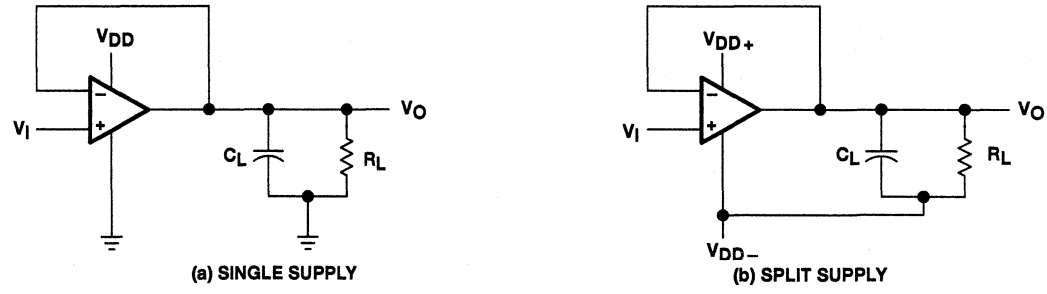


Figure 30. Unity-Gain Amplifier

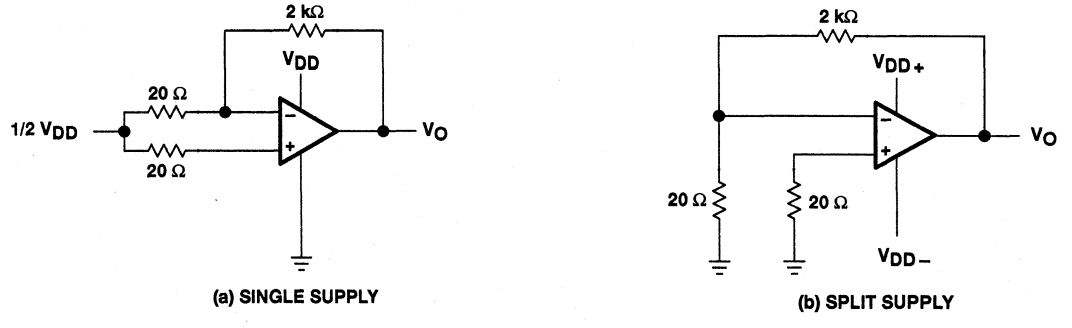


Figure 31. Noise-Test Circuit

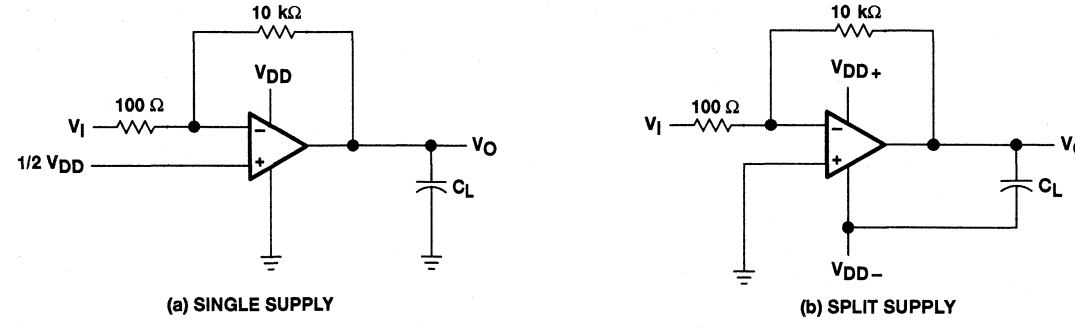


Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2344 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

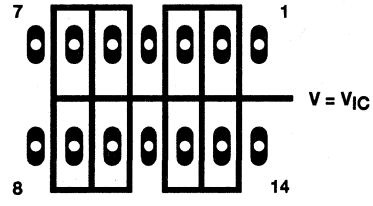


Figure 33. Isolation Metal Around Device Inputs
(N package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

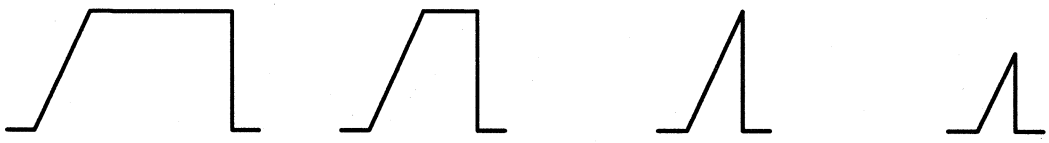


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV2344 performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$ while consuming very little power and is suitable for supply voltages of greater than 4 V.

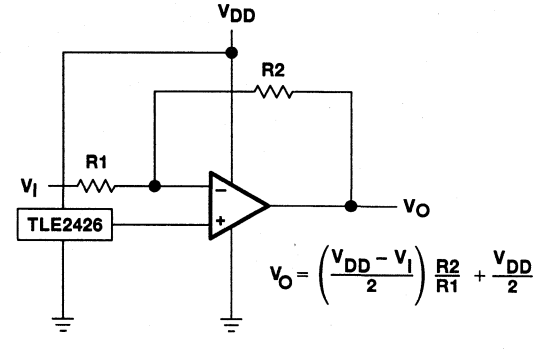


Figure 35. Inverting Amplifier With Voltage Reference

APPLICATION INFORMATION

single-supply operation (continued)

The TLV2344 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

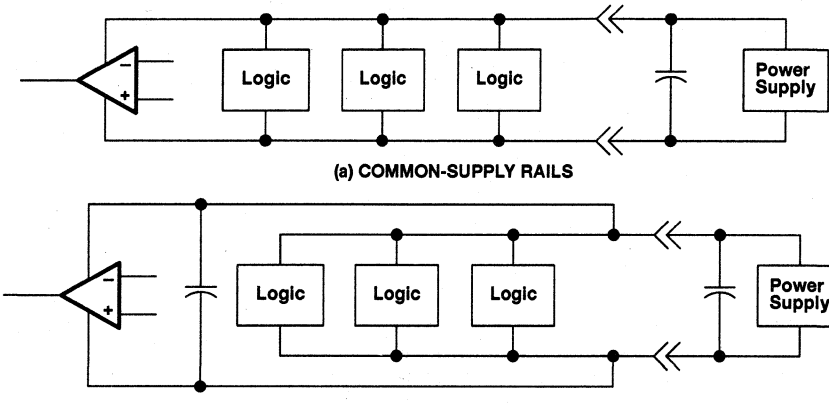


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2344 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

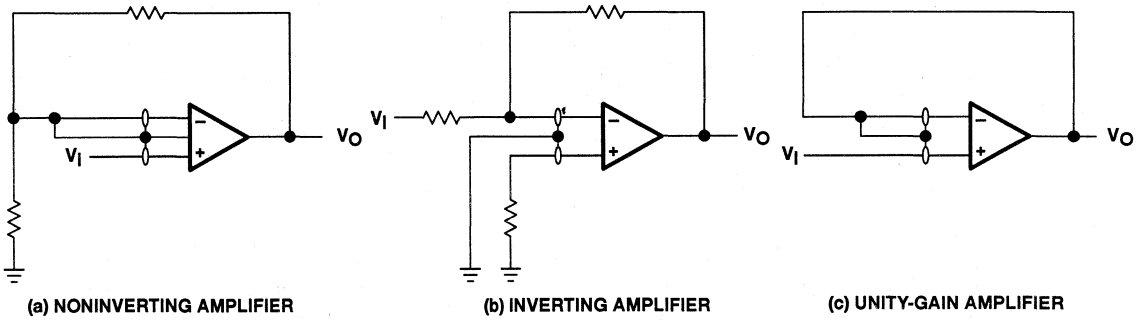
The use of the polysilicon-gate process and the careful input circuit design gives the TLV2344 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV2344 is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

APPLICATION INFORMATION

input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV2344 results in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifiers circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

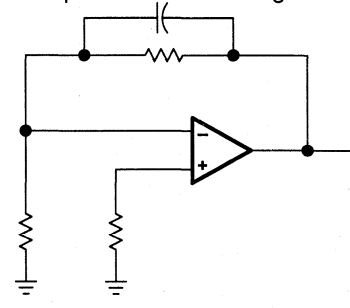


Figure 38. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV2344 incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C. Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2344 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage

APPLICATION INFORMATION

by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2344 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV2344 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

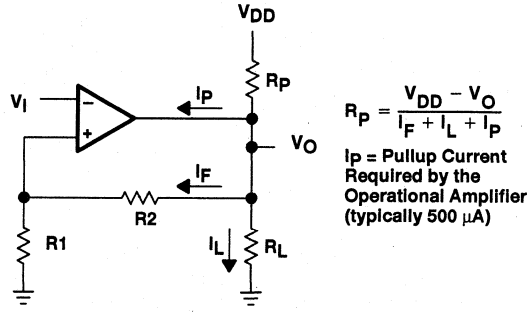


Figure 39. Resistive Pullup to Increase V_{OH}

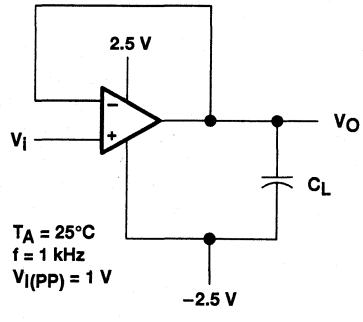
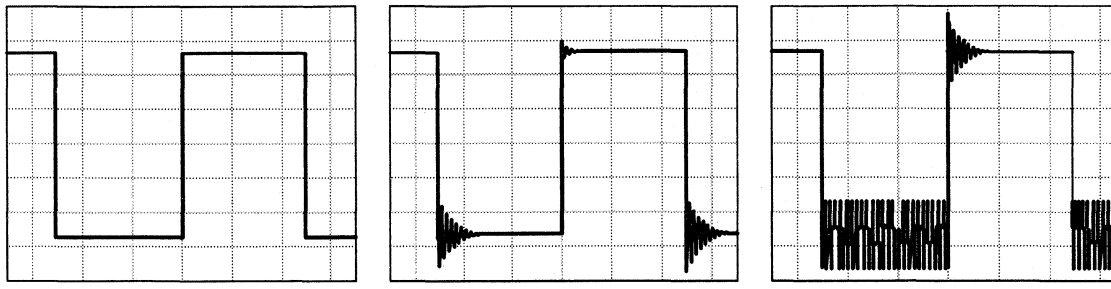


Figure 40. Test Circuit for Output Characteristics

All operating characteristics of the TLV2344 are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

TYPICAL APPLICATION DATA

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

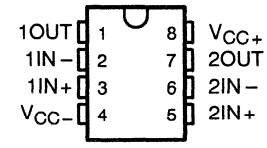
(b) C_L = 130 pF, R_L = NO LOAD

(c) C_L = 150 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads

- **Low Supply Voltage Operation**
  V_{CC} = ± 1 V Min
- **Wide Output Voltage Swing**
  ±2.4 V Typ at $V_{CC±}$ = ±2.5 V, R_L = 10 kΩ
- **Wide Bandwidth**
  7 MHz Typ at $V_{CC±}$ = 2.5 V
- **Low Noise . . . 8 nV/√Hz Typ at f = 1 kHz**
- **High Slew Rate**
  4 V/μsec Typ at $V_{CC±}$ = ±2.5 V
- **Available In TSSOP Packages**

D, P, OR PW PACKAGE
(TOP VIEW)



description

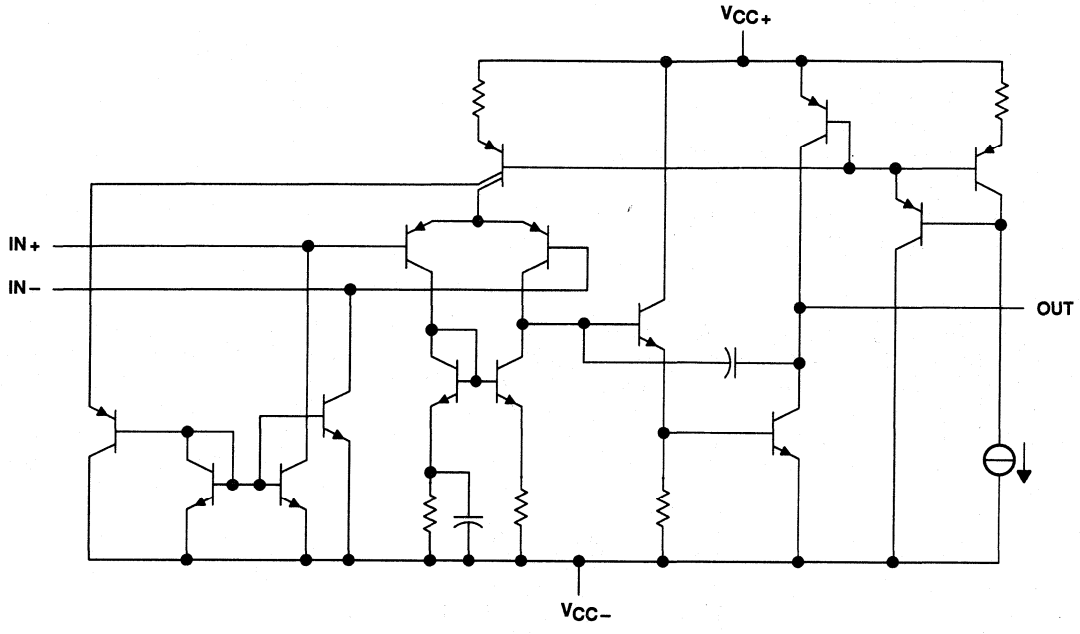
The TLV2362 is a high-performance dual operational amplifier built using an original Texas Instruments bipolar process. This device can be operated at a very low supply voltage (±1 V), while maintaining a wide output swing. The TLV2362 offers a dramatically improved dynamic range of signal conditioning in low-voltage systems. The TLV2362 provides higher performance than other general-purpose operational amplifiers by combining higher unity-gain bandwidth and faster slew rate. With its low distortion and low noise performance, this device is well suited for audio applications. The TLV2362 is available in the thin-shrink small-outline package (TSSOP) to reduce board space requirements.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
−20°C to 85°C	TLV2362ID	TLV2362IP	TLV2362IPWLE	TLV2362Y

The D packages are available taped and reeled. Add an R to the package suffix (e.g., TLV2362IDR).
The PW packages are only available left-ended taped and reeled, (e.g., TLV2362IPWLE).
Chip forms are specified for operation at 25°C only.

equivalent schematic (each amplifier)

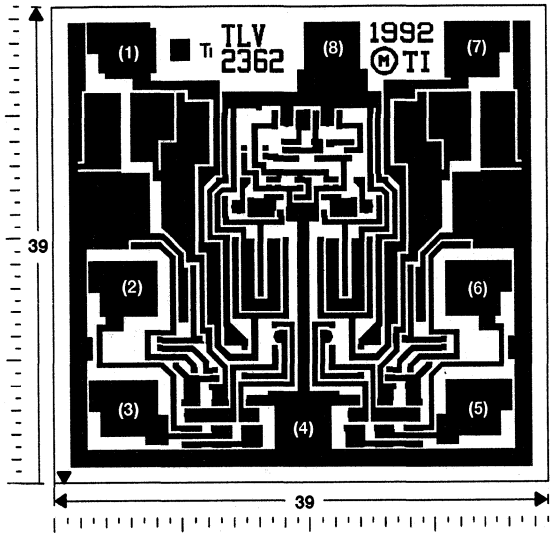


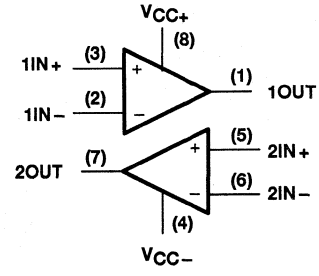
ACTUAL DEVICE COMPONENT COUNT	
Capacitors	4
Diodes	1
Resistors	11
J-FET	1
Transistors	46

TLV2362Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2362. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) ..... 3.5 V
Supply voltage, V_{CC-} (see Note 1) ..... −3.5 V
Differential input voltage, V_{ID} (see Note 2) ..... ±3.5 V
Input voltage, V_I (any input) (see Notes 1 and 3) ..... $V_{CC\pm}$
Output voltage, V_O ..... ±3.5 V
Output current, I_O ..... 20 mA
Duration of short-circuit current at (or below) 25°C (output shorted to GND) ..... unlimited
Continuous total dissipation, P_D ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −20°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. All input voltage values must not exceed V_{CC}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A \le 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	±1	±2.5	V
Operating free-air temperature, T_A	−20	85	°C

electrical characteristics, $V_{CC\pm}$ = ±1.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLV2362I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0	25°C		1	6	mV
			–20°C to 85°C			7.5	
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		5	100	nA
			–20°C to 85°C			150	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		20	150	nA
			–20°C to 85°C			250	
V_{ICR}	Common-mode input voltage	$\|V_{IO}\|$ 3 7.5 mV	25°C	±0.5			V
			–20°C to 85°C	+0.5			
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ	25°C	1.2	1.4		V
		R_L ≥ 10 kΩ	–20°C to 85°C	1.2			
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ	25°C	–1.2	–1.4		V
		R_L ≥ 10 kΩ	–20°C to 85°C	–1.2			
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load	25°C		2.8	4.5	mA
			–20°C to 85°C			5.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V, R_L = 10 kΩ	25°C		55		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V	25°C		75		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V	25°C		80		dB

operating characteristics, $V_{CC\pm}$ = ±1.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2362I			UNIT
			MIN	TYP	MAX	
SR	Slew rate	A_V = 1, V_I = ±0.5 V		2.5		V/μs
B_1	Unity-gain bandwidth	A_V = 40, R_L = 10 kΩ, C_L = 100 pF		6		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω, R_F = 10 kΩ, f = 1 kHz		9		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ±2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLV2362I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0	25°C		1	6	mV
			−20°C to 85°C			7.5	
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		5	100	nA
			−20°C to 85°C			150	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		20	150	nA
			−20°C to 85°C			250	
V_{ICR}	Common-mode input voltage	$\lvert V_{IO}\rvert \le$ 7.5 mV	25°C	±1.5			V
			−20°C to 85°C	±1.4			
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ	25°C	2	2.4		V
		$R_L \ge$ 10 kΩ	−20°C to 85°C	2			
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ	25°C	−2	−2.4		V
		$R_L \ge$ 10 kΩ	−20°C to 85°C	−2			
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load	25°C		3.5	5	mA
			−20°C to 85°C			6	
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V, R_L = 10 kΩ	25°C		60		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V	25°C		85		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V	25°C		80		dB

operating characteristics, $V_{CC\pm}$ = ±2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLV2362I			UNIT
					MIN	TYP	MAX	
SR	Slew rate	A_V = 1,	V_I = ±0.5 V			3		V/μs
B_1	Unity-gain bandwidth	A_V = 40,	R_L = 10 kΩ,	C_L = 100 pF		7		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω,	R_F = 2 kΩ,	f = 1 kHz		8		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ±1.5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0		1	6	mV
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		5	100	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		20	150	nA
V_{ICR}	Common-mode input voltage	$\|V_{IO}\| \leq$ 7.5 mV	±0.5			V
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ	1.2	1.4		V
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ	–1.2	–1.4		
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load		2.8	4.5	mA
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V, R_L = 10 kΩ		55		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V		75		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V		80		dB

operating characteristics, $V_{CC\pm}$ = ±1.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate	A_V = 1, V_I = ±0.5 V		2.5		V/μs
B_1	Unity-gain bandwidth	A_V = 40, R_L = 10 kΩ, C_L = 100 pF		6		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω, R_F = 2 kΩ, f = 1 kHz		9		nV/√Hz

electrical characteristics, $V_{CC\pm}$ = ±2.5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0		1	6	mV
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		5	100	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		20	150	nA
V_{ICR}	Common-mode input voltage	$\|V_{IO}\| \leq$ 7.5 mV	±1.5			V
V_{OM+}	Maximum positive-peak output voltage	R_L = 10 kΩ	2	2.4		V
V_{OM-}	Maximum negative-peak output voltage	R_L = 10 kΩ	–2	–2.4		
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load		3.5	5	mA
A_{VD}	Large-signal differential voltage amplification	V_O = ± 1 V, R_L = 10 kΩ		60		dB
CMRR	Common-mode rejection ratio	V_{IC} = ± 0.5 V		85		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ± 1.5 V to ± 2.5 V		80		dB

operating characteristics, $V_{CC\pm}$ = ±2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2362Y			UNIT
			MIN	TYP	MAX	
SR	Slew rate	A_V = 1, V_I = ±0.5 V		3		V/μs
B_1	Unity-gain bandwidth	A_V = 40, R_L = 10 kΩ, C_L = 100 pF		7		MHz
V_n	Equivalent input noise voltage	R_S = 20 Ω, R_F = 2 kΩ, f = 1 kHz		8		nV/√Hz

SLOS094A – NOVEMBER 1970 – REVISED JANUARY 1992

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Fairchild μA741**

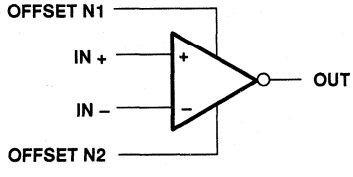
description

The μA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

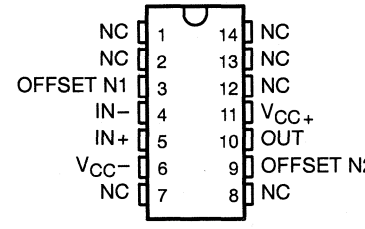
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The μA741C is characterized for operation from 0°C to 70°C. The μA741I is characterized for operation from −40°C to 85°C.The μA741M is characterized for operation over the full military temperature range of −55°C to 125°C.

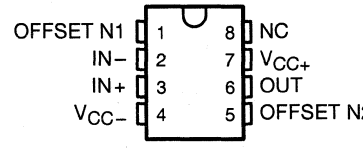
symbol



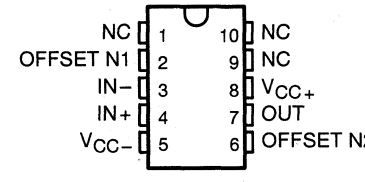
μA741M . . . J PACKAGE
(TOP VIEW)



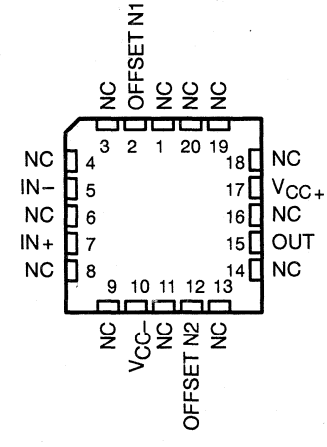
μA741M . . . JG PACKAGE
μA741C, μA741I . . . D, P, OR PW PACKAGE
(TOP VIEW)



μA741M . . . U PACKAGE
(TOP VIEW)



μA741M . . . FK PACKAGE
(TOP VIEW)



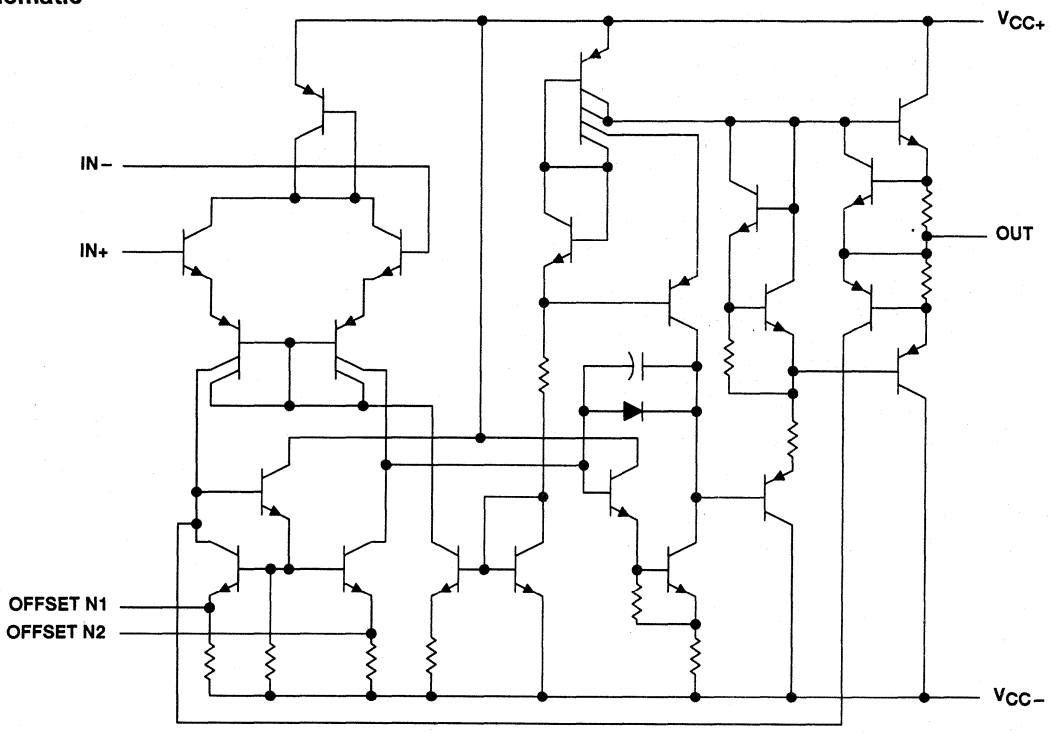
NC – No internal connection

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES							CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	
0°C to 70°C	uA741CD				uA741CP	uA741CPW		uA741Y
−40°C to 85°C	uA741ID				uA741IP			
−55°C to 125°C		uA741MFK	uA741MJ	uA741MJG			uA741MU	

The D package is available taped and reeled. Add the suffix R (e.g., uA741CDR).

schematic

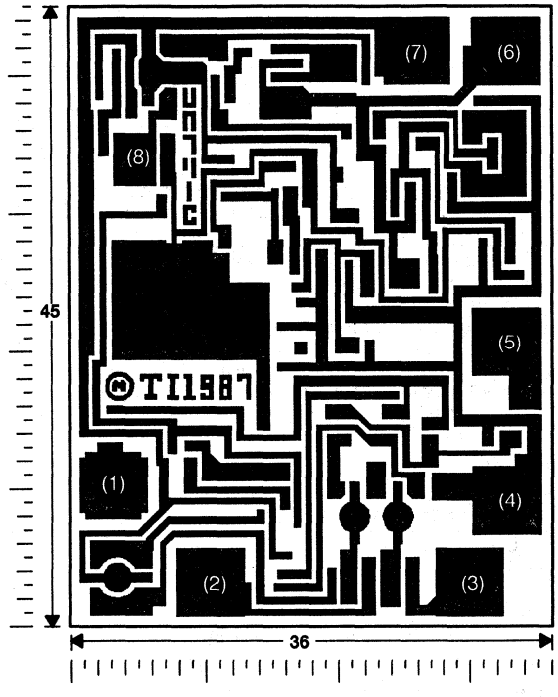


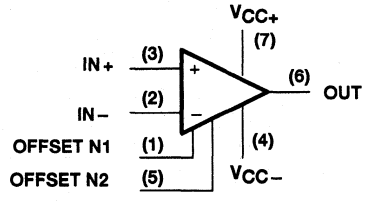
Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

μA741Y chip information

This chip, when properly assembled, displays characteristics similar to the μA741C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C.

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		μA741C	μA741I	μA741M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	22	22	V
Supply voltage, V_{CC-} (see Note 1)		−18	−22	−22	V
Differential input voltage, V_{ID} (see Note 2)		±15	±30	±30	V
Input voltage, V_I any input (see Notes 1 and 3)		±15	±15	±15	V
Voltage between offset null (either OFFSET N1 or OFFSET N2) and V_{CC-}		±15	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range, T_A		0 to 70	−40 to 85	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, P, or PW package	260	260		°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the μA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
PW	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	μA741C			μA741I, μA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6		1	5	mV
			Full range			7.5			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15			±15		mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		$R_L \geq$ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		$R_L \geq$ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ	25°C	20	200		50	200		V/mV
		V_O = ±10 V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	V_O = 0, No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	V_O = 0, No load	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the μA741C is 0°C to 70°C, the μA741I is –40°C to 85°C, and the μA741M is –55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		μA741C			μA741I, μA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,		0.5			0.5		V/μs
		C_L = 100 pF,	See Figure 1							

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0		1	6	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0		±15		mV
I_{IO}	Input offset current	V_O = 0		20	200	nA
I_{IB}	Input bias current	V_O = 0		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	±12	±14		V
		R_L = 2 kΩ	±10	±13		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 5		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		30	150	μV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	V_O = 0, No load		1.7	2.8	mA
P_D	Total power dissipation	V_O = 0, No load		50	85	mW

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3		μs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

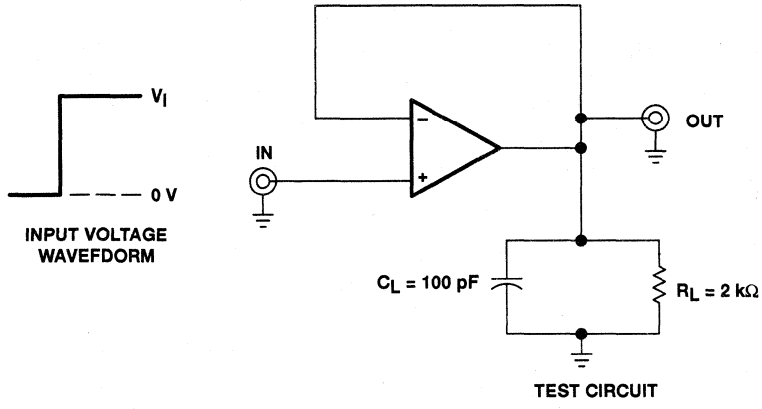


Figure 1. Rise Time, Overshoot, and Slew Rate

APPLICATION INFORMATION

Figure 2 shows a diagram for an input offset voltage null circuit.

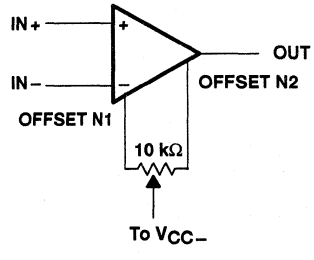


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

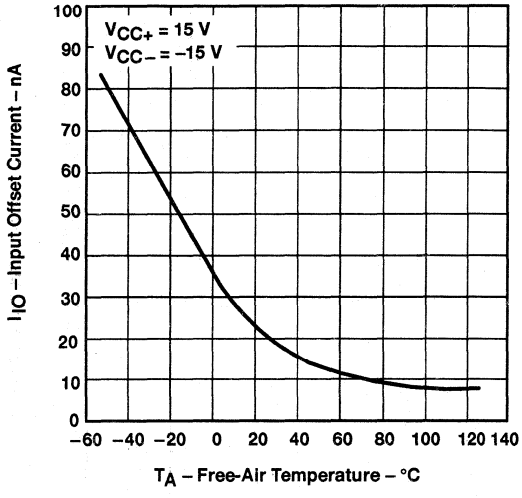


Figure 3

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

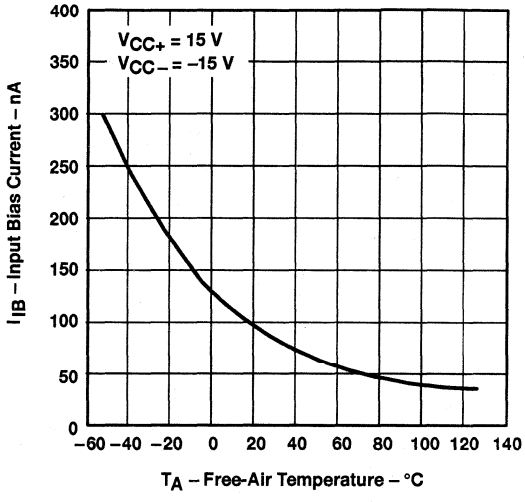


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

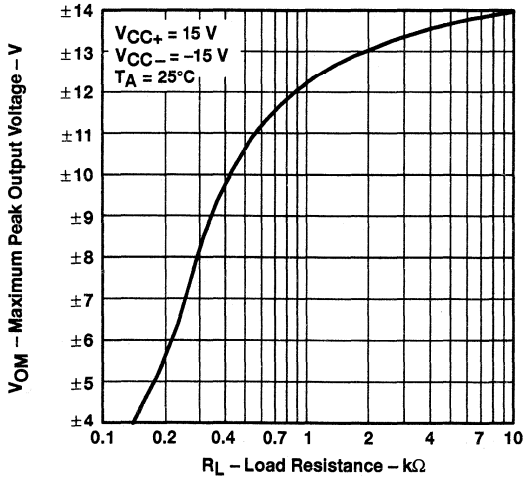


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

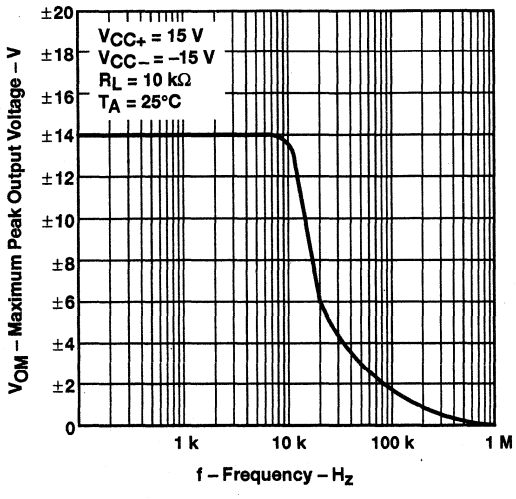


Figure 6

OPEN-LOOP SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

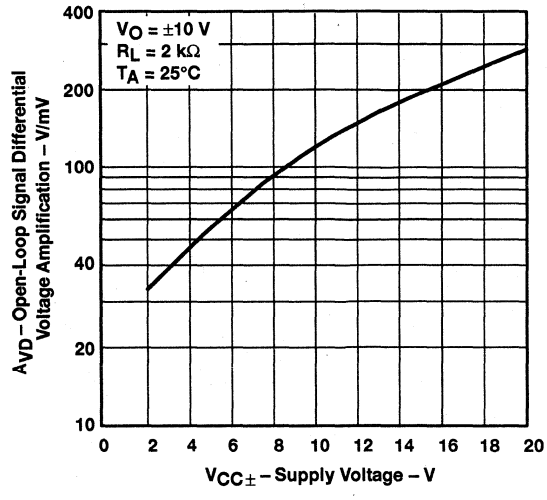


Figure 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

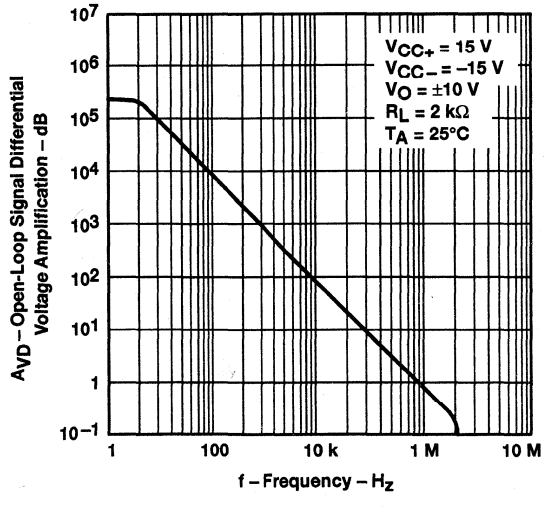


Figure 8

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

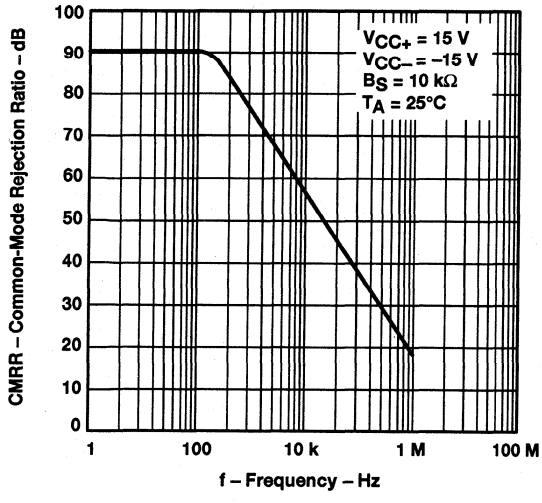


Figure 9

OUTPUT VOLTAGE vs ELAPSED TIME

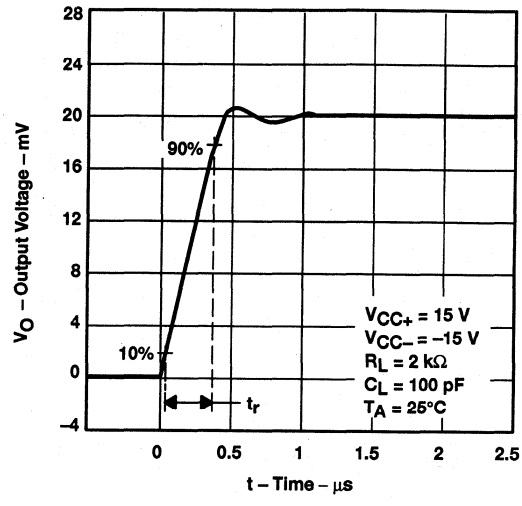


Figure 10

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

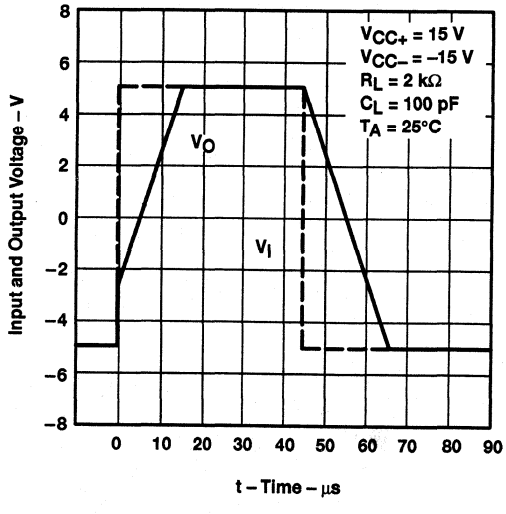


Figure 11

General Information (Volume A) 1
Operational Amplifiers 2
Mechanical Data (Volume A) 3
General Information (Volume B) 4
Operational Amplifiers (continued) 5
Comparators 6
Mechanical Data (Volume B) 7

6 Comparators

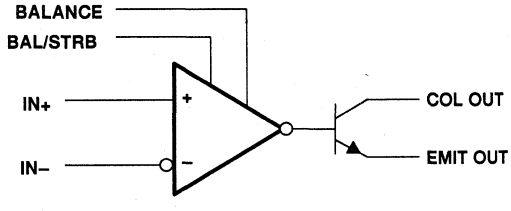
- **Fast Response Times**
- **Strobe Capability**
- **Maximum Input Bias Current . . . 300 nA**
- **Maximum Input Offset Current . . . 70 nA**
- **Can Operate From Single 5-V Supply**
- **Designed to Be Interchangeable With National Semiconductor LM111, LM211, and LM311**

description

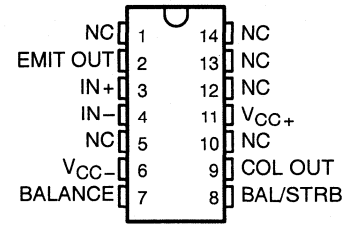
The LM111, LM211, and LM311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltages, including ±15-V supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+} or V_{CC-}. Offset balancing and strobe capabilities are available, and the outputs can be wire-OR connected. If the strobe is low, the output will be in the off state regardless of the differential input.

The LM111 is characterized for operation over the full military range of −55°C to 125°C. The LM211 is characterized for operation from −40°C to 85°C, and the LM311 is characterized for operation from 0°C to 70°C.

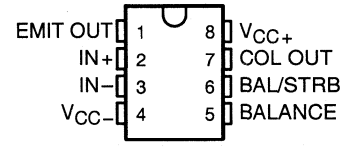
functional block diagram



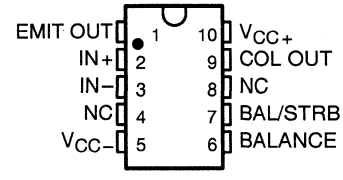
LM111 . . . J PACKAGE
(TOP VIEW)



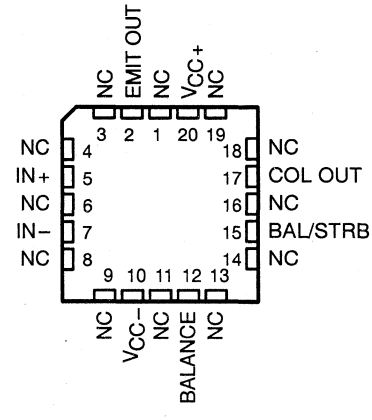
LM111 . . . JG PACKAGE
LM211, LM311 . . . D, DB, P, OR PW PACKAGE
(TOP VIEW)



LM111 . . . U PACKAGE
(TOP VIEW)



LM111 . . . FK PACKAGE
(TOP VIEW)



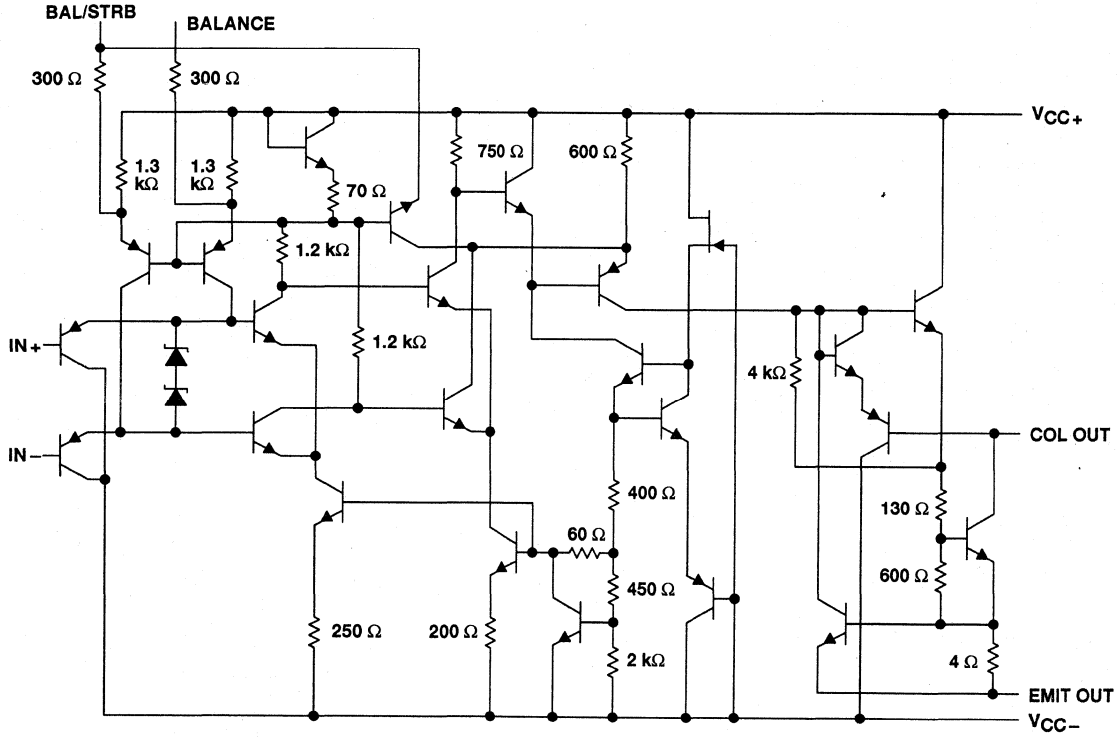
NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGED DEVICES								CHIP FORM (Y)
		SMALL OUTLINE (D)†	SSOP (DB)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FLATPACK (U)	
0°C to 70°C	7.5 mV	LM311D	LM311DBLE				LM311P	LM311PWLE		LM311Y
−40°C to 85°C	3 mV	LM211D					LM211P			
−55°C to 125°C	3 mV			LM111FK	LM111J	LM111JG			LM111U	

† The D package is available taped and reeled. Add the suffix R (e.g., LM311DR). The DB and PW packages are only available left-end taped and reeled.

schematic



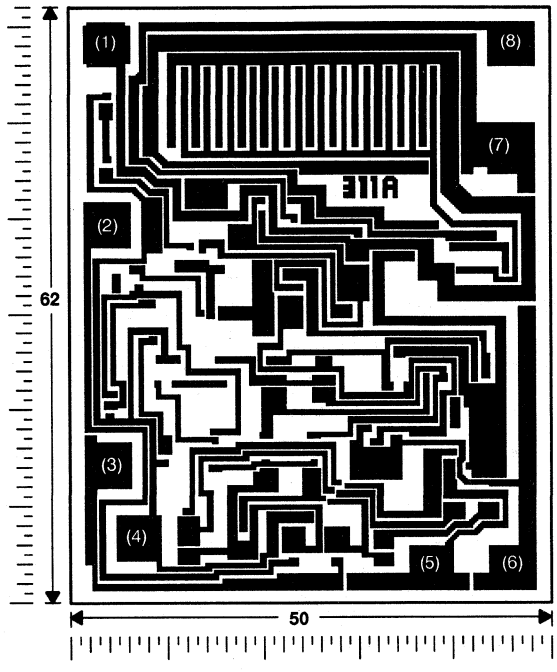
Component Count	
Resistors	20
Diodes	2
Epifet	1
Transistors	22

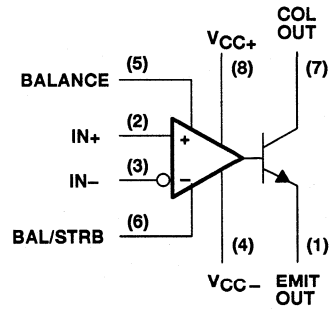
All resistor values shown are nominal.

LM311Y chip information

This chip, when properly assembled, displays characteristics similar to the LM311. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 18 V
Supply voltage, V_{CC-} (see Note 1) ..... −18 V
Supply voltage, $V_{CC+} - V_{CC-}$ ..... 36 V
Differential input voltage, V_{ID} (see Note 2) ..... ±30 V
Input voltage, V_I (either input, see Notes 1 and 3) ..... ±15 V
Voltage from emitter output to V_{CC-} ..... 30 V
Voltage from collector output to V_{CC-}: LM111 ..... 50 V
LM211 ..... 50 V
LM311 ..... 40 V
Duration of output short circuit (see Note 4) ..... 10 s
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: LM111 ..... −55°C to 125°C
LM211 ..... −40°C to 85°C
LM311 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or U package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, DB, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	–
DB or PW	500 mW	4.2 mW/°C	31°C	336 mW	–	–
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	–
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC+} - V_{CC-}$		3.5	30	V
Input voltage ($\lvert V_{CC\pm}\rvert \le 15$ V)		$V_{CC-} + 0.5$	$V_{CC+} - 1.5$	V
Operating free-air temperature range, T_A	LM111	−55	125	°C
	LM211	−40	85	
	LM311	0	70	

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LM111, LM211			LM311			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	See Note 5		25°C		0.7	3		2	7.5	mV
				Full range			4			10	
I_{IO}	Input offset current	See Note 5		25°C		4	10		6	50	nA
				Full range			20			70	
I_{IB}	Input bias current	V_O = 1 V to 14 V		25°C		75	100		100	250	nA
				Full range			150			300	
$I_{IL(S)}$	Low-level strobe current (see Note 6)	$V_{(strobe)}$ = 0.3 V,	$V_{ID} \le -10$ mV	25°C		−3			−3		mA
V_{ICR}	Common-mode input voltage range			Full range	13 to −14.5	13.8 to −14.7		13 to −14.5	13.8 to −14.7		V
A_{VD}	Large-signal differential voltage amplification	V_O = 5 V to 35 V,	R_L = 1 kΩ	25°C	40	200		40	200		V/mV
I_{OH}	High-level (collector) output current	$I_{(strobe)}$ = −3 mA, V_{ID} = 5 mV,	V_{OH} = 35 V	25°C		0.2	10				nA
				Full range			0.5				μA
		V_{ID} = 5 mV,	V_{OH} = 35 V	25°C					0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	I_{OL} = 50 mA	V_{ID} = −5 mV	25°C		0.75	1.5				V
			V_{ID} = −10 mV	25°C					0.75	1.5	
		V_{CC+} = 4.5 V, V_{CC-} = 0, I_{OL} = 8 mA	V_{ID} = −6 mV	Full range		0.23	0.4				
			V_{ID} = −10 mV	Full range					0.23	0.4	
I_{CC+}	Supply current from V_{CC+}, output low	V_{ID} = −10 mV,	No load	25°C		5.1	6		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-}, output high	V_{ID} = 10 mV,	No load	25°C		−4.1	−5		−4.1	−5	mA

† Unless otherwise noted, all characteristics are measured with BALANCE and BAL/STRB open and the emitter output grounded. Full range for LM111 is −55°C to 125°C, for LM211 is −40°C to 85°C, and for LM311 is 0°C to 70°C.

‡ All typical values are at T_A = 25°C.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pullup resistor of 7.5 kΩ to V_{CC+}. These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. The strobe should not be shorted to ground; it should be current driven at −3 mA to −5 mA (see Figures 13 and 27).

switching characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LM111, LM211, LM311			UNIT
		MIN	TYP	MAX	
Response time, low-to-high-level output	R_C = 500 Ω to 5 V, C_L = 5 pF, See Note 7		115		ns
Response time, high-to-low-level output			165		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	LM311Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 5		2	7.5	mV
I_{IO}	Input offset current	See Note 5		6	50	nA
I_{IB}	Input bias current	V_O = 1 V to 14 V		100	250	nA
$I_{IL(S)}$	Low-level strobe current (see Note 6)	$V_{(strobe)}$ = 0.3 V, $V_{ID} \le -10$ mV		−3		mA
V_{ICR}	Common-mode input voltage range		13 to −14.5	13.8 to −14.7		V
A_{VD}	Large-signal differential voltage amplification	V_O = 5 V to 35 V, R_L = 1 kΩ	40	200		V/mV
I_{OH}	High-level (collector) output current	I_{strobe} = −3 mA, V_{ID} = 5 mV, V_{OH} = 35 V		0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	I_{OL} = 50 mA, V_{ID} = −10 mV		0.75	1.5	V
I_{CC+}	Supply current from V_{CC+}, output low	V_{ID} = −10 mV, No load		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-}, output low	V_{ID} = 10 mV, No load		−4.1	−5	mA

† Unless otherwise noted, all characteristics are measured with BALANCE and BAL/STRB open and the emitter output grounded.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pullup resistor of 7.5 kΩ to V_{CC+}. These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. The strobe should not be shorted to ground; it should be current driven at −3 mA to −5 mA (see Figures 13 and 27).

switching characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LM311Y			UNIT
		MIN	TYP	MAX	
Response time, low-to-high-level output	R_C = 500 Ω to 5 V, C_L = 5 pF, See Note 7		115		ns
Response time, high-to-low-level output			165		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

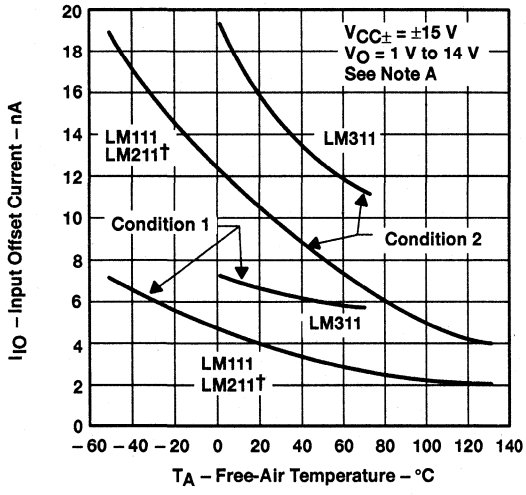


Figure 1

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

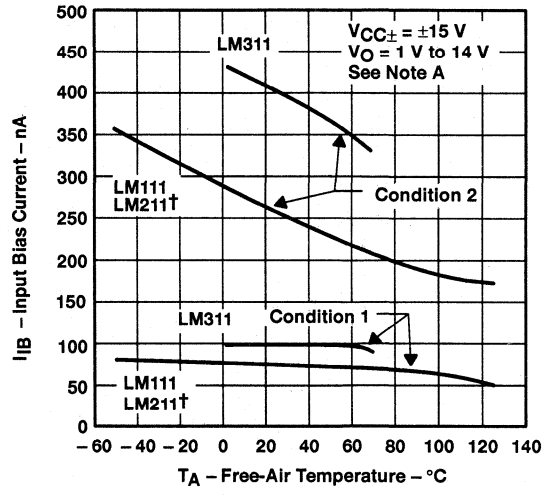
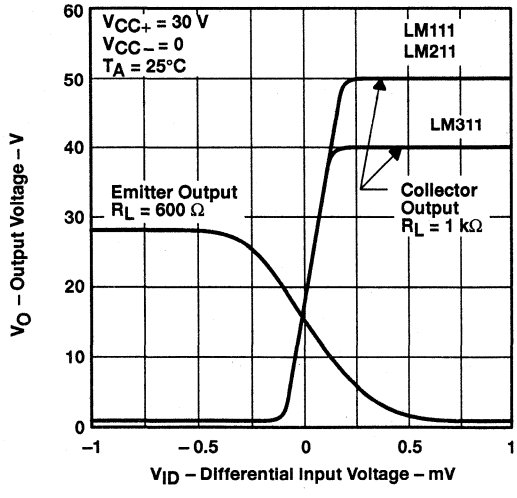
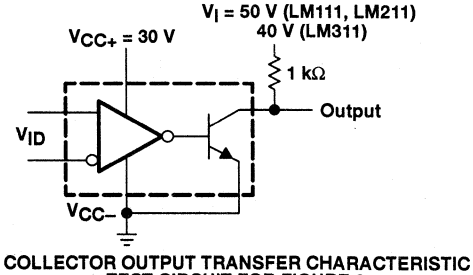


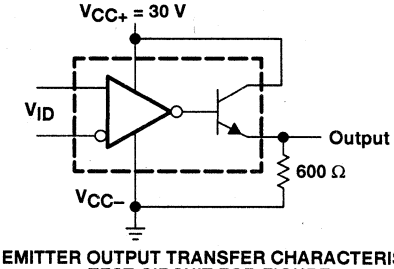
Figure 2

VOLTAGE TRANSFER CHARACTERISTICS





COLLECTOR OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3



EMITTER OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3

Figure 3

NOTE A: Condition 1 is with BALANCE and BAL/STRB open. Condition 2 is with BALANCE and BAL/STRB connected to V_{CC+}.

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

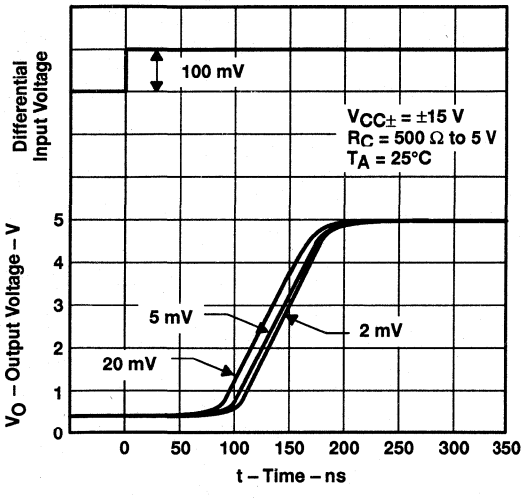


Figure 4

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

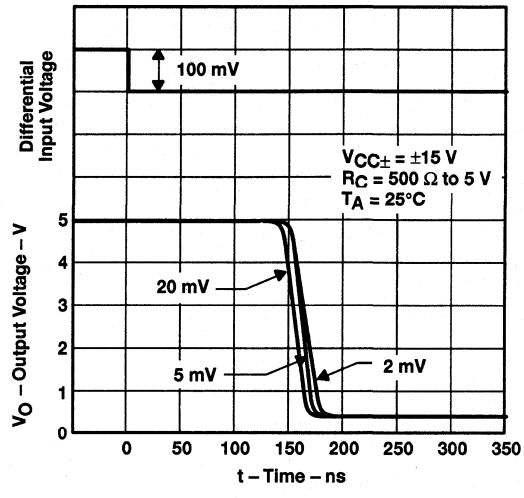
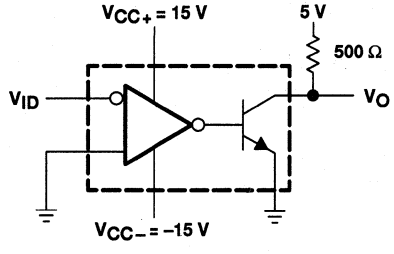


Figure 5



TEST CIRCUIT FOR FIGURES 4 AND 5

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

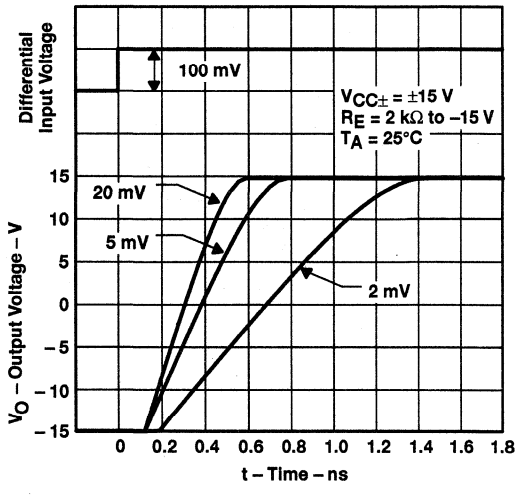


Figure 6

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

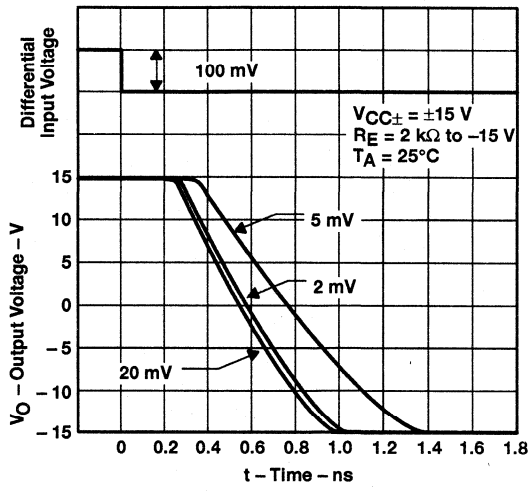
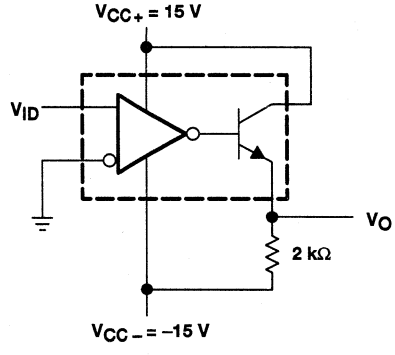


Figure 7



TEST CIRCUIT FOR FIGURES 6 AND 7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT AND DISSIPATION vs OUTPUT VOLTAGE

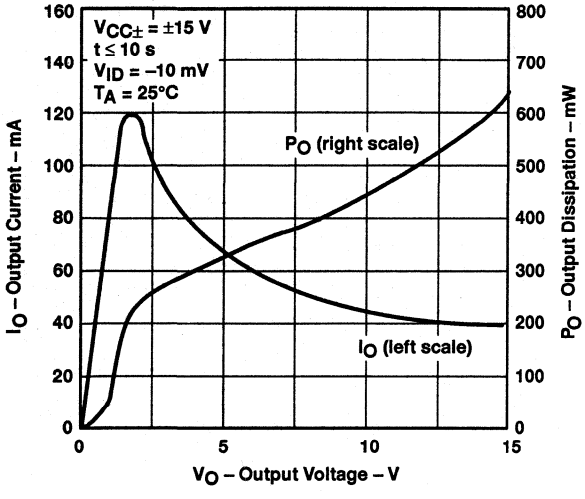


Figure 8

POSITIVE SUPPLY CURRENT vs POSITIVE SUPPLY VOLTAGE

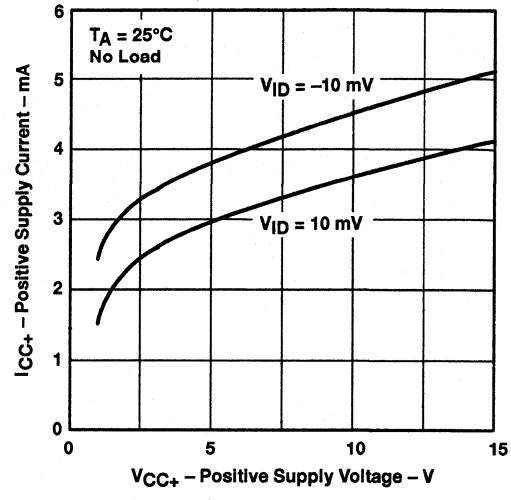


Figure 9

NEGATIVE SUPPLY CURRENT vs NEGATIVE SUPPLY VOLTAGE

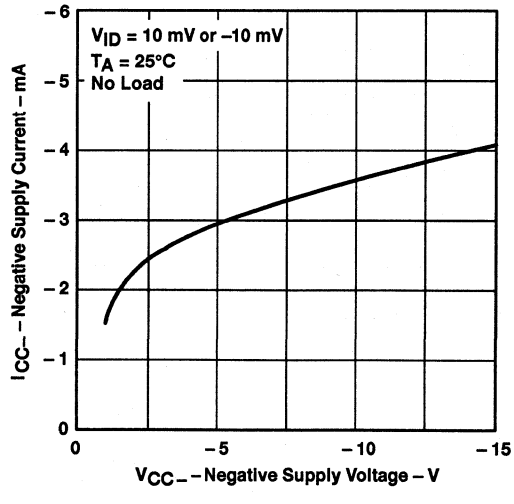


Figure 10

APPLICATION INFORMATION

Figure 11 through Figure 29 show various applications for the LM111, LM211, and LM311 comparators.

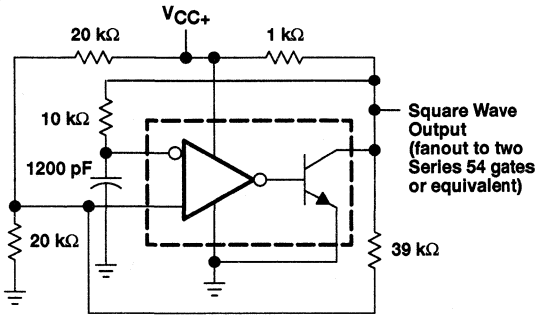


Figure 11. 100-kHz Free-Running Multivibrator

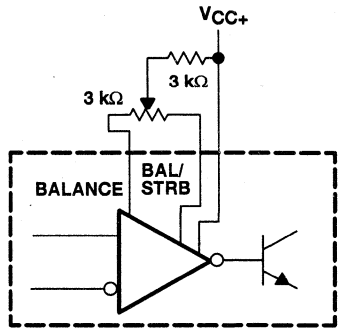


Figure 12. Offset Balancing

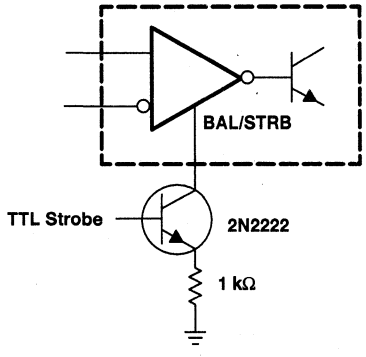


Figure 13. Strobing

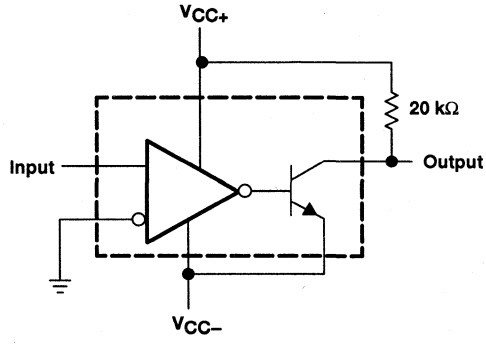
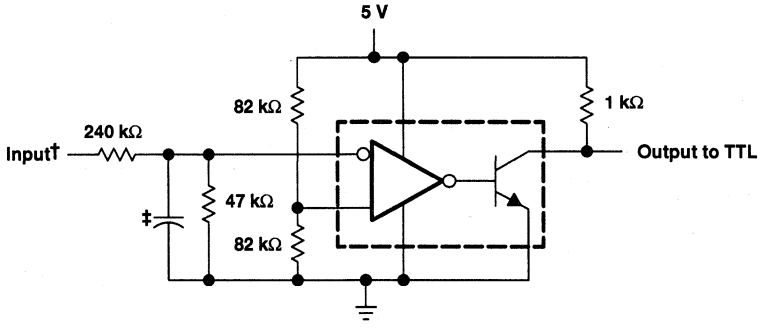


Figure 14. Zero-Crossing Detector



† Resistor values shown are for a 0-to-30-V logic swing and a 15-V threshold.
‡ May be added to control speed and reduce susceptibility to noise spikes.

Figure 15. TTL Interface With High-Level Logic

APPLICATION INFORMATION

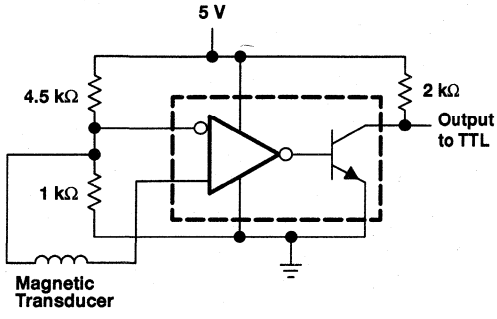


Figure 16. Detector for Magnetic Transducer

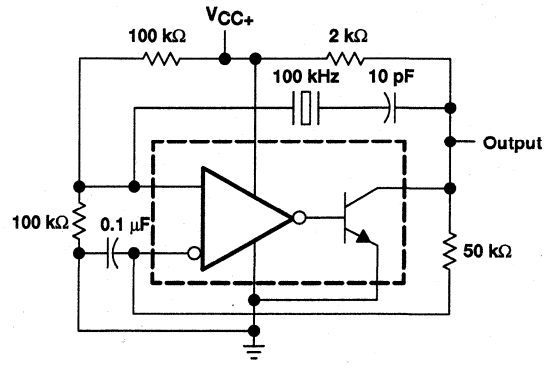


Figure 17. 100-kHz Crystal Oscillator

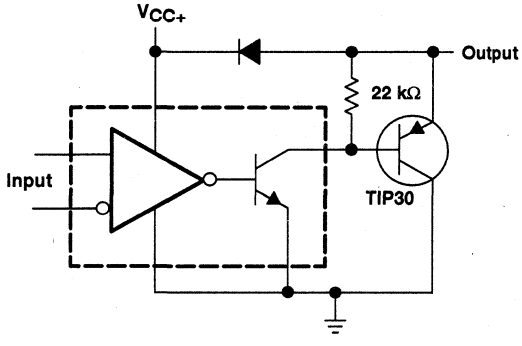
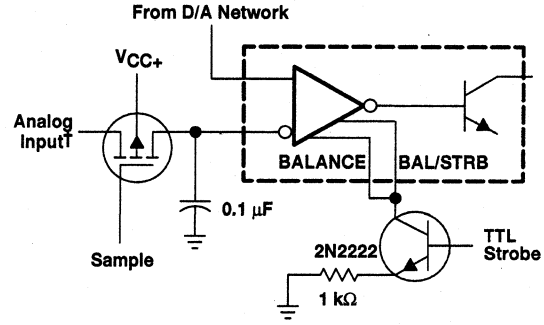


Figure 18. Comparator and Solenoid Driver



†Typical input current is 50 pA with inputs strobed off.

Figure 19. Strobing Both Input and Output Stages Simultaneously

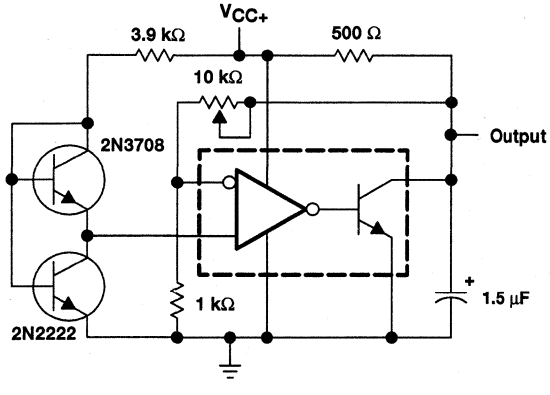


Figure 20. Low-Voltage Adjustable Reference Supply

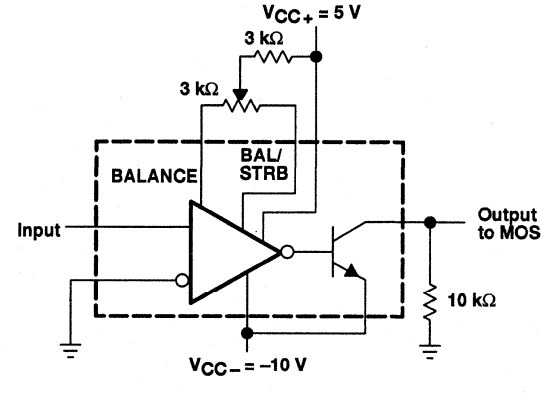
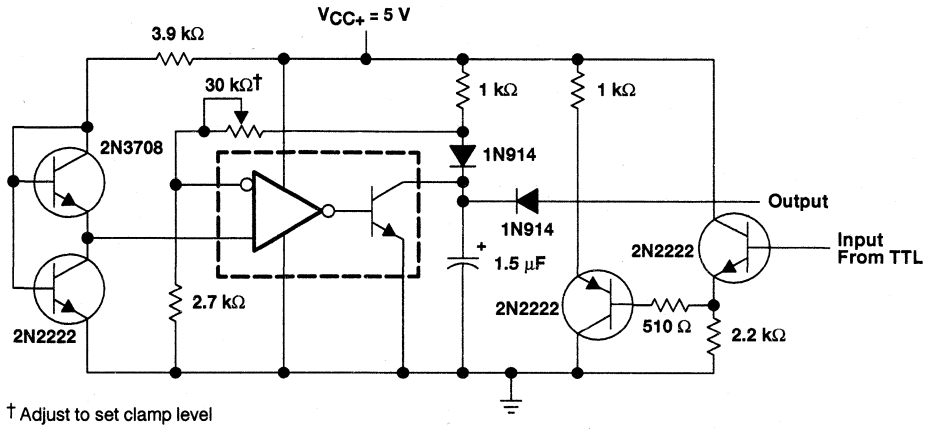


Figure 21. Zero-Crossing Detector Driving MOS Logic

APPLICATION INFORMATION



† Adjust to set clamp level

Figure 22. Precision Squarer

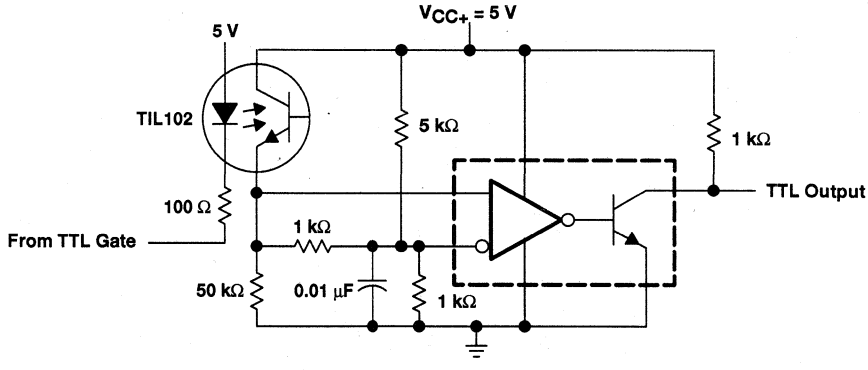


Figure 23. Digital Transmission Isolator

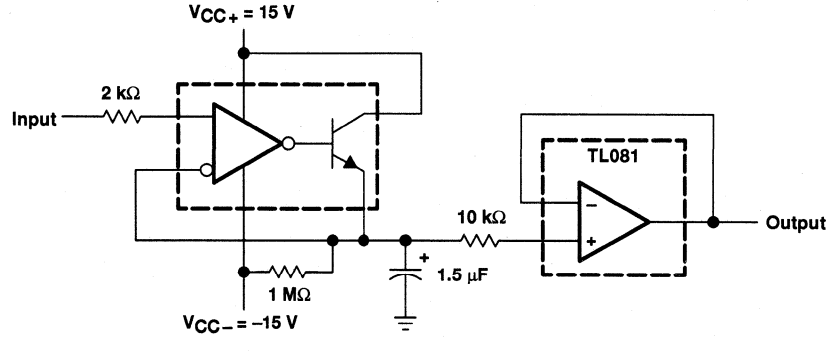


Figure 24. Positive-Peak Detector

APPLICATION INFORMATION

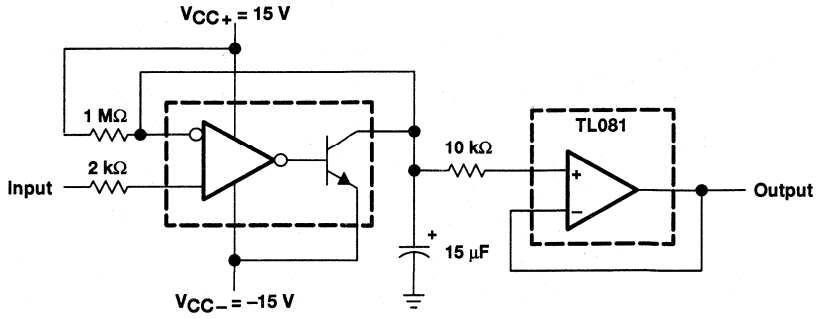
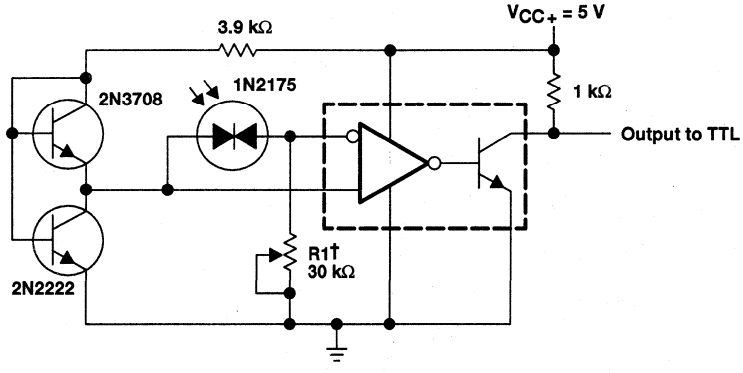
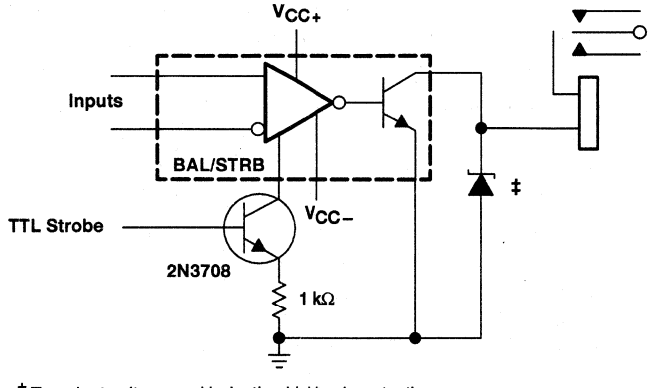


Figure 25. Negative-Peak Detector



† R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it decreasing dark current by an order of magnitude.

Figure 26. Precision Photodiode Comparator



‡ Transient voltage and inductive kickback protection

Figure 27. Relay Driver With Strobe

APPLICATION INFORMATION

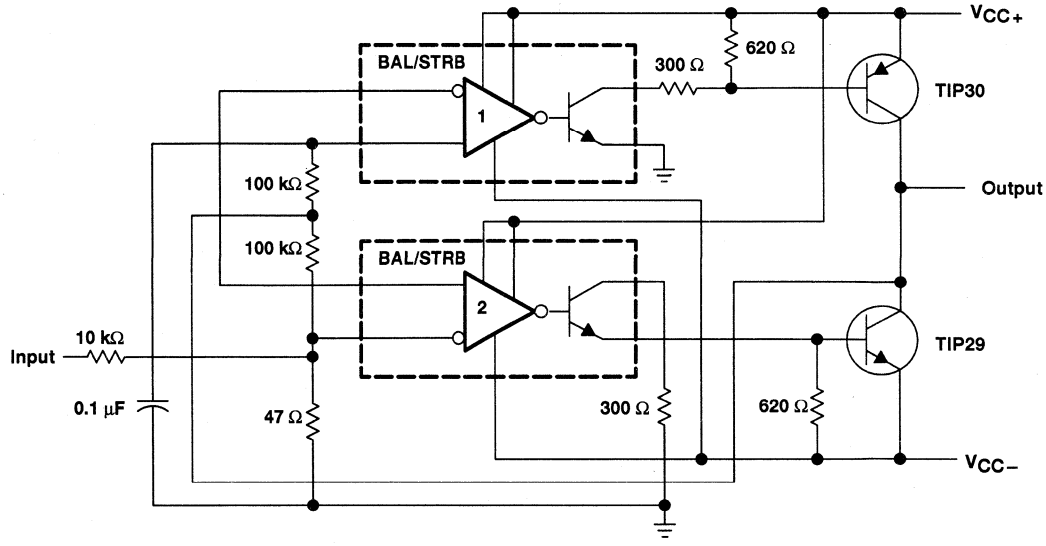


Figure 28. Switching Power Amplifier

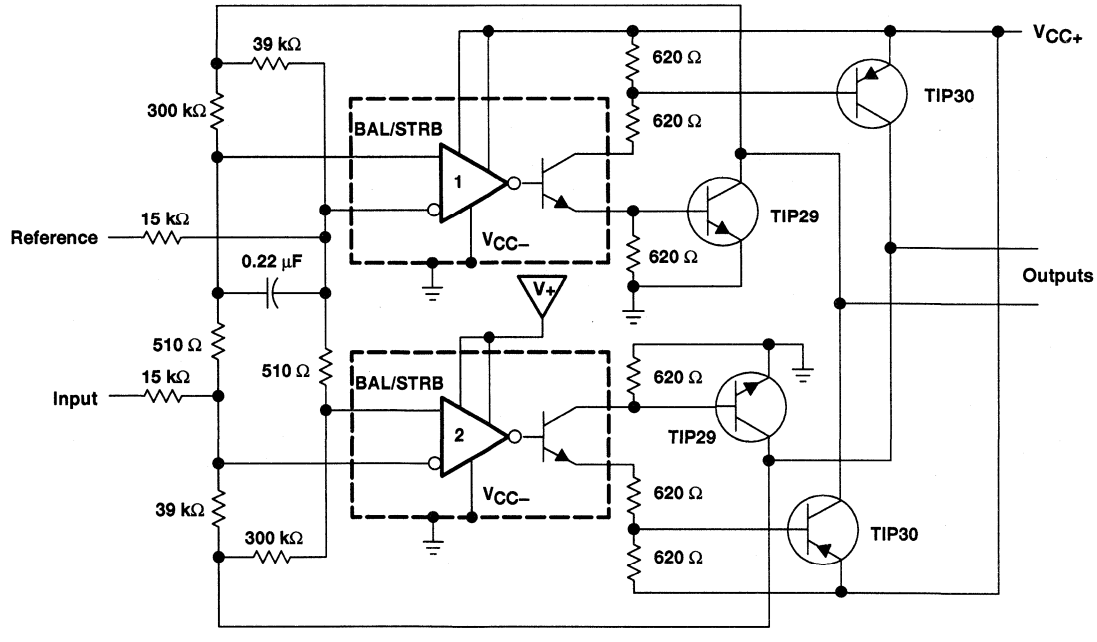


Figure 29. Switching Power Amplifiers

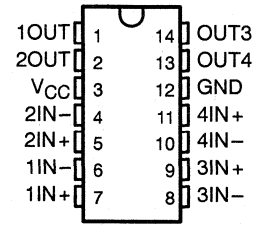
- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage 2 V to 36 V**
- **Low Supply-Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Low Input Bias Current . . . 25 nA Typ**
- **Low Input Offset Current . . . 3 nA Typ (LM139)**
- **Low Input Offset Voltage . . . 2 mV Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V**
- **Low Output-Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

description

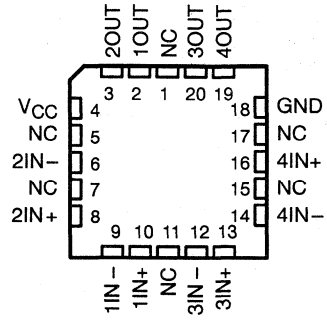
These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wire-AND relationships.

The LM139 and LM139A are characterized for operation from −55°C to 125°C. The LM239 and LM239A are characterized for operation from −25°C to 125°C. The LM339 and LM339A are characterized for operation from 0°C to 70°C. The LM2901 and LM2901Q are characterized for operation from −40°C to 85°C.

D, DB, J, N, OR PW PACKAGE
(TOP VIEW)

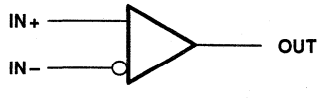


FK PACKAGE
(TOP VIEW)



NC – No internal connection

symbol (each comparator)

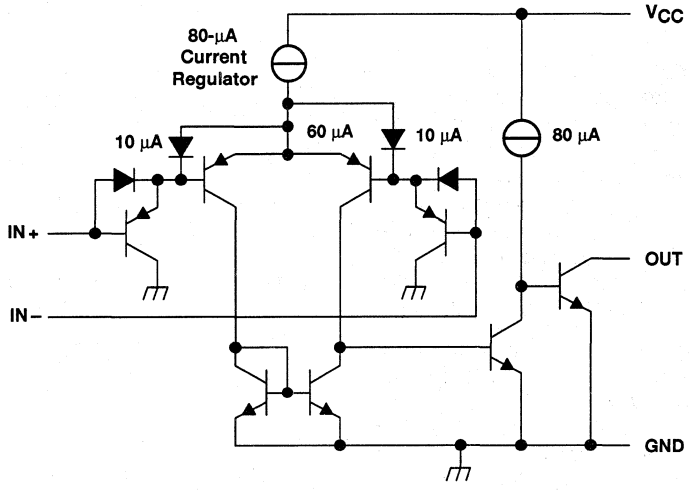


AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGED DEVICES						CHIP FORM (Y)§
		SMALL OUTLINE (D)†	SSOP (DB)‡	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)‡	
0°C to 70°C	5 mV 2 mV	LM339D LM339AD	LM339DBLE —	—	—	LM339N LM339AN	LM339PWLE —	LM339Y
−25°C to 85°C	5 mV 2 mV	LM239D LM239AD	—	—	—	LM239N LM239AN	—	—
−40°C to 125°C	7 mV	LM2901D LM2901QD	LM2901DBLE —	—	—	LM2901QN	LM2901PWLE —	—
−55°C to 125°C	5 mV 2 mV	LM139D LM139AD	—	LM139AFK	LM139J LM139AJ	LM139N LM139AN	—	—

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., LM339DR).
‡ The DB and PW packages are only available left-end taped and reeled.
§ Chips are tested at 25°C (see electrical characteristics).

schematic (each comparator)

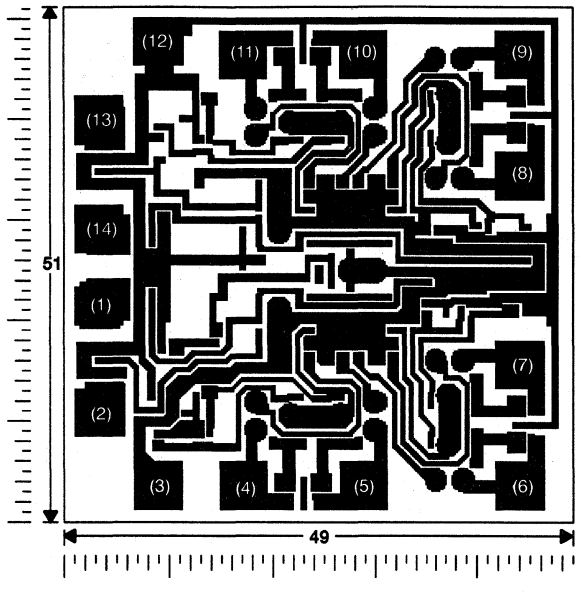


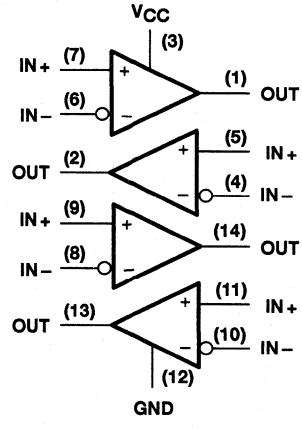
All current values shown are nominal.

LM339Y chip information

This chip, when properly assembled, displays characteristics similar to the LM339. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 36 V
Differential input voltage, V_{ID} (see Note 2) ..... ±36 V
Input voltage range, V_I (either input) ..... −0.3 V to 36 V
Output voltage, V_O ..... 36 V
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: LM139, LM139A ..... −55°C to 125°C
LM239, LM239A ..... −25°C to 85°C
LM339, LM339A ..... 0°C to 70°C
LM2901, LM2901Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, N, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	31°C	608 mW	494 mW	—
DB	775 mW	6.2 mW/°C	25°C	496 mW	403 mW	155 mW
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	—
PW	700 mW	5.6 mW/°C	25°C	448 mW	364 mW	140 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LM139			LM139A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V	$V_{IC} = V_{ICR}$min,	25°C		2	5		1	2	mV
				−55°C to 125°C			9			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		3	25	nA
				−55°C to 125°C			100			100	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−100		−25	−100	nA
				−55°C to 125°C			−300			−300	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				−55°C to 125°C	0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC}± = ± 7.5 V,	V_O = −5 V to 5 V	25°C		200		50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 30 V	−55°C to 125°C			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				−55°C to 125°C			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	25°C		0.8	2		0.8	2	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		LM139, LM139A			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 4	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

‡ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	LM239, LM339			LM239A, LM339A			LM2901, LM2901Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$min, V_O = 1.4 V		25°C		2	5		1	2		2	7	mV
				Full range			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50		5	50		5	50	nA
				Full range			150			150			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−250		−25	−250		−25	−250	nA
				Full range			−400			−400			−500	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15\ k\Omega$ to V_{CC}		25°C	50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1	50		0.1	50		0.1	50	nA
			V_{OH} = 30 V	Full range			1			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	500	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	25°C		0.8	2		0.8	2		0.8	2	mA
		V_{CC} = 30 V, No load	V_O = 2.5 V,									1	2.5	

† Full range (MIN to MAX) for LM239 and LM239A is −25°C to 85°C, for LM339 and LM339A is 0°C to 70°C, and for LM2901 is −40°C to 125°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		LM239, LM239A LM339, LM339A LM2901, LM2901Q			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 4	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

‡ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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electrical characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM339Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V	V_{IC} = V_{ICR}min,		2	5	mV
I_{IO}	Input offset current	V_O = 1.4 V			5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V			−25	−250	nA
V_{ICR}	Common-mode input voltage range			0 to V_{CC}−1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, $R_L \geq 15\ k\Omega$ to V_{CC}	V_O = 1.4 V to 11.4 V,	25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V		0.1	50	nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load		0.8	2	mA
		V_O = 30 V, No load	V_O = 15 V,		1	2.5	

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

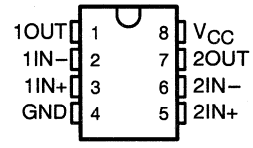
PARAMETER	TEST CONDITIONS		LM339Y			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 4	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

‡ C_L includes probe and jig capacitance.

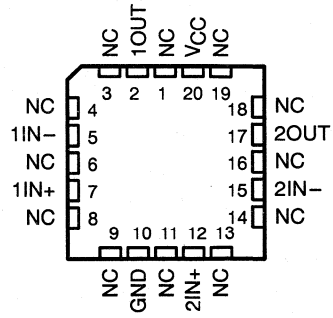
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage . . . 2 to 36 V**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ**
- **Low Input Bias Current . . . 25 nA Typ**
- **Low Input Offset Current . . . 3 nA Typ (LM193)**
- **Low Input Offset Voltage . . . 2 mV Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V**
- **Low Output Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



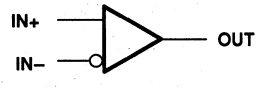
NC – No internal connection

description

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

The LM193 is characterized for operation from –55°C to 125°C. The LM293 and LM293A are characterized for operation from –25°C to 85°C. The LM393 and LM393A are characterized for operation from 0°C to 70°C. The LM2903 and LM2903Q are characterized for operation from –40°C to 125°C and is manufactured to demanding automotive requirements.

symbol (each comparator)



AVAILABLE OPTIONS

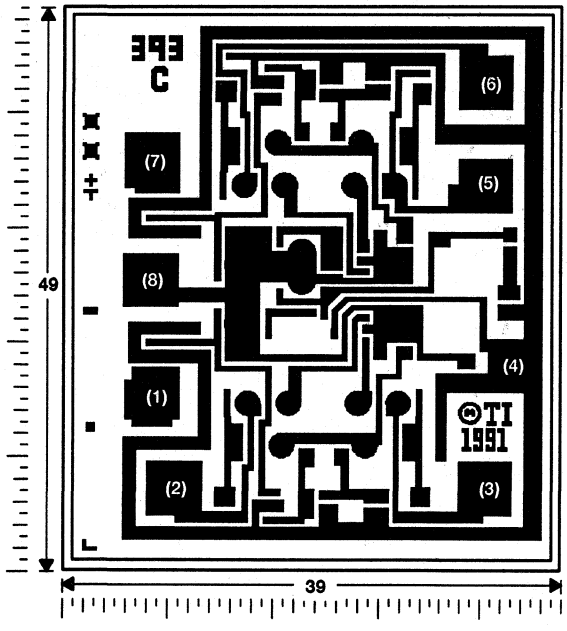
T_A	V_{IO}max at 25°C	PACKAGED DEVICES						CHIP FORM (Y)§
		SMALL OUTLINE (D)†	SSOP (DB)‡	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)‡	
0°C to 70°C	5 mV 2 mV	LM393D LM393AD	LM393DB —	—	—	LM393P LM393AP	LM393PW —	LM393Y
−25°C to 85°C	5 mV 2 mV	LM293D LM293AD	—	—	—	LM293P LM293AP	—	—
−40°C to 125°C	7 mV	LM2903D LM2903QD	LM2903DB —	—	—	LM2903P LM2903QP	LM2903PW —	—
−55°C to 125°C	5 mV	LM193D	—	LM193FK	LM193JG	LM193P	—	—

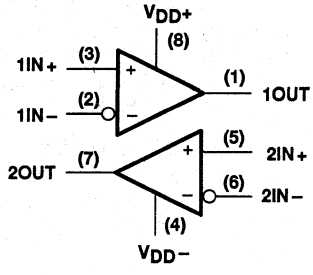
† The D package is available taped and reeled. Add the suffix R (e.g., LM393DR).
‡ The DB and PW packages are only available left-end taped and reeled. Add suffix LE (e.g., LM393DBLE).
§ Chips are tested at 25°C (see LM393Y for electrical characteristics.

LM393Y chip information

This chip, when properly assembled, displays characteristics similar to the LM393. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 3.6 × 3.6 MINIMUM

$T_J$max = 150°C

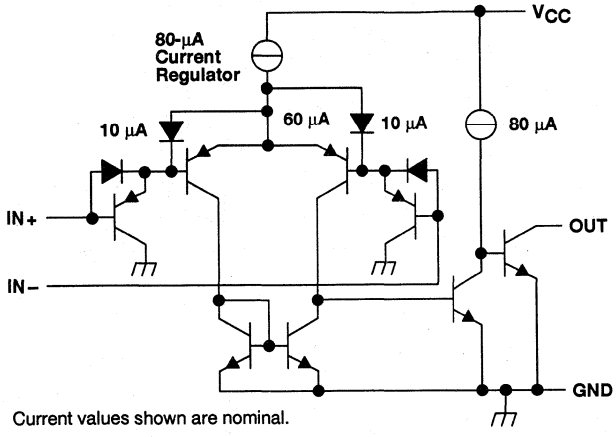
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

NO BACKSIDE METALLIZATION

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

schematic (each comparator)



Current values shown are nominal.

Component Count	
Epi-SET	1
Diodes	2
Resistors	2
Transistors	30

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 36 V
Differential input voltage, V_{ID} (see Note 2) ..... ±36 V
Input voltage range, V_I (either input) ..... −0.3 V to 36 V
Output voltage, V_O ..... 36 V
Output current, I_O ..... 20 mA
Duration of output short-circuit to ground (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: LM193 ..... −55°C to 125°C
LM293, LM293A ..... −25°C to 85°C
LM393, LM393A ..... 0°C to 70°C
LM2903, LM2903Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DB, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	25°C	464 mW	377 mW	145 mW
DB	525 mW	4.2 mW/°C	25°C	336 mW	273 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
JG	900 mW	8.4 mW/°C	43°C	672 mW	546 mW	210 mW
P	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	200 mW
PW	525 mW	4.2 mW/°C	25°C	336 mW	273 mW	N/A

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TAT	LM193			LM293, LM393			LM293A, LM393A			LM2903, LM2903Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{IC}$ min, V_O = 1.4 V		25°C		2	5		2	5		1	2		2	7	mV
				Full range			9			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		5	50		5	50		5	50	nA
				Full range			100			100			150			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−10 0		−25	−25 0		−25	−25 0		−25	−25 0	nA
				Full range			−30 0			−40 0			−40 0			−50 0	
V_{IO}	Common-mode input voltage range‡			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15\ k\Omega$ to V_{CC}		25°C	50	200		50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V	25°C		0.1			0.1	50		0.1	50		0.1	50	nA
		V_{OH} = 30 V,	V_{ID} = 1 V	Full range			1			1			1			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V	25°C		150	400		150	400		150	400		150	400	mV
				Full range			700			700			700			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = 1 V	25°C	6			6			6			6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5 V	25°C		0.8	1		0.8	1		0.8	1		0.8	1	mA
			V_{CC} = 30 V	Full range			2.5			2.5			2.5			2.5	

† Full range (MIN or MAX) for LM193 is –55°C to 125°C, for LM293 and LM293A is 25°C to 85°C, for the LM393 and LM393A is 0°C to 70°C, and for LM2903 and LM2903Q is –40°C to 125°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

‡ The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V, but either or both inputs can go to 30 V without damage.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		LM193, LM293, LM293A LM393, LM393A LM2903, LM2903Q			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF§, See Note 4	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

§ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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electrical characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LM393Y			UNIT
				MIN	TYP†	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V	$V_{IC} = V_{ICR}$min,		2	5	mV
I_{IO}	Input offset current				5	50	nA
I_{IB}	Input bias current				−25	−250	nA
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 30 V		0 to V_{CC}−1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, $R_L \geq 15\ k\Omega$ to V_{CC}	V_O = 1.4 V to 11.4 V,	25	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V		0.1	50	nA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V		150	400	mV
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = −1 V	6			mA
I_{CC}	Supply current	R_L = ∞,	V_{CC} = 5 V		0.8	1	mA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

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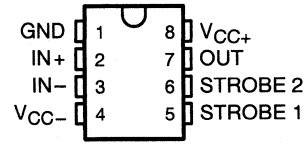
- **Fast Response Times**
- **Improved Gain and Accuracy**
- **Fanout to 10 Series 54/74 TTL Loads**
- **Strobe Capability**
- **Short-Circuit and Surge Protection**
- **Designed to Be Interchangeable With National Semiconductor LM306**

D OR P PACKAGE
(TOP VIEW)



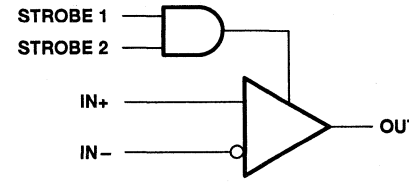
description

The LM306 is a high-speed voltage comparator with differential inputs, a low-impedance high-sink-current (100 mA) output, and two strobe inputs. This device detects low-level analog or digital signals and can drive digital logic or lamps and relays directly. Short-circuit protection and surge-current limiting is provided.

A low-level input at either strobe causes the output to remain high regardless of the differential input. When both strobe inputs are either open or at a high logic level, the output voltage is controlled by the differential input voltage. The circuit will operate with any negative supply voltage between −3 V and −12 V with little difference in performance.

The LM306 is characterized for operation from 0°C to 70°C.

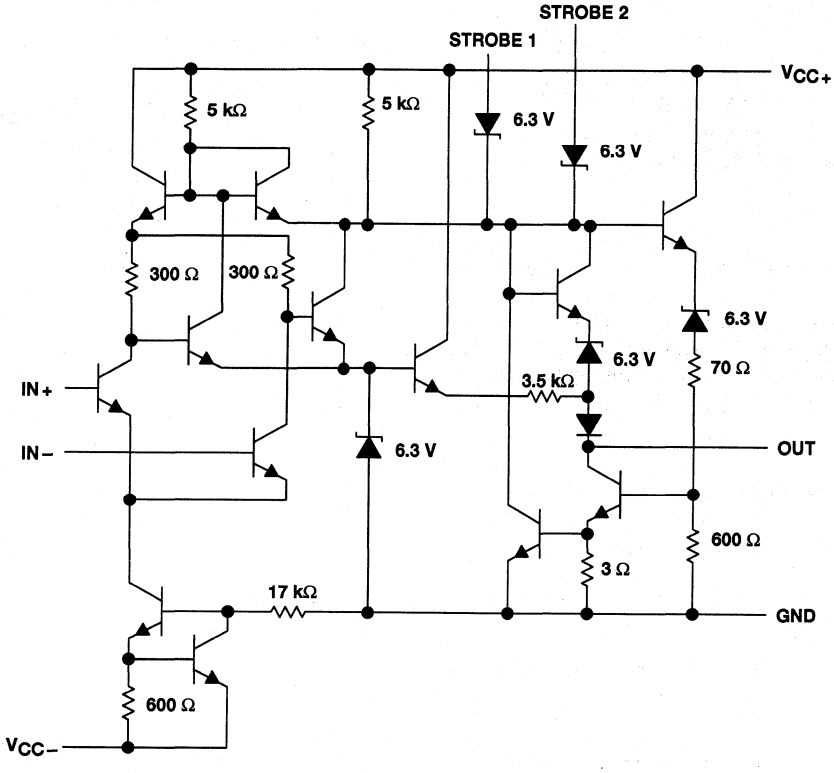
functional block diagram



AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	5 mV	LM306D	LM306P

schematic



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} (see Note 1) ..... −15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±5 V
Input voltage, V_I (either input, see Notes 1 and 3) ..... ±7 V
Strobe voltage range (see Note 1) ..... 0 V to V_{CC+}
Output voltage, V_O (see Note 1) ..... 24 V
Voltage from output to V_{CC-} ..... 30 V
Duration of output short circuit to ground (see Note 4) ..... 10 s
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages and the voltage from the output to V_{CC-}, are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 7 V, whichever is less.
4. The output may be shorted to ground or either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	600 mW	5.8 mW/°C	46°C	464 mW
P	600 mW	8.0 mW/°C	75°C	600 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = –3 V to –12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A‡	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S \le 200\ \Omega$		25°C		1.6§	5	mV
				Full range			6.5	
α_{VIO}	Average temperature coefficient of input offset voltage	R_S = 50 Ω,	See Note 5	Full range		5	20	µV/°C
I_{IO}	Input offset current	See Note 5		25°C		1.8	5	µA
				MIN		1	7.5	
				MAX		0.5	5	
α_{IIO}	Average temperature coefficient of input offset current	See Note 5		MIN to 25°C		24	100	nA/°C
				25°C to MAX		15	50	
I_{IB}	Input bias current	V_O = 0.5 V to 5 V		MIN to 25°C			40	µA
				25°C to MAX		16	25	
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)}$ = 0.4 V		Full range		–1.7	–3.2	mA
$V_{IH(S)}$	High-level strobe voltage			Full range	2.2			V
$V_{IL(S)}$	Low-level strobe voltage			Full range			0.9	V
V_{ICR}	Common-mode input voltage range	V_{CC-} = –7 V to –12 V		Full range	±5			V
V_{ID}	Differential input voltage range			Full range	±5			V
A_{VD}	Large-signal differential voltage amplification	V_O = 0.5 V to 5 V,	No load	25°C		40		V/mV
V_{OH}	High-level output voltage	I_{OH} = –400 µA	V_{ID} = 8 mV	Full range	2.5		5.5	V
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	V_{ID} = –7 mV	25°C		0.8	2	V
		I_{OL} = 50 mA	V_{ID} = –7 mV	Full range			1	
		I_{OL} = 16 mA	V_{ID} = –8 mV	Full range			0.4	
I_{OH}	High-level output voltage	V_{OH} = 8 V to 24 V	V_D = 7 mV	MIN to 25°C		0.02	2	µA
			V_{ID} = 8 mV	25°C to MAX			100	
I_{CC+}	Supply current from V_{CC+}	V_{ID} = –5 mV,	No load	Full range		6.6	10	mA
I_{CC-}	Supply current from V_{CC-}	No load		Full range		–1.9	–3.6	mA

† Unless otherwise noted, all characteristics are measured with both strobes open.
‡ Full range is 0°C to 70°C. MIN is 0°C. MAX is 70°C.
§ This typical value is at V_{CC+} = 12 V, V_{CC-} = –6 V.
NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output down to the low range (V_{OL}) or up to the high range (V_{OH}). These parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = –6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	R_L = 390 Ω to 5 V,	C_L = 15 pF,	See Note 6		28	40	ns

† All characteristics are measured with both strobes open.
NOTE 6: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	1
I_{IO}	Input offset current	vs Free-air temperature	2
V_{OH}	High-level output voltage	vs Free-air temperature	3
V_{OL}	Low-level output voltage	vs Free-air temperature	4
V_O	Output voltage	vs Differential input voltage	5
I_O	Output current	vs Differential input voltage	6
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature	7
I_{OS}	Short-circuit output current	vs Free-air temperature	8
	Output response	vs Time	9, 10
I_{CC+}	Positive supply current	vs Positive supply voltage	11
I_{CC-}	Negative supply current	vs Negative supply voltage	12
P_D	Total power dissipation	vs Free-air temperature	13

INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

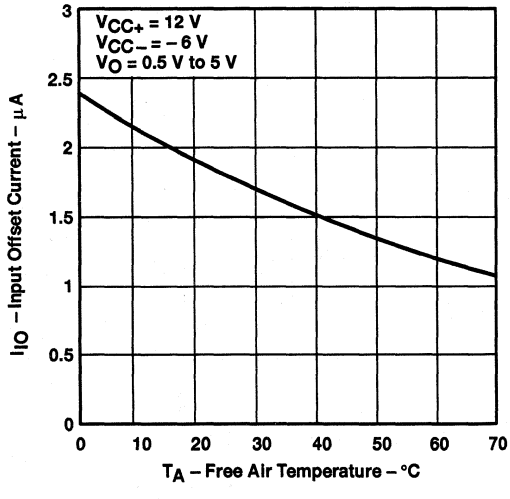


Figure 1

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

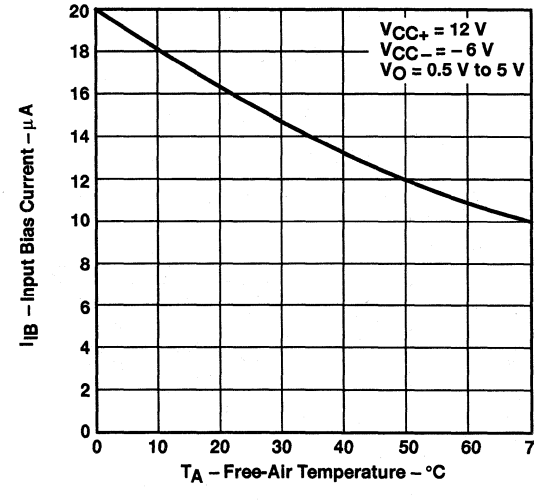


Figure 2

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

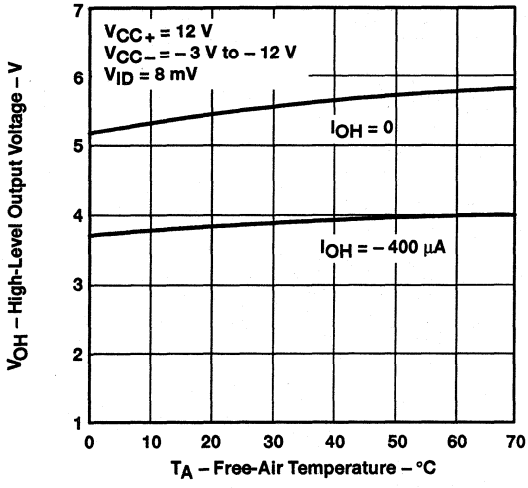


Figure 3

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

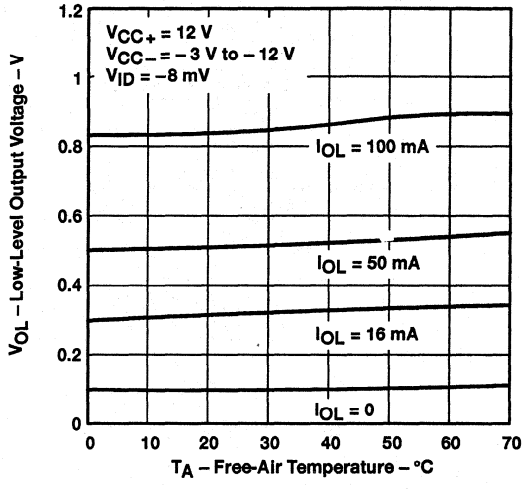


Figure 4

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

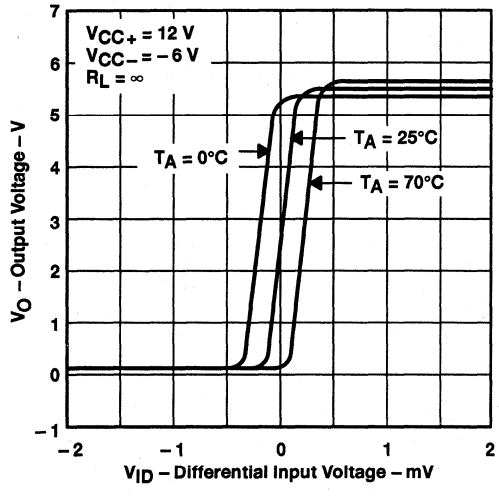


Figure 5

OUTPUT CURRENT vs DIFFERENTIAL INPUT VOLTAGE

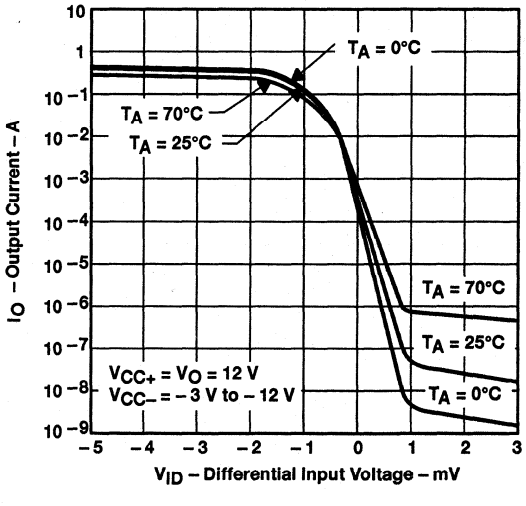


Figure 6

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

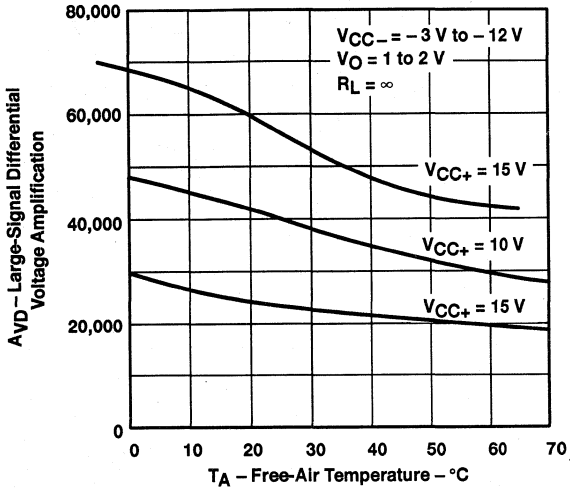
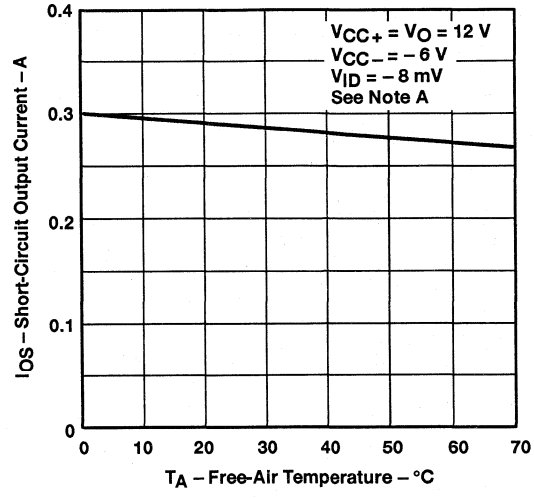


Figure 7

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE



NOTE A: This parameter was measured using a single 5-ms pulse.

Figure 8

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

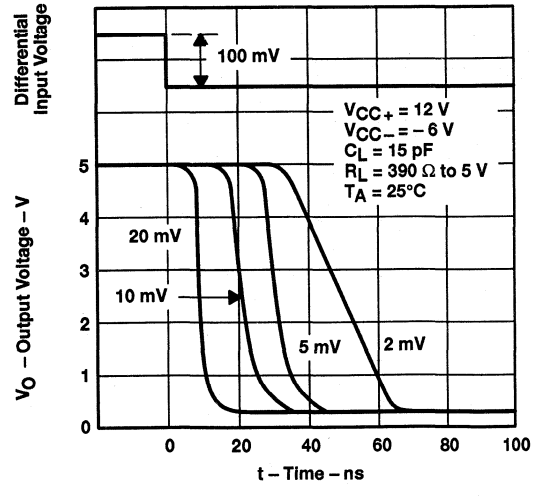


Figure 9

OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

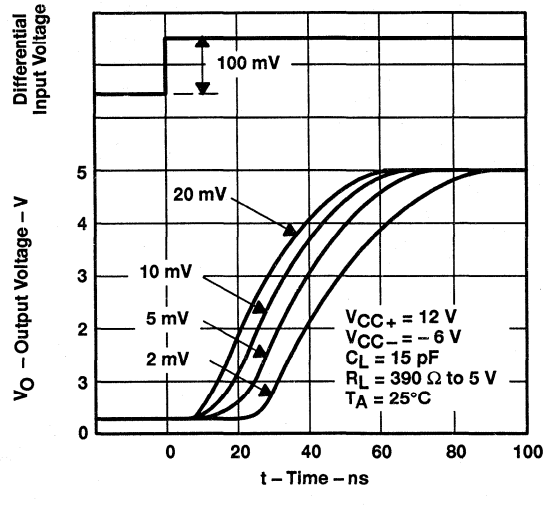


Figure 10

TYPICAL CHARACTERISTICS

POSITIVE SUPPLY CURRENT vs POSITIVE SUPPLY VOLTAGE

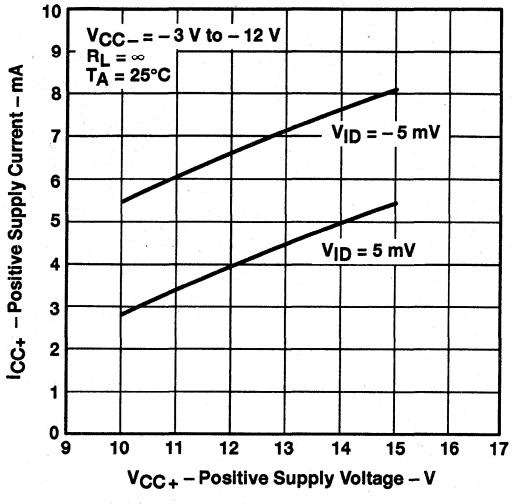


Figure 11

NEGATIVE SUPPLY CURRENT vs NEGATIVE SUPPLY VOLTAGE

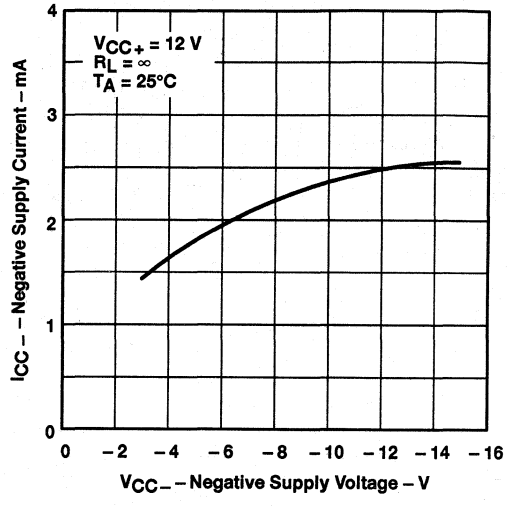


Figure 12

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

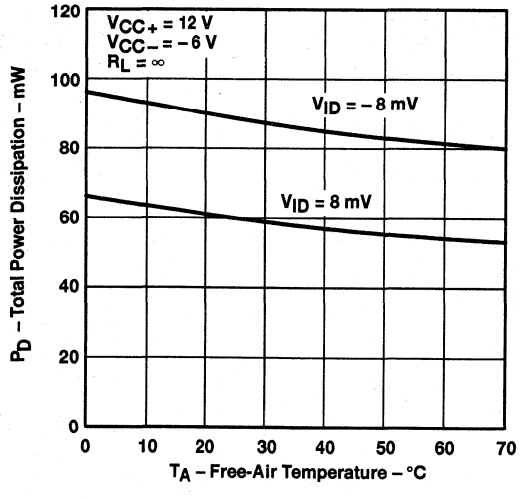
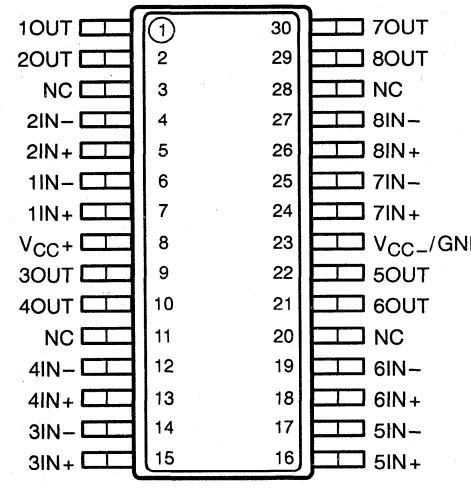


Figure 13

- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage 2 V to 36 V**
- **Low Supply-Current Drain Independent of Supply Voltage . . . 1.6 mA Typ**
- **Low Input Bias Current . . . 25 nA Typ**
- **Low Input Offset Current . . . 5 nA Typ**
- **Low Input Offset Voltage . . . 2 mV Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V**
- **Low Output Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

DB PACKAGE
(TOP VIEW)

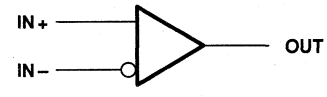


NC – No internal connection

description

The LM339x2 consists of eight independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible when the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wire-AND relationships.

symbol (each comparator)



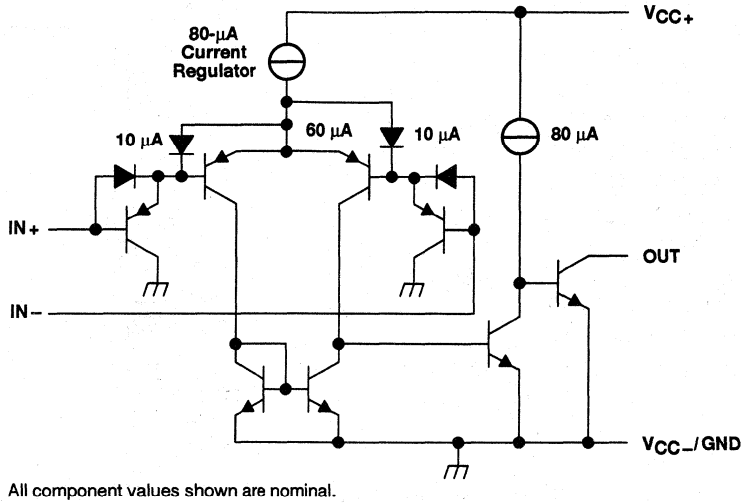
AVAILABLE OPTION

T_A	V_{IO}max AT 25°C	PACKAGE
		SMALL OUTLINE (DB)†
0°C to 70°C	5 mV	LM339x2DBLE

† The DB package is only available left-end taped and reeled.

schematic (each comparator)

ACTUAL DEVICE COMPONENT COUNT	
Transistors	120
Diodes	7
Resistors	4
JFET	2



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 36 V
Differential input voltage, V_{ID} (see Note 2) ..... ±36 V
Input voltage range, V_I (any input) ..... −0.3 V to 36 V
Output voltage, V_O ..... 36 V
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −60°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network GND.
2. Differential voltages are at IN+ with respect to IN–.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1024 mW	8.2 mW/°C	655 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP‡	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$min, V_O = 1.4 V		25°C		2	5	mV
				Full range			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−250	nA
				Full range			−400	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L = ≥ 15 kΩ to V_{CC}		25°C	50	200		V/mV
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400	mV
				Full range			700	
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1	50	nA
			V_{OH} = 30 V	Full range			1	μA
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		mA
I_{CC}	Supply current (eight comparators)	V_O = 2.5 V,	No load	25°C		1.6	4	mA
		V_{CC} = 30 V,	No load	25°C		2	5	mA

† Full range for LM339 is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.
‡ All typical values are measured at T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

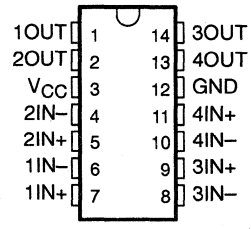
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF§, See Note 4	100-mV input step with 5-mV overdrive		1.3		ns
		TTL 1-level input step		0.3		

§ C_L includes probe and jig capacitance.
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

SLCS014 – D2402, OCTOBER 1977 – REVISED APRIL 1988

- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage 2 V to 28 V**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Low Input Bias Current . . . 25 nA Typ**
- **Low Input Offset Current . . . 3 nA Typ**
- **Low Input Offset Voltage . . . 3 mV Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ± 28 V**
- **Low Output Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

D, J, OR N PACKAGE
(TOP VIEW)



description

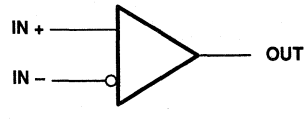
This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 V to 28 V and V_{CC} is a least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

AVAILABLE OPTIONS

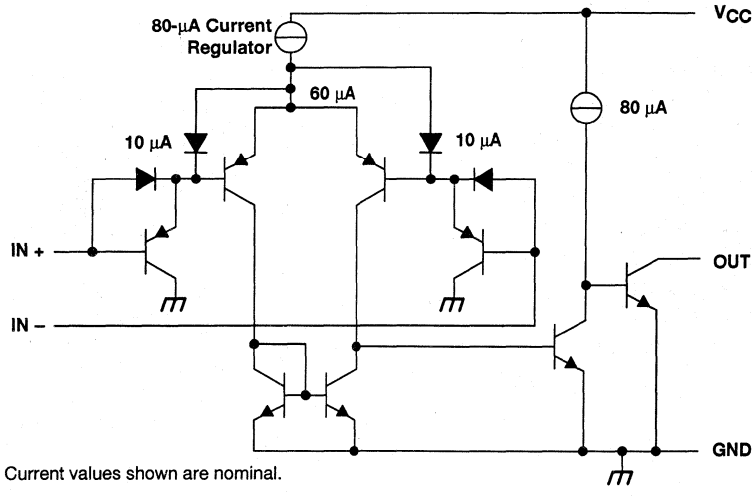
T_A	V_{IO}max at 25°C	PACKAGE		
		SMALL OUTLINE (D)†	CERAMIC DIP (J)	PLASTIC DIP (N)
–40°C to 85°C	20 mV	LM3302D	LM3302J	LM3302N

† The D packages are available taped and reeled. Add the suffix R to the device type, when ordering. (i.e., LM3302DR)

symbol (each comparator)



schematic



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 28 V
Differential input voltage, V_{ID} (see Note 2) ..... ±28 V
Input voltage range, V_I (either input), V_I ..... – 0.3 V to 28 V
Output voltage, V_O ..... 28 V
Output current, I_O ..... 20 mA
Duration of output short-circuit to ground (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature range 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature range 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. There are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN –.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 28 V, V_O = 1.4 V	$V_{IC} = V_{ICR}$ min,	25°C		3	20	mV
				– 40°C to 85°C			40	
I_{IO}	Input offset voltage	V_O = 1.4 V		25°C		3	100	nA
				– 40°C to 85°C			300	
I_{IB}	Input bias current			25°C		– 25	– 500	nA
				– 40°C to 85°C			–1000	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC} – 1.5			V
				– 40°C to 85°C	0 to V_{CC} – 2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, RL = 15 Ω to V_{CC}	V_O = 1.4 V to 11.4 V,	25°C	2	30		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V	25°C		0.1		nA
				– 40°C to 85°C			1	µA
V_{OL}	Low-level output voltage	V_{ID} = 1 V,	V_{OH} = 5 V	25°C		150	500	mV
				– 40°C to 85°C			700	
I_{OL}	Low-level output current	V_{ID} = 1 V,	V_{OL} = 1.5 V	25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	25°C		0.8		mA

‡ All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ to 5 V, See Note 4	C_L = 15 pF†, 100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

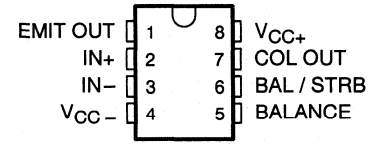
† C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

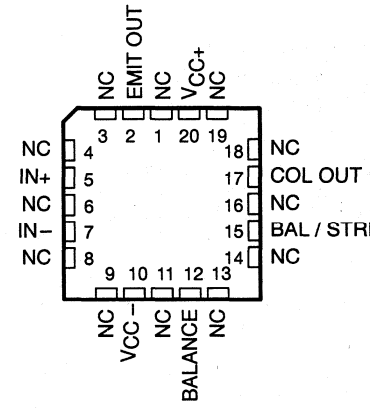
SLCS003A – D3019, JUNE 1987 – REVISED MAY 1988

- **Low Power Drain . . . 900 μW Typical With 5-V Supply**
- **Operates From ±15 V or From a Single Supply as Low as 3 V**
- **Output Drive Capability of 25 mA**
- **Emitter Output Can Swing Below Negative Supply**
- **Response Time . . . 1.2 μs Typ**
- **Low Input Currents:**
  Offset Current . . . 2 nA Typ
  Bias Current . . . 15 nA Typ
- **Wide Common-Mode Input Range:**
  – 14.5 V to 13.5 V Using ±15-V Supply
- **Same Pinout as LM111, LM211, LM311**
- **Designed to Be Interchangeable With National Semiconductor LP311**

LP111 . . . JG PACKAGE
LP211, LP311 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LP111 . . . FK PACKAGE
(TOP VIEW)



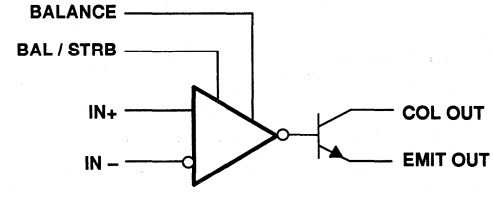
NC – No internal connection

description

The LP111, LP211, LP311 are low-power versions of the industry standard LM111, LM211, LM311. They take advantage of stable, high-value, ion-implanted resistors to perform the same function as the LM311 series, with a 30:1 reduction in power consumption but only a 6:1 slowdown in response time. They are well suited for battery-powered applications and all other applications where fast response times are not needed. They operate over a wide range of supply voltages, from ±18 V down to a single 3-V supply with less than 300-μA current drain, but are still capable of driving a 25-mA load. The LP111, LP211, and LP311 are quite easy to apply free of oscillation if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins.

The LP111 is characterized for operation over the full military temperature range of – 55°C to 125°C. The LP211 is characterized for operation from – 25°C to 85°C, and the LP311 is characterized for operation from 0°C to 70°C.

functional block diagram



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0 °C to 70 °C	7.5 mV	LP311D	—	LP311JG	LP311P
– 25 °C to 85 °C	7.5 mV	LP211D	—	LP211JG	LP211P
– 55 °C to 125 °C	7.5 mV	—	LP111FK	LP111JG	—

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 18 V
Supply voltage, V_{CC-} (see Note 1) ..... – 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ±30 V
Input voltage, V_I (either input, see Notes 1 and 3) ..... ±15 V
Voltage from emitter output to V_{CC-} ..... 30 V
Voltage from collector output to V_{CC-} ..... 40 V
Voltage from collector output to emitter output ..... 40 V
Duration of output short circuit (see Note 4) ..... 40 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: LP111 ..... – 55°C to 125°C
LP211 ..... – 25°C to 85°C
LP311 ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature range 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature range 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages are at IN+ with respect to IN –.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage of ±15 V, whichever is less.
4. The output may be shorted to ground or to either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	25°C	880 mW	715 mW	275 mW
JG (LP111)	1050 mW	8.4 mW/°C	25°C	672 mW	546 mW	210 mW
JG (LP_11)	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	—
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	—

recommended operating conditions

	MIN	MAX	UNIT
Input voltage ($\lvert V_{CC\pm} \rvert \le 15$ V)	V_{CC-} + 0.5	V_{CC+} – 1.5	V
Supply voltage, $V_{CC+} - V_{CC-}$	3.5	30	V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A		MIN	TYP†	MAX	UNIT
V_{ID}	Input offset voltage	RS < 100 kΩ, See Note 5		25°C			2	7.5	mV
				Full range				10	
V_{OL}	Low-level output voltage	V_{ID} > 10 mV, See Note 6	I_{OL} = 25 mA,	25°C			0.4	1.5	V
		V_{CC} = 4.5 V, V_{ID} < −10 mV, See Note 6	V_{CC-} = 0, I_{OL} = 1.6 mA,	Full range	LP111		0.1	0.7	
					LP211, LP311		0.1	0.4	
I_{IO}	Input offset current	See Note 5		25°C			2	25	nA
				Full range				35	
I_{IB}	Input bias current			25°C			15	100	nA
				Full range				150	
	Low-level strobe current	$V_{(strobe)}$ = 0.3 V, See Note 7	V_{ID} < −10 mV,	25°C			100	300	µA
$I_{O(off)}$	Output off-state current	V_{ID} > 10 mV,	V_{CE} = 35 V	25°C			0.2	100	nA
A_{VD}	Large signal differential voltage amplification	R_L = 5 kΩ		25°C		40	100		V/mV
I_{CC+}	Supply current from V_{CC+}	V_{ID} = − 50 V,	R_L = ∞	Full range			150	300	µA
I_{CC-}	Supply current from V_{CC-}	V_{ID} = 50 V,	R_L = ∞	Full range			− 80	− 180	µA

† All typical values are at $V_{CC\pm}$ = ±15 V, T_A = 25°C.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the output within 1 V of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. Voltages are with respect to EMIT OUT and V_{CC-} tied together.

7. The strobe should not be shorted to ground; it should be current driven at 100 µA to 300 µA.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C (unless otherwise noted)

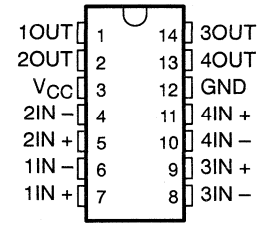
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	See Note 8		1.2		µs

NOTE 8: The response time is specified for a 100-mV input step with 5-mV overdrive.

SLCS004A – D3044, OCTOBER 1987 – REVISED MAY 1988

- **Ultralow Power Supply Current Drain . . . 60 μA Typ**
- **Low Input Biasing Current . . . 3 nA**
- **Low Input Offset Current . . . ±0.5 nA**
- **Low Input Offset Voltage . . . ±2 mV**
- **Common-Mode Input Voltage Includes Ground**
- **Output Voltage Compatible With MOS and CMOS Logic**
- **High Output Sink-Current Capability (30 mA at V_O = 2V)**
- **Power Supply Input Reverse-Voltage Protected**
- **Single-Power-Supply Operation**
- **Pin-for-Pin Compatible With LM239, LM339, LM2901**

D, J, OR N PACKAGE
(TOP VIEW)



description

The LP239, LP339, LP2901 are low-power quadruple differential comparators. Each device consists of four independent voltage comparators designed specifically to operate from a single power supply and typically to draw 60-μA drain current over a wide range of voltages. Operation from split power supplies is also possible and the ultralow power supply drain current is independent of the power supply voltage.

Applications include limit comparators, simple analog-to-digital converters, pulse generators, squarewave generators, time delay generators, voltage controlled oscillators, multivibrators, and high-voltage logic gates. The LP239, LP339, LP2901 were specifically designed to interface with the CMOS logic family. The ultralow power supply current makes these products desirable in battery-powered applications.

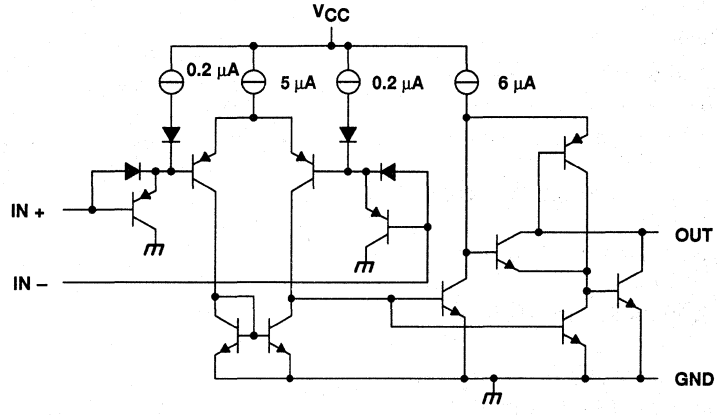
The LP239 is characterized for operation from – 25°C to 85°C. The LP339 is characterized for operation from 0°C to 70°C. The LP2901 is characterized for operation from – 40°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE		
		SMALL OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)
0 °C to 70 °C	±5 mV	LP339D	LP339N	LP339J
– 25 °C to 85 °C	±5 mV	LP239D	LP239N	LP239J
– 40 °C to 85 °C	±5 mV	LP2901D	LP2901N	LP2901J

The D package is available taped-and-reeled. Add R suffix to device type when ordering (e.g., LP339DR).

schematic diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 36 V
Differential input voltage, V_{ID} (see Note 2) ..... ±36 V
Input voltage range, V_I (either input) ..... – 0.3 V to 36 V
Input current, $V_I \leq -0.3$ V (see Note 3) ..... – 50 mA
Duration of output short-circuit to ground (see Note 4) ..... Unlimited
Continuous total dissipation (see Note 5) ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: LP239 ..... – 25°C to 85°C
LP339 ..... 0°C to 70°C
LP2901 ..... – 40°C to 85°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature range 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature range 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN –.
3. This input current only exists when the voltage at any of the inputs is driven negative. The current flows through the collector-base junction of the input clamping device. In addition to the clamping device action, there is lateral n-p-n parasitic transistor action. This action is not destructive and normal output states are re-established when the input voltage returns to a value more positive than – 0.3 V at T_A = 25°C.
4. Short circuits between outputs to V_{CC} can cause excessive heating and eventual destruction.
5. If the output transistors are allowed to saturate, the low bias dissipation and the on-off characteristics of the outputs keep the dissipation very small (usually less than 100 mW).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

			LP239		LP339		LP2901		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		5	30	5	30	5	30	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	3	0	3	0	3	V
		V_{CC} = 30 V	0	28	0	28	0	28	V
V_I	Input voltage	V_{CC} = 5 V	0	3	0	3	0	3	V
		V_{CC} = 30 V	0	28	0	28	0	28	V
T_A	Operating free-air temperature		– 25	85	0	70	– 40	85	°C

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, RS = 0,	V_O = 2 V, See Note 6	25°C		±2	±5	mV
				Full range			±9	
I_{IO}	Input offset current			25°C		±0.5	±5	nA
				Full range		±1	±15	
I_{IB}	Input bias current	See Note 7		25°C		– 2.5	– 25	nA
				Full range		– 4	– 40	
V_{ICR}	Common-mode input voltage range	Single supply		25°C	0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V,	RL = 15 kΩ			500		V/mV
	Output sink current	V_{I-} = 1 V, V_{I+} = 0	V_O = 2 V, See Note 8	25°C	20	30		mA
				Full range	15			
			V_O = 0.4 V	25°C	0.2	0.7		
	Output leakage current	V_{I+} = 1 V, V_{I-} = 0	V_O = 5 V	25°C		0.1		nA
			V_O = 30 V	Full range			1	µA
V_{ID}	Differential input voltage	$V_I \leq 0$ (or V_{CC-} on split supplies)					36	V
I_{CC}	Supply current	R_L = ∞ all comparators				60	100	µA

† Full range is –25°C to 85°C for the LP239, 0°C to 70°C for the LP339, and –40°C to 85°C for the LP2901.

NOTES: 6. V_{IO} is measured over the full common-mode input voltage range.

7. Because of the p-n-p input stage, the direction of the current is out of the device. This current is essentially constant (i.e., independent of the output state). No loading change exists on the reference or input lines as long as the common-mode input voltage range is not exceeded.
8. The output sink current is a function of the output voltage. These devices have a bimodal output section that allows them to sink (via a Darlington connection) large currents at output voltages greater than 1.5 V, and smaller currents at output voltages less than 1.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L connected to 5 V through 5.1 kΩ

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Large-signal response time	TTL logic swing, V_{ref} = 1.4 V		1.3		µs
Response time			8		

APPLICATION INFORMATION

Figure 1 shows the basic configuration for using the LP239, LP339, or LP2901 comparator. Figure 2 shows the diagram for using one of these comparators as a CMOS driver.

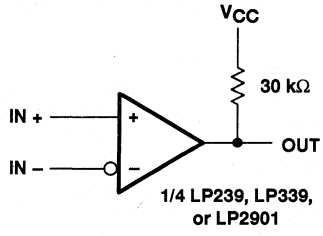


Figure 1. Basic Comparator

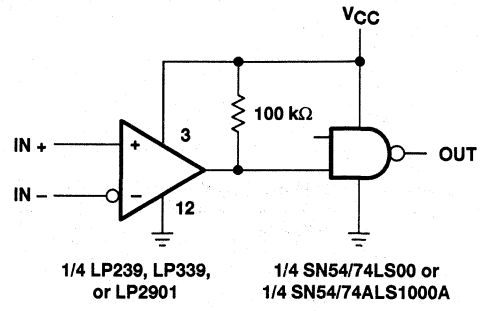


Figure 2. CMOS Driver

All pins of any unused comparators should be grounded. The bias network of the LP239, LP339, and LP2901 establishes a drain current that is independent of the magnitude of the power supply voltage over the range of 2 V to 30 V. It is usually necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative by more than – 0.3 V. The output section has two distinct modes of operation: a Darlington mode and a ground-emitter mode. This unique drive circuit permits the device to sink 30 mA at V_O = 2 V in the Darlington mode and 700 μA at V_O = 0.4 V in the ground-emitter mode. Figure 3 is a simplified schematic diagram of the output section. The output section is configured in a Darlington connection (ignoring Q3). If the output voltage is held high enough (above 1 V), Q1 is not saturated and the output current is limited only by the product of the h_{FE} of Q1, the h_{FE} of Q2, and I1 and the 60-Ω saturation resistance of Q2. The devices are capable of driving LEDs, relays, etc. in this mode while maintaining an ultralow power supply current of 60 μA typically.

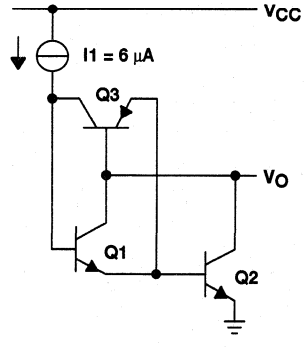


Figure 3. Output-Section Schematic Diagram

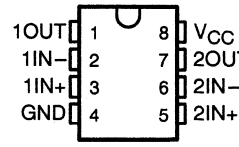
APPLICATION INFORMATION

Without transistor Q3, if the output voltage were allowed to drop below 0.8 V, transistor Q1 would saturate and the output current would drop to zero. The circuit would be unable to pull low current loads down to ground or the negative supply, if used. Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the h_{FE} of Q2 (700 μA at V_O = 0.4 V). The output of the devices exhibit a bimodal characteristic with a smooth transition between modes.

In both cases, the output is an uncommitted collector. Several outputs can be tied together to provide a dot logic function. An output pullup resistor can be connected to any available power supply voltage within the permitted power supply range, and there is no restriction on this voltage based on the magnitude of the voltage that is supplied to V_{CC} of the package.

- **Low-Voltage and Single-Supply Operation V_{CC} = 2 V to 7 V**
- **Common-Mode Voltage Range That Includes Ground**

D, P, OR PW PACKAGE
(TOP VIEW)



description

The TL393 is a dual differential comparator built using a new Texas Instruments-developed bipolar process. The TL393 is intended as an enhanced alternative to the industry-standard LM393 in circuits with supply-voltage limits of 7 V.

The new bipolar process allows the TL393 to perform with lower supply-current requirements than the LM393 (0.7 mA typical) while still providing a faster response time than the older device.

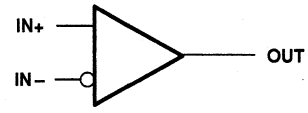
Package availability for this device includes the TSSOP (thin-shrink small-outline package). With a maximum thickness of 1.1 mm and a package area that is 25% smaller than the standard surface-mount package, the TSSOP is ideal for high-density circuits, particularly in hand-held and portable equipment.

AVAILABLE OPTIONS

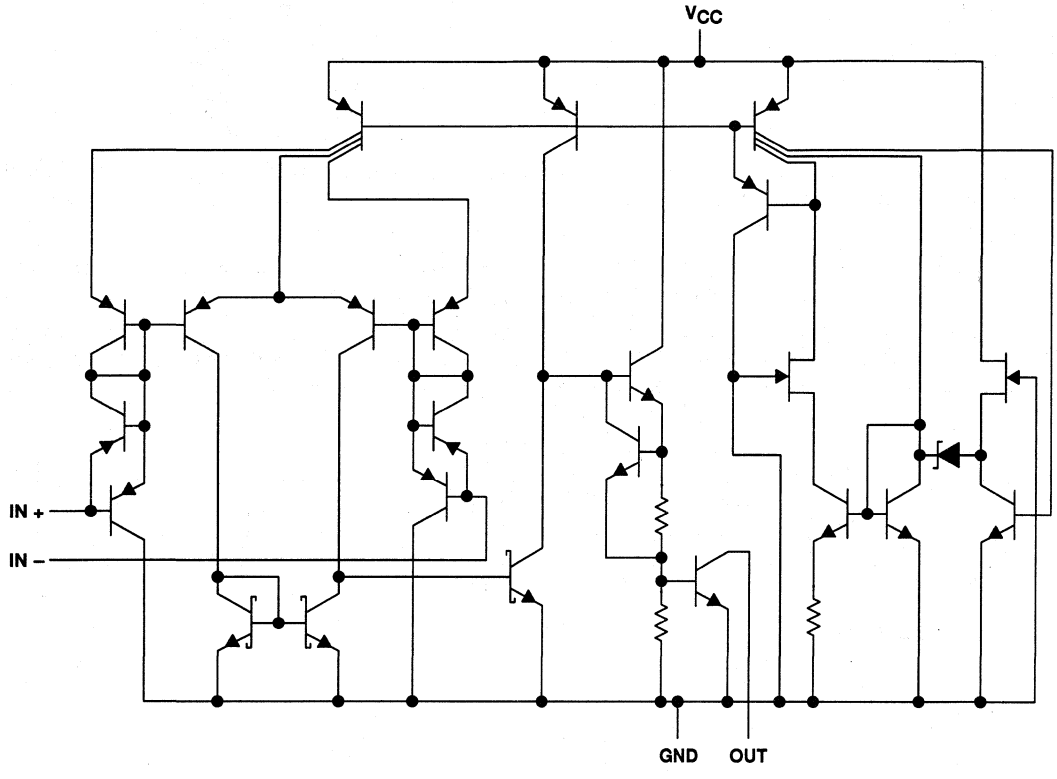
T_A	SUPPLY CURRENT (TYP)	RESPONSE TIME (TYP)	PACKAGED DEVICES			CHIP FORM (Y)
			SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)†	
–40°C to 105°C	0.7 mA	0.65 µs	TL393CD	TL393IP	TL393CPWLE	TL393Y

† The PW packages are only available left-ended taped and reeled (e.g., TL393CPWLE).

symbol (each comparator)



equivalent schematic (each comparator)

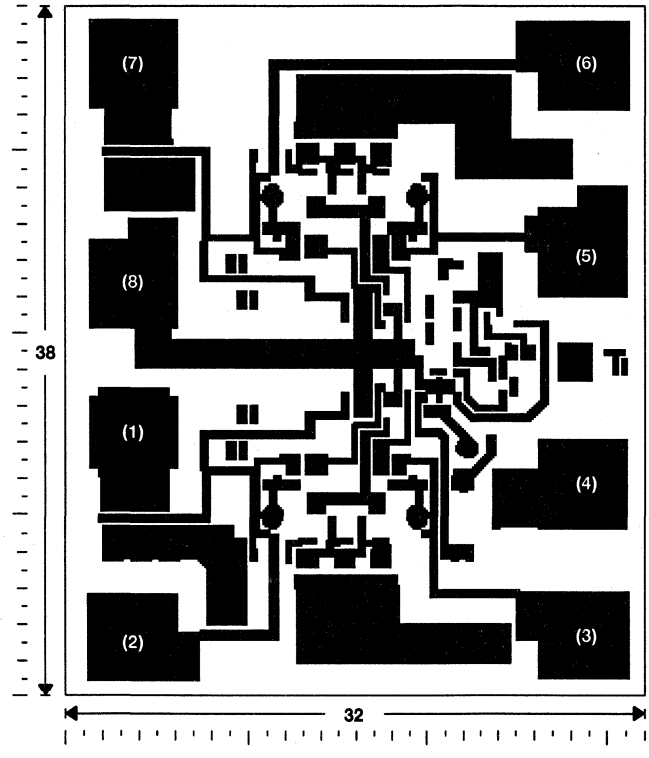


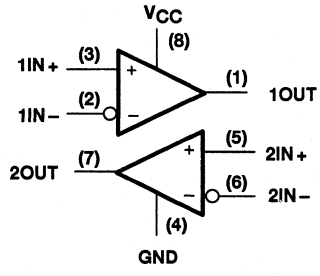
COMPONENT COUNT	
Transistors	48
Resistors	5
Diodes	7
Epi-FETs	2

TL393Y chip information

This chip, when properly assembled, displays characteristics similar to the TL393. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 13 TYPICAL

BONDING PADS: 3.54 × 3.54 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Differential input voltage, V_{ID} (see Note 2) ..... 7 V
Input voltage, V_I (any input) ..... 7 V
Output voltage, V_O ..... 7 V
Output current, I_O (each output) ..... 20 mA
Duration of short-circuit current to GND (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 105°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network GND.
2. Differential voltages are at IN+ with respect to IN−.
3. Short circuits from the outputs to V_{CC} can cause excessive heating and eventual destruction of the chip.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	2	7	V
Operating free-air temperature, T_A	−40	105	°C

electrical characteristics, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TL393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range			9	
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{CC}-1.5$	0 to $V_{CC}-1.2$		V
				Full range	0 to $V_{CC}-2$			
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 1 mA	25°C		70	300	mV
		V_{ID} = −1 V,	I_{OL} = 4 mA	Full range		200	700	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−40	−250	nA
				Full range			−400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6			mA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		140	200	µA
				Full range			300	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		0.8	1	mA
				Full range			1.2	

† Full range is −40°C to 105°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS		TL393			UNIT
			MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 kΩ		0.65		µs
	TTL-level input step,	R_L connected to 5 V through 5.1 kΩ		0.2		

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TL393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 1 mA		70	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–40	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	6			mA
I_{CCH}	High-level supply current	V_O = V_{OH}		140	200	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		0.8	1	mA

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TL393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.65		µs
	TTL-level input step, R_L connected to 5 V through 5.1 kΩ		0.2		

TYPICAL CHARACTERISTICS

LOW- TO HIGH-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

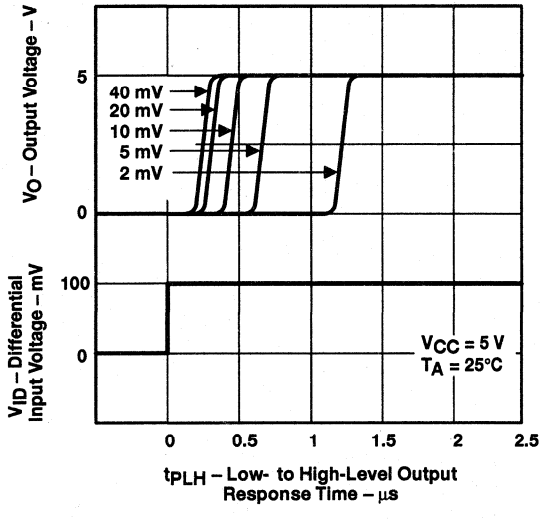


Figure 1

HIGH- TO LOW-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

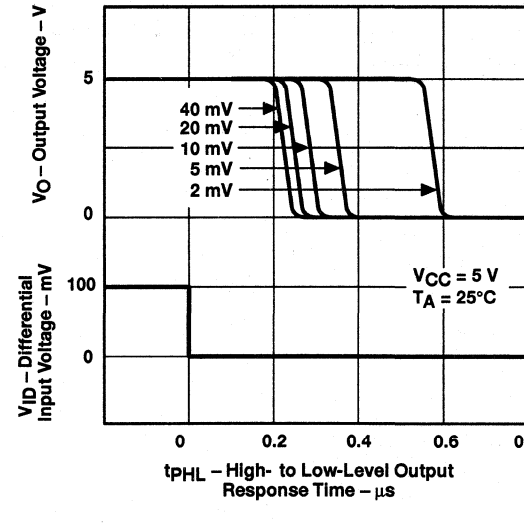
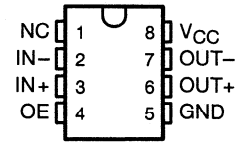


Figure 2

SLCS002B – D2741, JUNE 1983 – REVISED DECEMBER 1992

- **Operates From a Single 5-V Supply**
- **0 to 5 V Common-Mode Input Voltage Range**
- **Self-Biased Inputs**
- **Complementary 3-State Outputs**
- **Enable Capability**
- **Hysteresis . . . 5 mV Typ**
- **Response Times . . . 25 ns Typ**

D, JG, P, OR PW PACKAGE
(TOP VIEW)



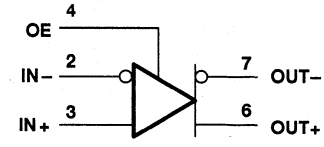
NC – No internal connection

description

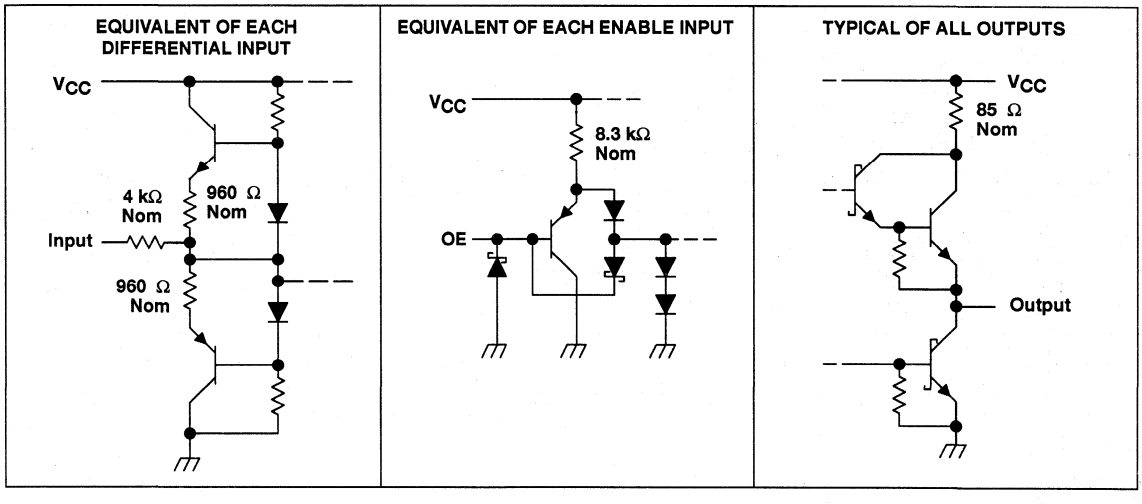
The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable, (OE), is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

The TL712 is characterized for operation from 0°C to 70°C.

symbol (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I, any differential input ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Enable input voltage ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltage values are at IN+ with respect to IN–.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}	0		5	V
High-level output current, I_{OH}			–1	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	V_{ICR} = 0 to 5 V		–100‡		100	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	I_{OH} = –1 mA	2.7	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = – 100 mV,	I_{OL} = 16 mA		0.4	0.5	V
I_{OZ}	Off-state output current	V_O = 2.4 V				–20	μA
I_I	Enable current	V_I = 5.5 V				100	μA
I_{IH}	High-level enable current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable current	V_{IL} = 0.4 V				–360	μA
r_i	Differential input resistance			4			kΩ
r_o	Output resistance					100	Ω
I_{OS}	Short-circuit output current			–15		–85	mA
I_{CC}	Supply current	V_{ID} = 0,	No load		17	20	mA

‡ The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TTL load,	See Figure 1,	See Note 3		25		ns
t_{PHL}	Propagation delay time, high-to-low-level output					25		ns

NOTE 3: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total), and is the interval between the input step function and the instant when the output crosses 2.5 V.

PARAMETER MEASUREMENT INFORMATION

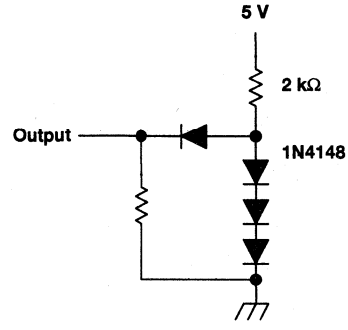


Figure 1. TTL Output Load Circuit

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVE VOLTAGES

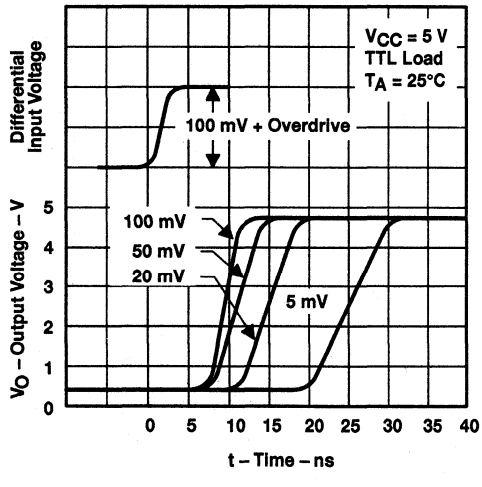


Figure 2

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVE VOLTAGES

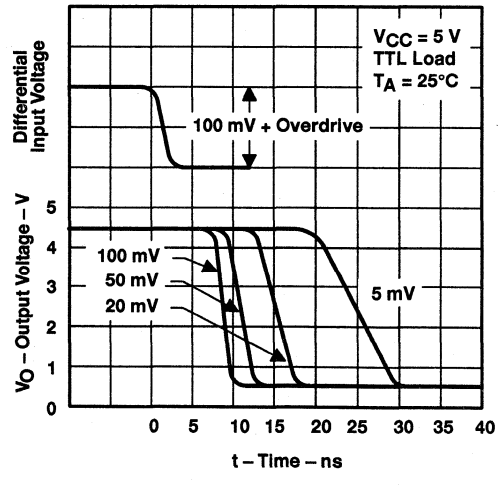


Figure 3

TYPICAL CHARACTERISTICS

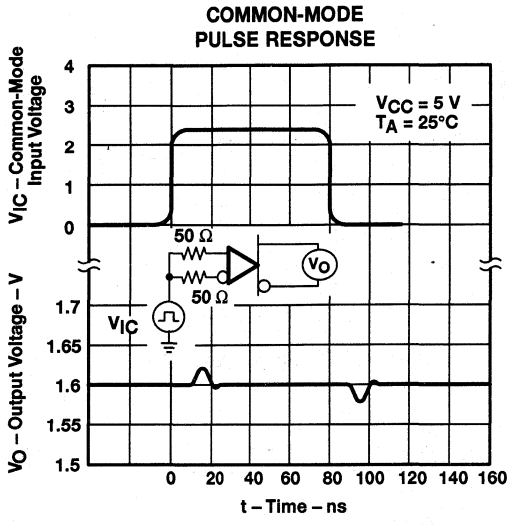
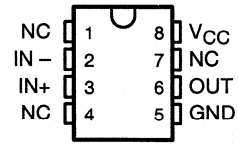


Figure 4

SLCS015 – D3131, DECEMBER 1988 – REVISED JUNE 1989

- **Operates From a 5-V Supply**
- **Self-Biasing Inputs**
- **Hysteresis . . . 10 mV Typ**
- **Response Time . . . 6 ns Typ**
- **Maximum Operating Frequency 50 MHz Typ**

D OR P PACKAGE
(TOP VIEW)



NC — No internal connection

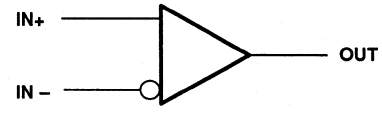
description

The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics.

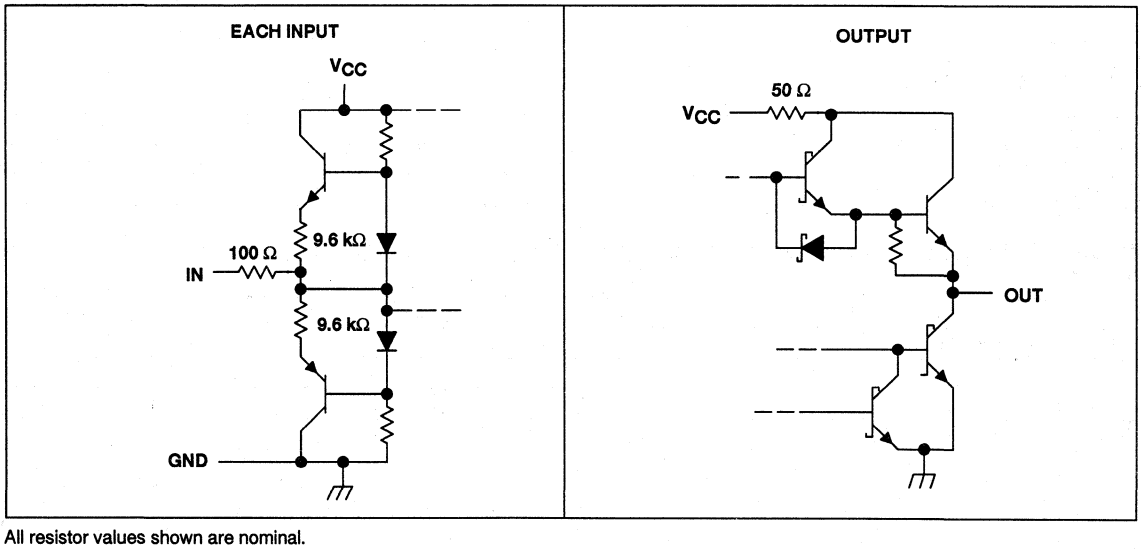
The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

The TL714C is characterized for operation from 0°C to 70°C.

symbol



schematic of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Differential input voltage, V_{ID} (see Note 2) ..... ±5 V
Input voltage range, V_I ..... V_{CC} to GND
Low-level output current, I_{OL} ..... 40 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltage, are with respect to the network ground.
2. Differential voltage values are at IN+ with respect to IN –.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 75°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW
P	500 mW	N/A	N/A	500 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.25	V
Common-mode input voltage, V_{IC}	1.4 to V_{CC} – 1.4		V
High-level output current, I_{OH}		– 1	mA
Low-level output current, I_{OL}		16	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over free-air operating temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_T	Threshold voltage ($V_{T+} - V_{T-}$)	V_{IC} = 1.4 V to 3.6 V		–75§		75	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			2	10	30	mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	I_{OH} = – 1 mA	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{ID} = – 100 mV,	I_{OL} = 16 mA		0.4	0.5	V
I_{OS}	Short-circuit output current			– 30		– 110	mA
r_i	Differential input resistance			2.9			kΩ
I_{CC}	Supply current	V_{ID} = –100 mV,	I_O = 0		7	12	mA

‡ All typical values are at T_A = 25°C.
§ The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}	Maximum operating frequency	V_{ID} = ± 250 mV, $t_r = t_f$ = 4 ns, C_L = 25 pF, Input duty cycle = 50%		50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = ± 100 mV, C_L = 25 pF, See Figures 1 and 2		6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			6	12	ns
t_r	Rise time	V_{ID} = ± 100 mV, C_L = 25 pF, See Figure 3		4	8	ns
t_f	Fall time			4	8	ns

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

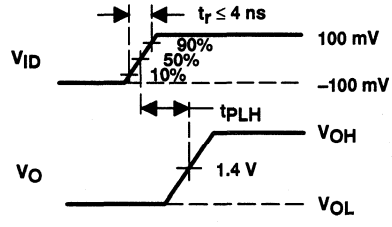


Figure 1. Propagation Delay Time, Low to High (t_{PLH})

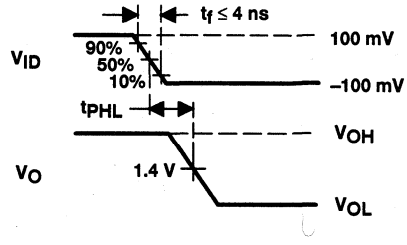


Figure 2. Propagation Delay Time, High to Low (t_{PHL})

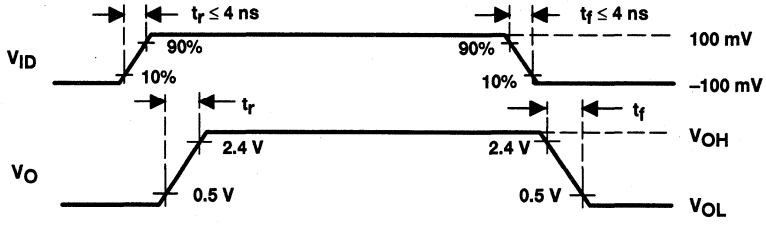
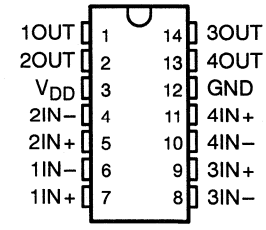


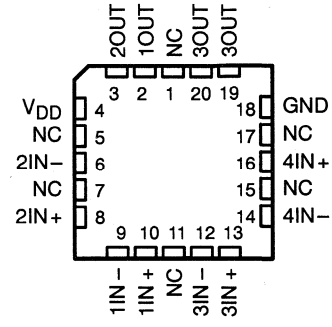
Figure 3. Rise and Fall Times (t_r, t_f)

- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . 2.5 μs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  TLC139M . . . 4 V to 16 V
  TLC339M . . . 4 V to 16 V
  TLC339C . . . 3 V to 16 V
  TLC339I . . . 3 V to 16 V
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input at Condition Typically 0.23 μV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

D, J OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



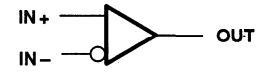
NC – No internal connection

description

The TLC139/TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM139/LM339 family but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of leads and supplies, as well as wired logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

The Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC339CD	—	—	TLC339CN
–40°C to 85°C	5 mV	TLC339ID	—	—	TLC339IN
–40°C to 125°C	5 mV	TLC339QD	—	—	TLC339QN
–55°C to 125°C	5 mV	TLC339MD	TLC139MFK	TLC139MJ	TLC339MN

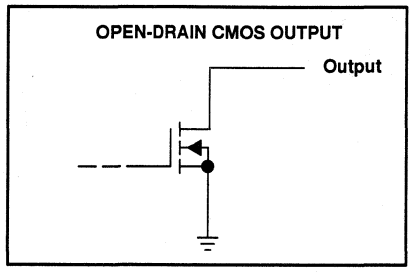
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC339CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC139M and TLC339M are characterized for operation over the full military temperature range of −55°C to 125°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC339I is characterized for operation over the industrial temperature range of −40°C to 85°C. The TLC339Q is characterized for operation over the extended industrial temperature range of −40°C to 125°C.

output schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... −0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ±18 V
Input voltage range, V_I ..... −0.3 V to V_{DD}
Output voltage range, V_O ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
Output current, I_O (each output) ..... 20 mA
Total supply current into V_{DD} ..... 40 mA
Total current out of GND ..... 60 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC139M ..... −55°C to 125°C
TLC339C ..... 0°C to 70°C
TLC339I ..... −40°C to 85°C
TLC339M ..... −55°C to 125°C
TLC339Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

	TLC139M, TLC339M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC139M, TLC339M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC}=V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC}=V_{ICR}$min	25°C		84		dB
			125°C		84		
			−55°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		30 0	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = −1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low, No load	25°C		44	80	µA
			−55°C to 125°C			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC339C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				70°C			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				70°C		84		
				0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				70°C		85		
				0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				70°C			650	
I_{OH}	High-level output current	V_{ID} = −1 V,	V_O = 5 V	25°C		0.8	40	nA
				70°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC339I MIN	TLC339I TYP	TLC339I MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				85°C			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				−40°C to 85°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				85°C		84		
				−40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				85°C		85		
				−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				85°C			700	
I_{OH}	High-level output current	V_{ID} = −1 V,	V_O = 5 V	25°C		0.8	40	nA
				85°C			1	μA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	μA
				−40°C to 85°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339Q			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC339Q			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				−40°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				−40°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				125°C		84		
				−40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		84		
				−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				125°C			800	
I_{OH}	High-level output current	V_{ID} = −1 V,	V_O = 5 V	25°C		0.8	40	nA
				125°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				−40°C to 125°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

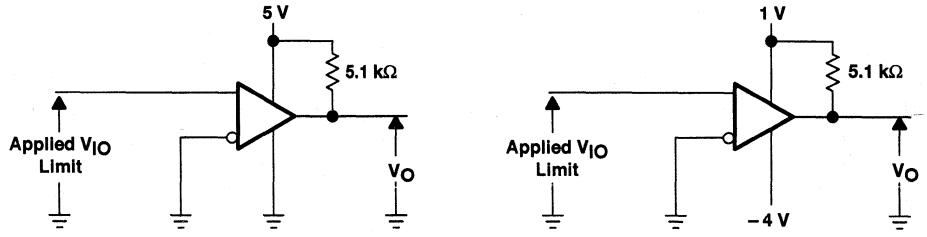
PARAMETER		TEST CONDITIONS		TLC139M, TLC339C TLC339I, TLC339M TLC339Q			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+			1.1		
t_{PHL}	Propagation delay time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+			0.10		
t_{THL}	Transition time, high-to-low level output	f = 10 kHz, C_L = 15pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC139 and TLC339 contain a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

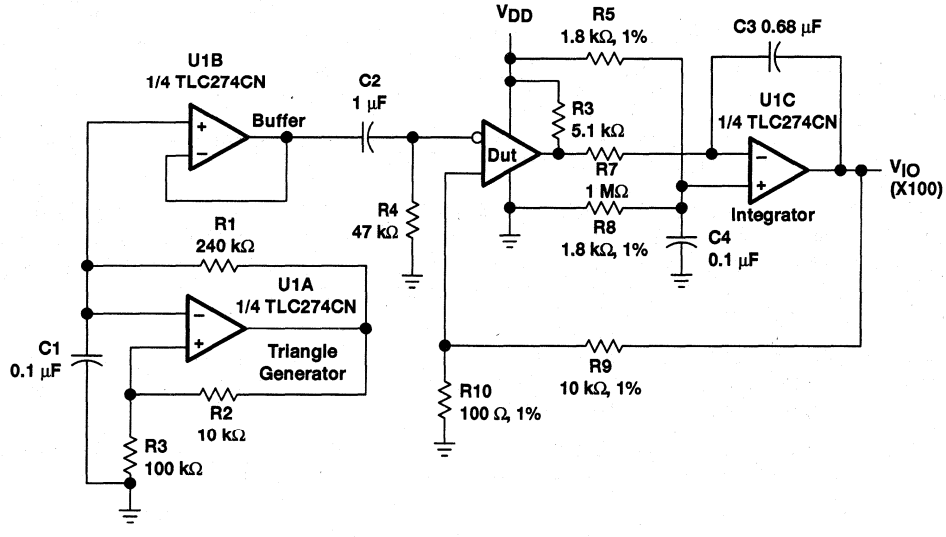
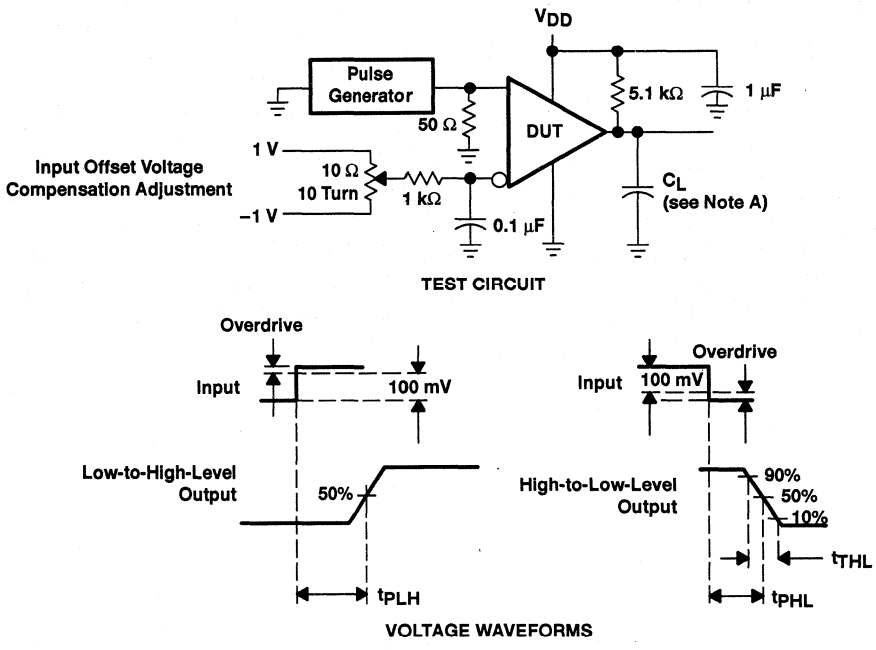


Figure 2. Circuit for Input Offset Voltage Measurement

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained, with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Free-air temperature	6
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	7
I_{OH}	High-level output current	vs High-level output voltage vs Free-air temperature	8 9
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	10 11
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	12 13
t_{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	14
t_{PHL}	Low-to-high level output propagation delay time	vs Supply voltage	15
	Overdrive voltage	vs Low-to-high-level output propagation delay time	16
t_f	Output fall time	vs Supply voltage	17
	Overdrive voltage	vs High-to-low-level output propagation delay time	18

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

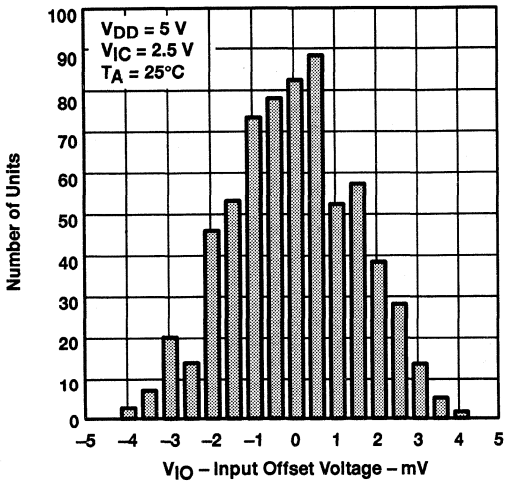


Figure 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

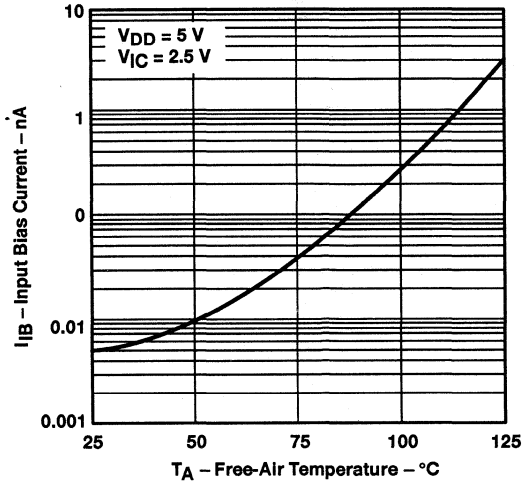


Figure 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

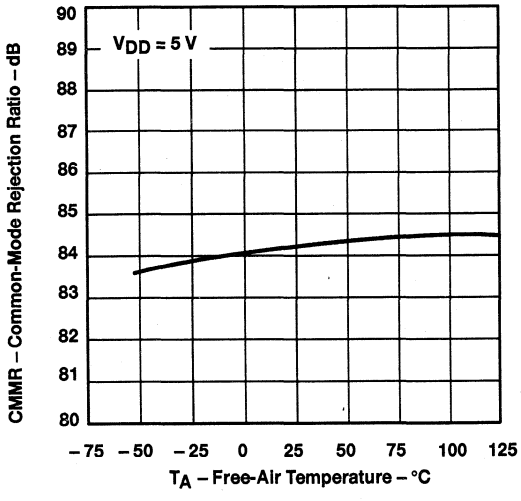


Figure 6

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

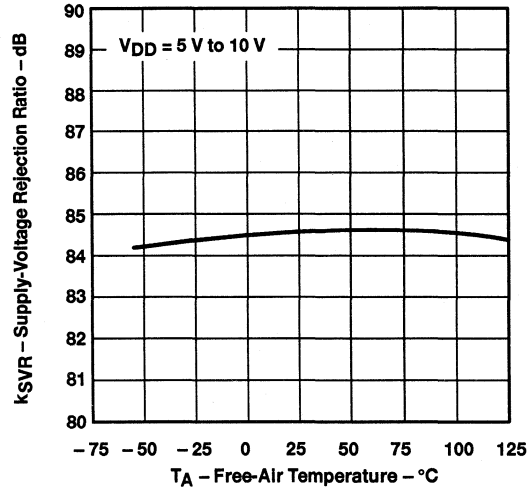


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

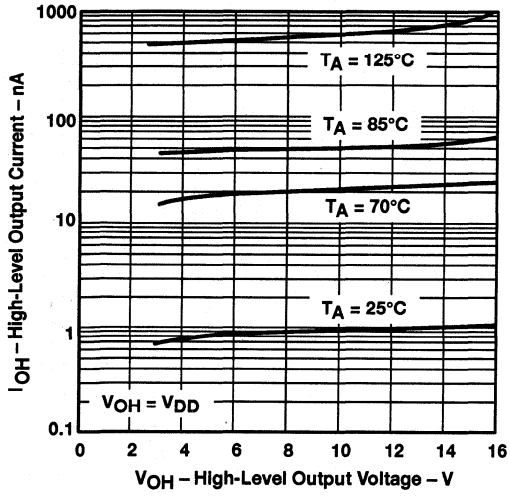


Figure 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

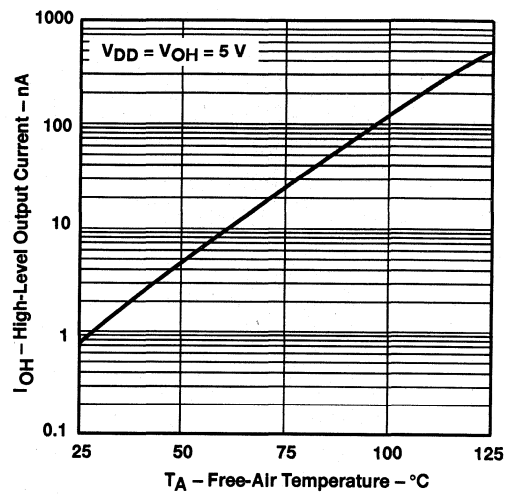


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

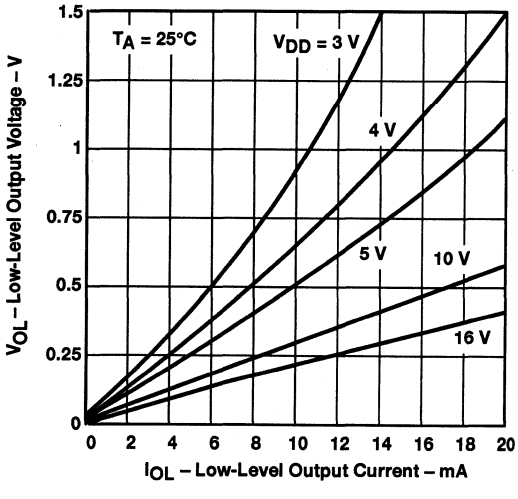


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

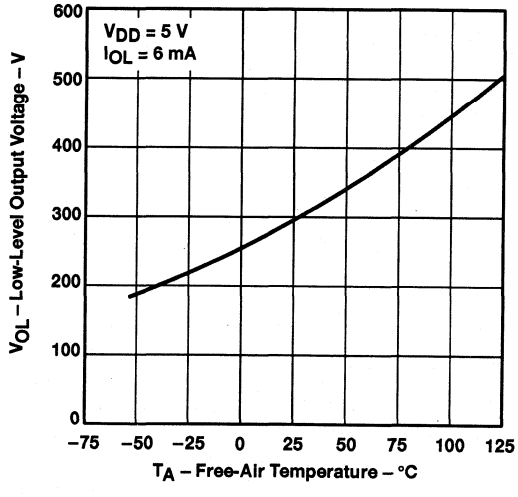


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

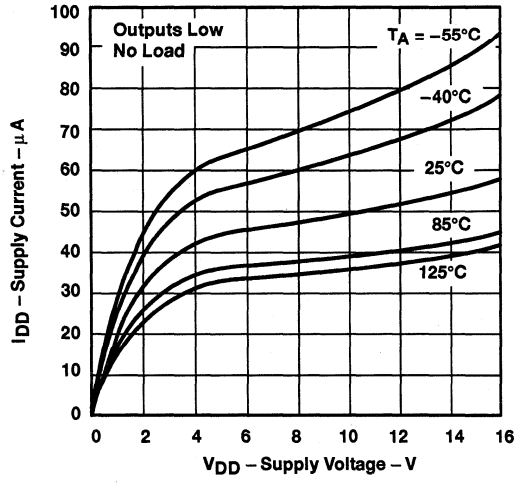


Figure 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

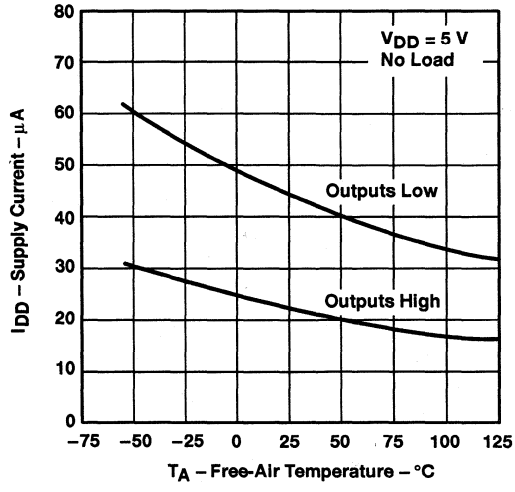


Figure 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

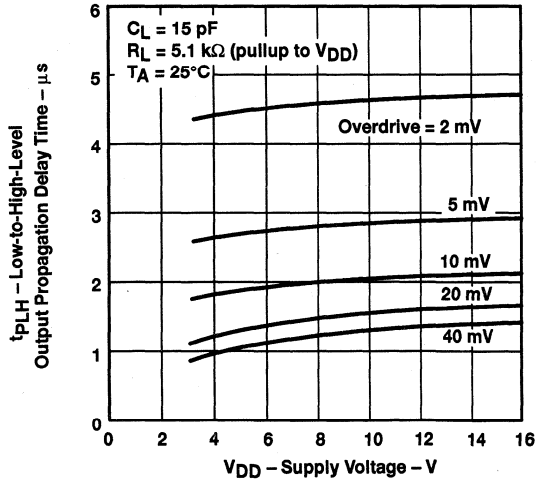


Figure 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

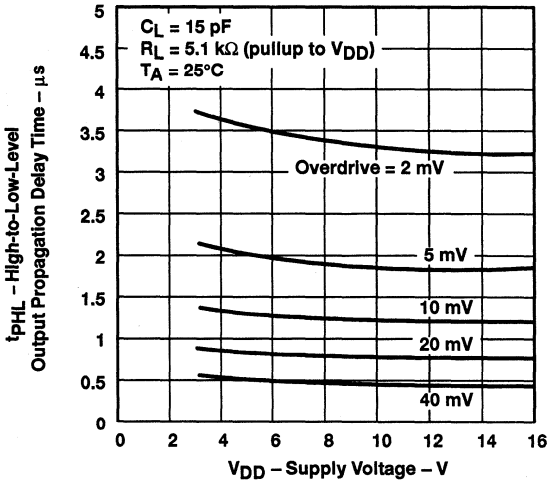


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

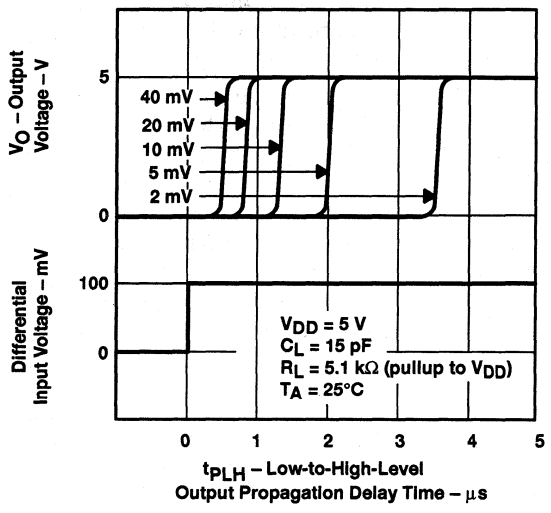


Figure 16

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

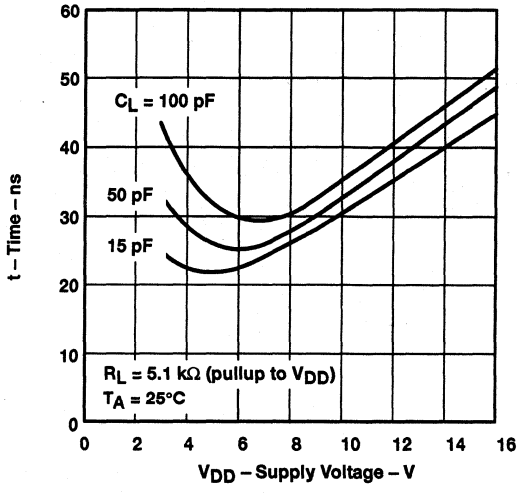


Figure 17

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

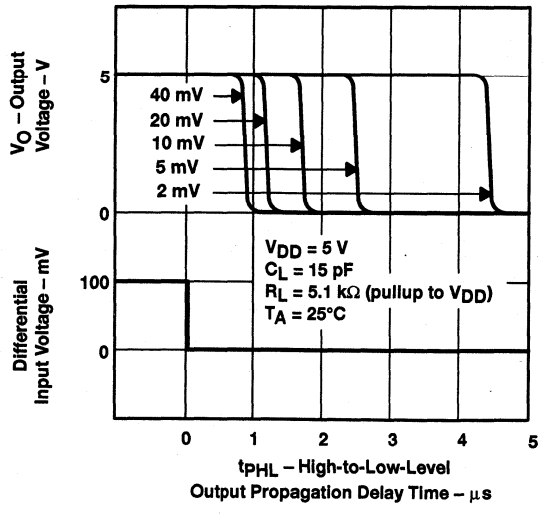


Figure 18

APPLICATION INFORMATION

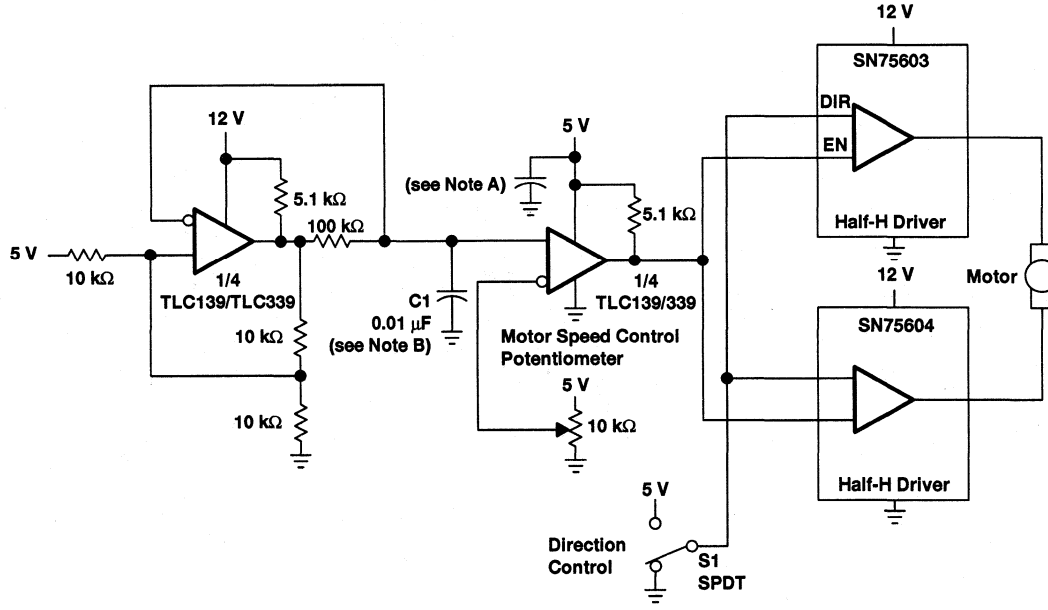
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between –0.2 V and 4 V to assure proper device operation. To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

The output and supply currents require close observation since the TLC139/TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground has an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC139 and TLC339 have internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care when handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

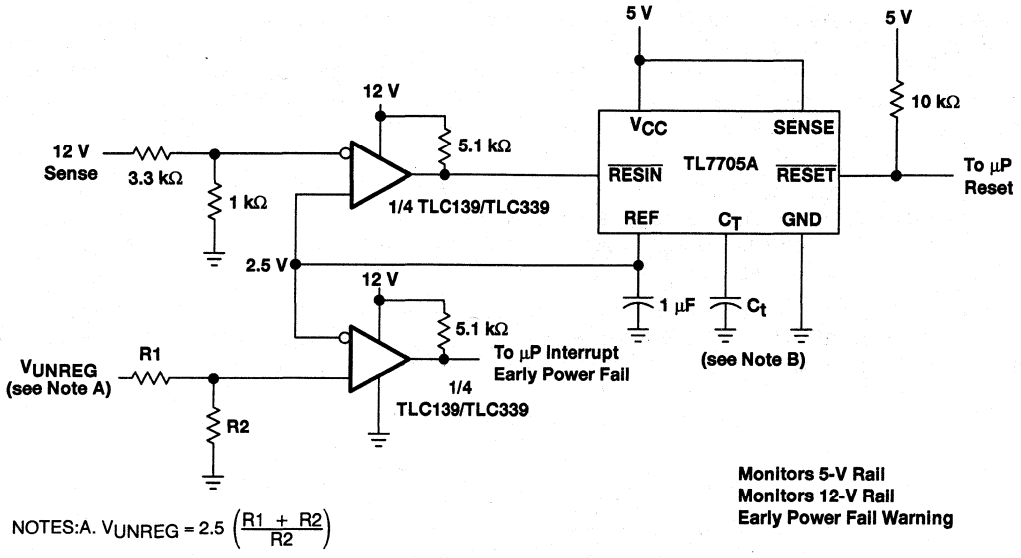
	FIGURE
Pulse-width-modulated motor speed controller	19
Enhanced supply supervisor	20
Two-phase nonoverlapping clock generator	21



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

Figure 19. Pulse-Width-Modulated Motor Speed Controller

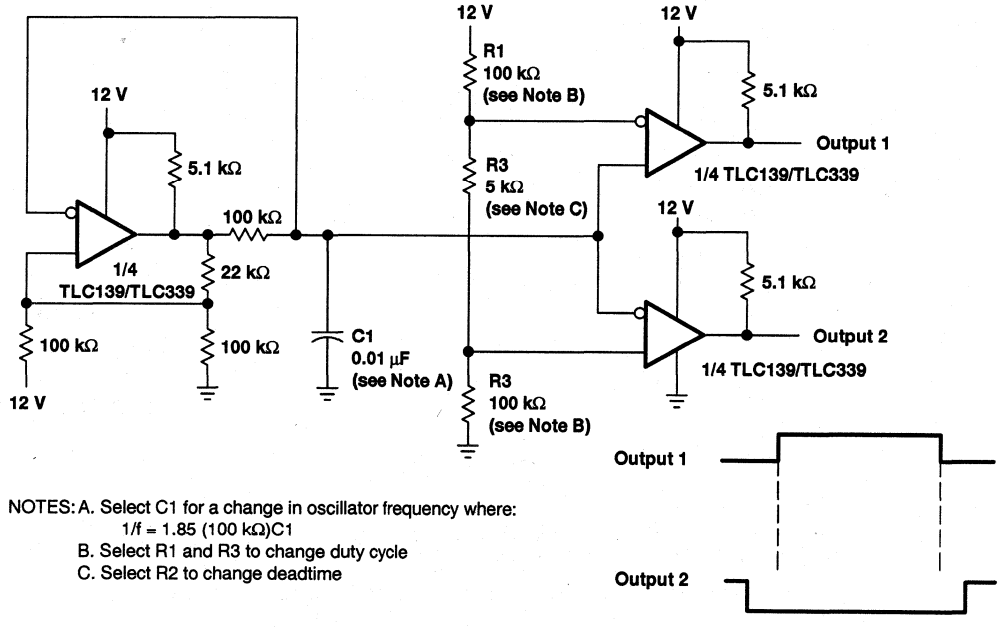
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5 \left(\frac{R1 + R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor



NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85\ (100\ k\Omega)C1$

B. Select R1 and R3 to change duty cycle

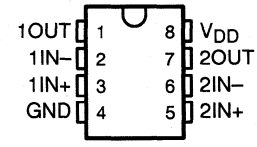
C. Select R2 to change deadtime

Figure 21. Two-Phase Nonoverlapping Clock Generator

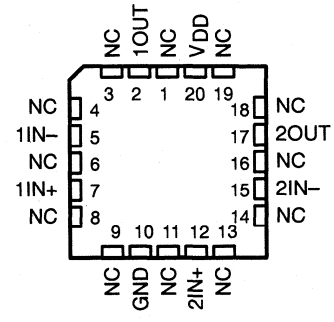
SLCS016 – D2901, SEPTEMBER 1985 – REVISED OCTOBER 1990

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages**
  1.5 V to 18 V
- **Very Low Supply Current Drain**
  150 μA Typ at 5 V
  65 μA Typ at 1.4 V
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/ Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM393**

TLC352C, TLC352I . . . D OR P PACKAGE
TLC352M . . . JG PACKAGE
(TOP VIEW)

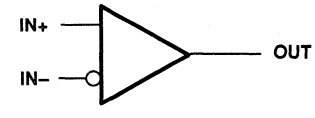


TLC352M . . . FK PACKAGE
(TOP VIEW)



NC — No Internal connection

symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interface to high-impedance sources. The output are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC352C is characterized for operation from 0°C to 70°C. The TLC352I is characterized for operation over the industrial temperature range of – 40°C to 85°C. The TLC352M is characterized for operation over the full military temperature range – 55°C to 125°C.

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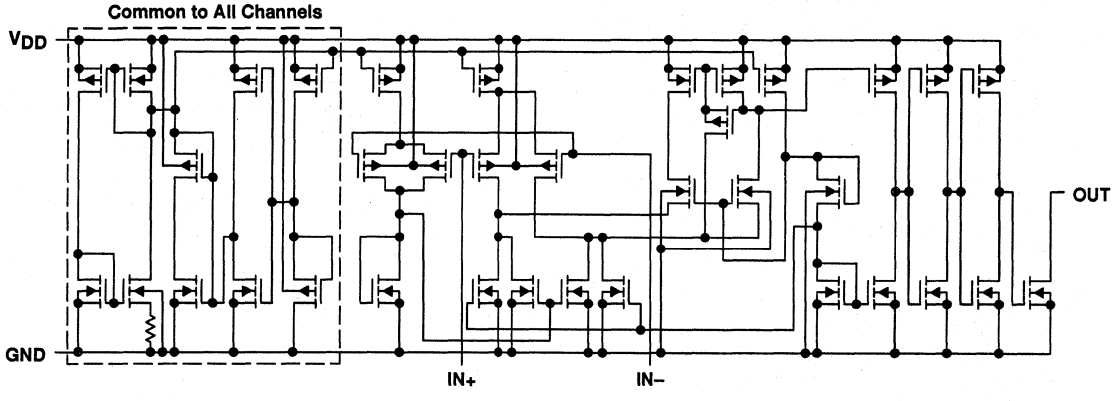
AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC352CD	—	—	TLC352CP
– 40°C to 85°C	5 mV	TLC352ID	—	—	TLC352IP
– 55°C to 125°C	5 mV	—	TLC352MFK	TLC352MJG	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC352 CDR).

equivalent schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ± 18 V
Input voltage, V_I ..... V_{DD}
Input voltage range, V_I ..... – 0.3 V to 18 V
Output voltage, V_O ..... 18 V
Input current, I_I ..... ± 5 mA
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A TLC352C ..... 0°C to 70°C
TLC352I ..... – 40°C to 85°C
TLC352M ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN –.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A

recommended operating conditions

		TLC352C			TLC352I			TLC352M			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1.4		16	1.4		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	– 40		85	– 55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC352C			TLC352I			TLC352M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min,	See Note 4	25°C		2	5		2	5		2	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			Full range	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OL}	Low-level output voltage			25°C		100	200		100	200		100	200	mV
				Full range			200			200			200	
I_{OL}	Low-level output current	V_{ID} = – 0.5 V,	V_{OL} = 0.3 V	25°C	1	1.6		1	1.6		1	1.6		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 0.5 V,	No load	25°C		65	150		65	150		65	150	µA
				Full range			200			200			200	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, – 40°C to 85°C for TLC352I, – 55°C to 125°C for TLC352M. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC352C			TLC352I			TLC352M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min,	See Note 5	25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			0 to V_{DD} – 1			0 to V_{DD} – 1			V
				Full range	0 to V_{DD} – 1.5			0 to V_{DD} – 1.5			0 to V_{DD} – 1.5			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = 1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = – 1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		0.15	0.3		0.15	0.3		0.15	0.3	mA
				Full range			0.4			0.4			0.4	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC352C, – 40°C to 85°C for TLC352I, – 55°C to 125°C for TLC352M. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC352C, TLC352I TLC352M			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

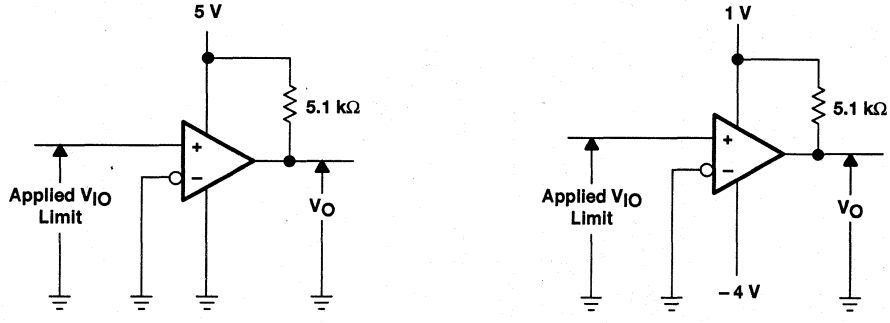
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

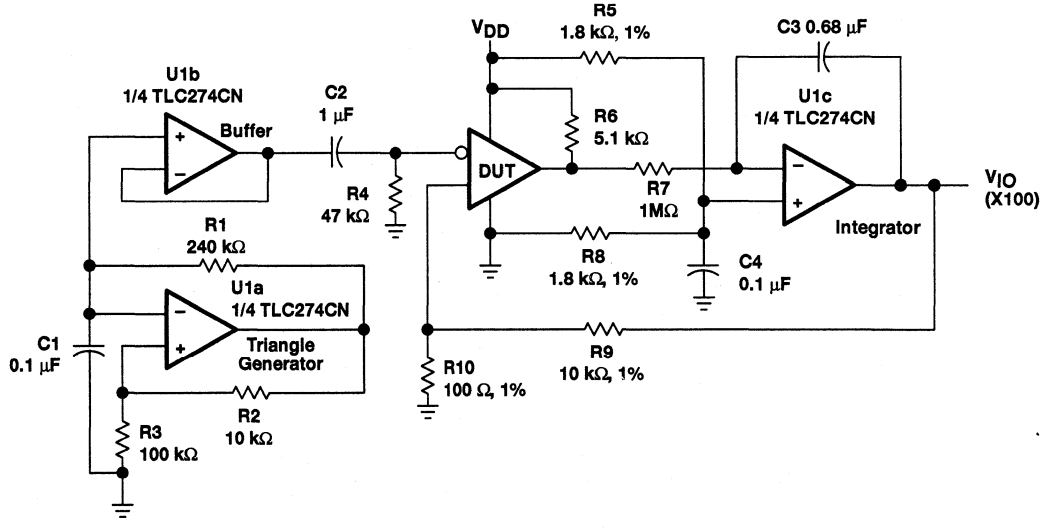
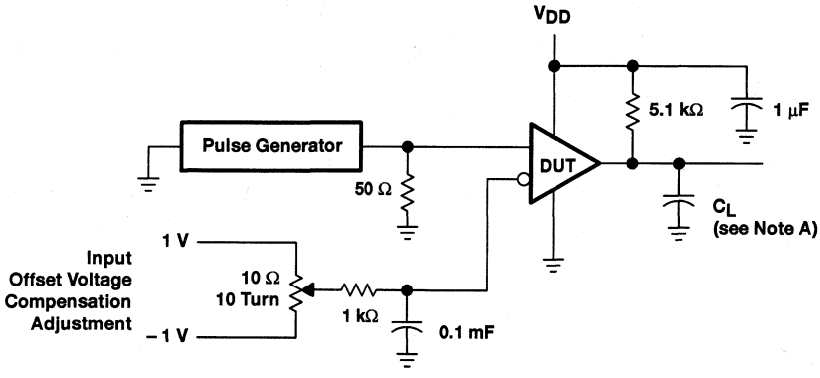


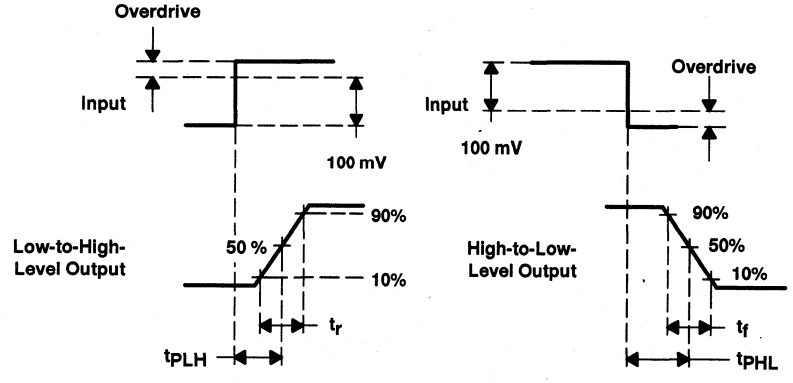
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

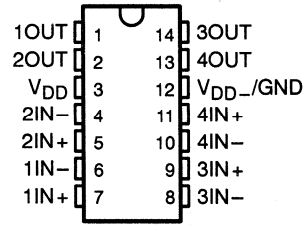
NOTE A: C_L includes probe and jig capacitance.

Figure 3. Response, Rise, and Fall Times Circuit and Voltage Waveforms

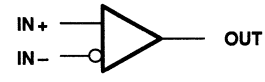
SLCS116 – D2901, SEPTEMBER 1985 – REVISED DECEMBER 1992

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages 1.4 V to 18 V**
- **Very Low Supply Current Drain 300 μA Typ at 5 V 130 μA Typ at 1.4 V**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM339**

D, N, OR PW PACKAGE
(TOP VIEW)



symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of four independent differential voltage comparators; each is designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interface to high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC354 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC354 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-833C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC354C is characterized for operation from 0°C to 70°C. The TLC354I is characterized for operation over the industrial temperature range of −40° to 85°C. The TLC354M is characterized for operation over the full military temperature range −55°C to 125°C.

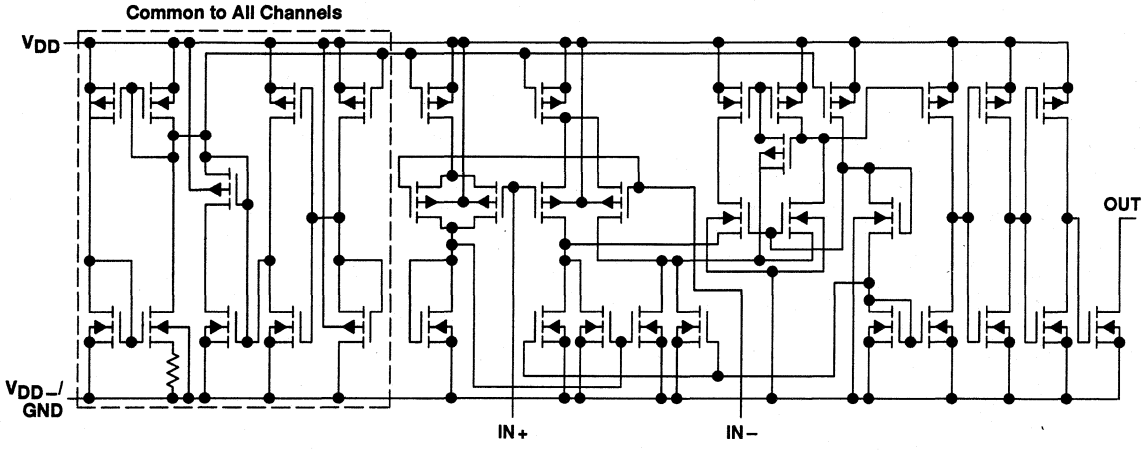
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	5 mV	TLC354CD	TLC354CN	TLC354CPW	TLC354Y
−40°C to 85°C	5 mV	TLC354ID	TLC354IN	—	—
−55°C to 125°C	5 mV	TLC354MD	TLC354MN	—	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC354CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic (each comparator)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ±18 V
Input voltage, V_I ..... V_{DD}
Input voltage range, V_I ..... –0.3 V to 18 V
Output voltage, V_O ..... 18 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... Unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC354C ..... 0°C to 70°C
TLC354I ..... –40°C to 85°C
TLC354M ..... –55°C to 125°C
Storage temperature range ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

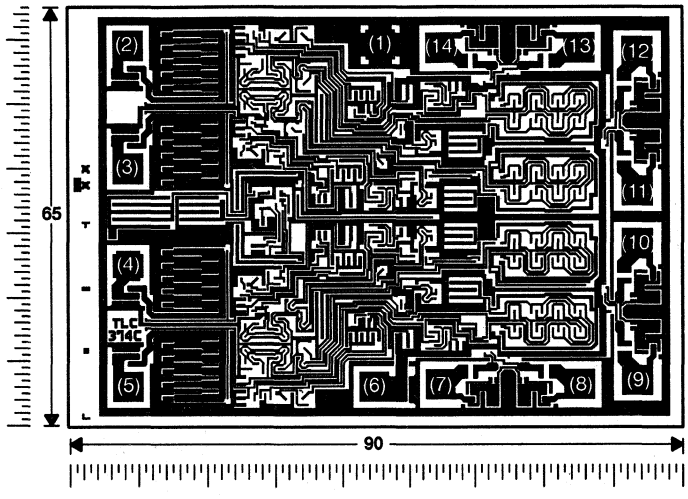
DISSIPATION RATING TABLE

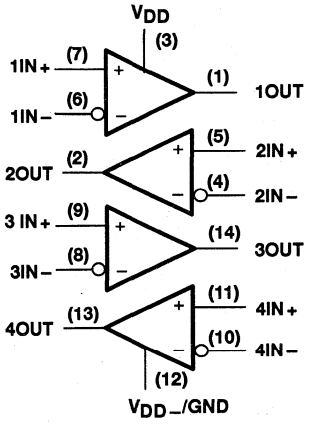
PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mV	7.6 mW/°C	84°C	500 mW	494 mW	190 mW
N	500 mV	9.2 mW/°C	96°C	500 mW	500 mW	230 mW
PW	700 mV	5.6 mW/°C	25°C	448 mW	N/A	N/A

TLC364Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC354C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

recommended operating conditions

		TLC354C		TLC354		TLC354M		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		1.4	16	1.4	16	1.4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0	0.2	0	0.2	0	0.2	V
	V_{DD} = 5 V	0	3.5	0	3.5	0	3.5	
	V_{DD} = 10 V	0	8.5	0	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V

PARAMETER		TEST CONDITIONS		T_A†	TLC354C			TLC354I			TLC354M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 4		25°C		2	5		2	5		2	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −0.5 V,	I_{OL} = 0.6 mA	25°C		100	200		100	200		100	200	mV
				Full range			200			200			200	
I_{OL}	Low-level output current	V_{ID} = −0.5 V,	V_{OL} = 300 mV	25°C	1	1.6		1	1.6		1	1.6		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 0.5 V,	No load	25°C		130	300		130	300		130	300	µA
				Full range			400			400			400	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC354C, −40°C to 85°C for TLC354I, and −55°C to 125°C for the TLC354M. MAX is 70°C for TLC354C, 85°C TLC354I, and 125°C for the TLC354M. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC354C			TLC354I			TLC354M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 5		25°C		2	5		2	5		2	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 mV	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		0.3	0.6		0.3	0.6		0.3	0.6	mA
				Full range			0.8			0.8			0.8	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70 °C for TLC354C, −40°C to 85°C for TLC354I, and −55°C to 125°C for the TLC354M. MAX is 70°C for TLC354C, 85°C TLC354I, and 125°C for the TLC354M. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC354C, TLC354I TLC354M			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC354Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min,	See Note 4		2	5	mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				5		pA
V_{ICR}	Common-mode input voltage range			0 to 0.2			V
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V		0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −0.5 V,	I_{OL} = 0.6 mA		100	200	mV
I_{OL}	Low-level output current	V_{ID} = −0.5 V,	V_{OL} = 300 mV	1	1.6		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 0.5 V,	No load		130	300	µA

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC354Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min,	See Note 5		2	5	mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				5		pA
V_{ICR}	Common-mode input voltage range			0 to V_{DD}−1			V
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V		0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 mV	6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load		0.3	0.6	mA

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC354Y			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages ca be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

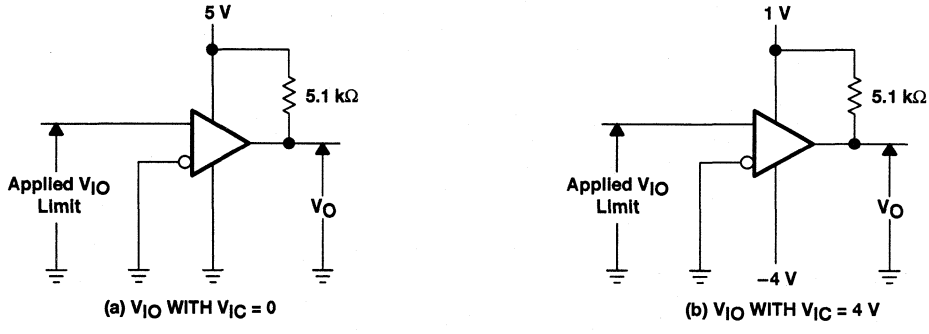


Figure 1. Method for Verifying That Input Offset Voltage is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practicle circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

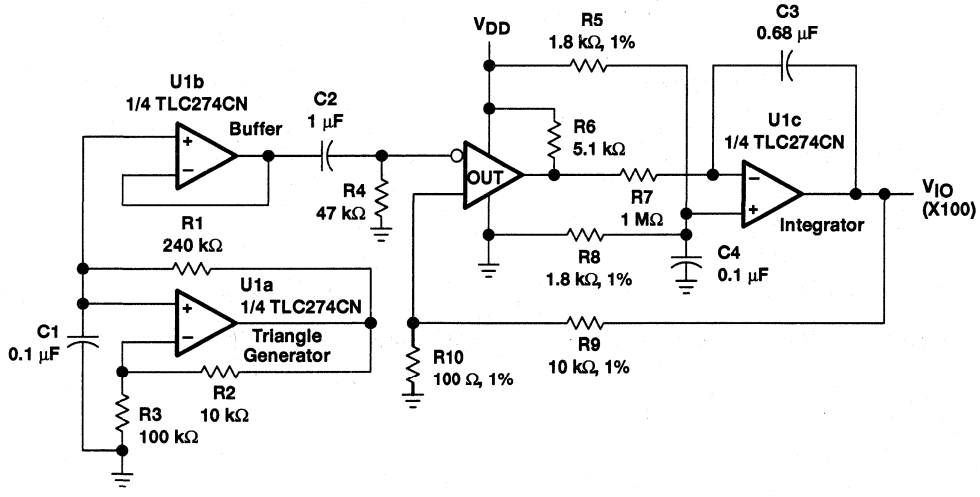
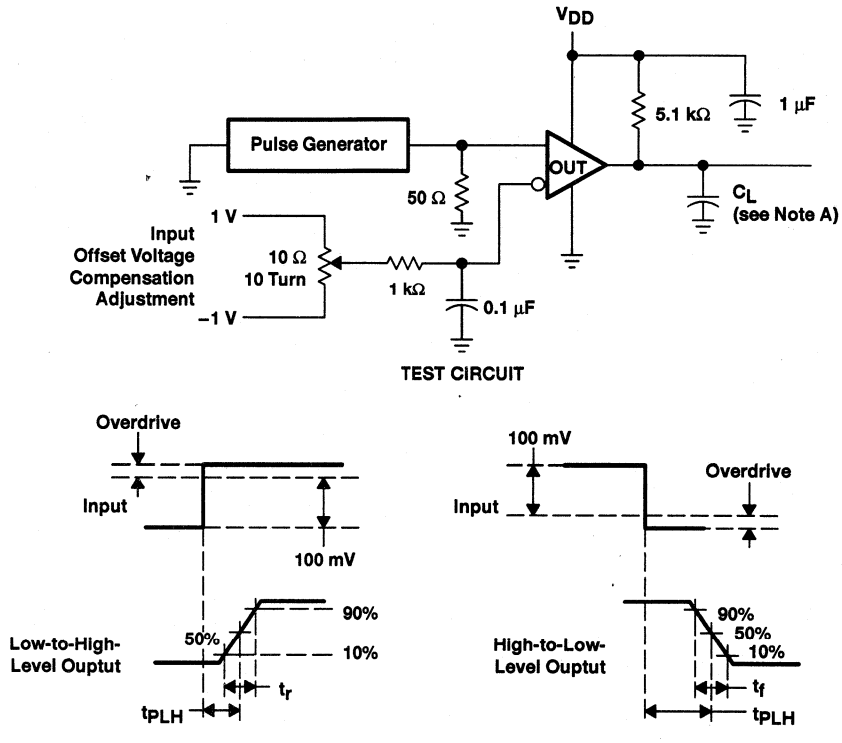


Figure 2. Test Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105-mV or 5-mV overdrive, causes the output to change.



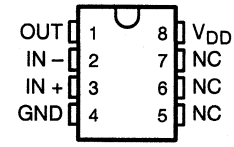
NOTE A: C_L includes probe and jig capacitance.

Figure 3. Response, Rise, and Fall Times Test Circuit and Voltage Waveforms

SLCS017 – JULY 1991 – REVISED FEBRUARY 1992

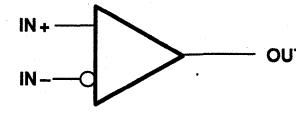
- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages**
  3 V to 16 V
- **Very Low Supply Current Drain**
  75 μA Typ at 5 V
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **Extremely Low Input Bias Current**
  5 pA Typ
- **Ultrastable Low Input Offset Voltage**
- **Common-Mode Input Voltage Range Includes Ground**
- **Output Compatible With TTL, MOS, and CMOS**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



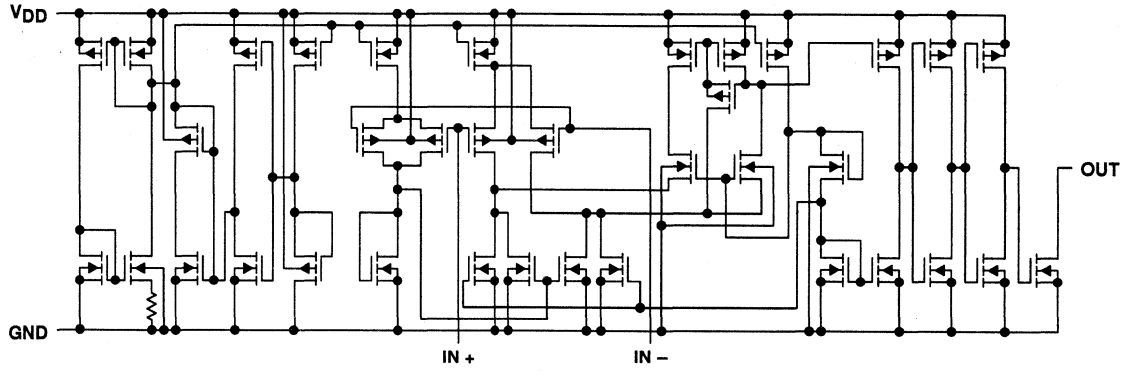
description

The TLC371 is a voltage comparator fabricated using LinCMOS™ technology and designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. The TLC371 features extremely high input impedance, allowing direct interfacing with high-impedance sources. The output is in n-channel open-drain configuration.

The TLC371 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC371C is characterized for operation from 0°C to 70°C. The TLC371I is characterized for operation from – 40°C to 85°C. The TLC371M is characterized for operation over the full military temperature range of – 55°C to 125°C.

equivalent schematic (each comparator)

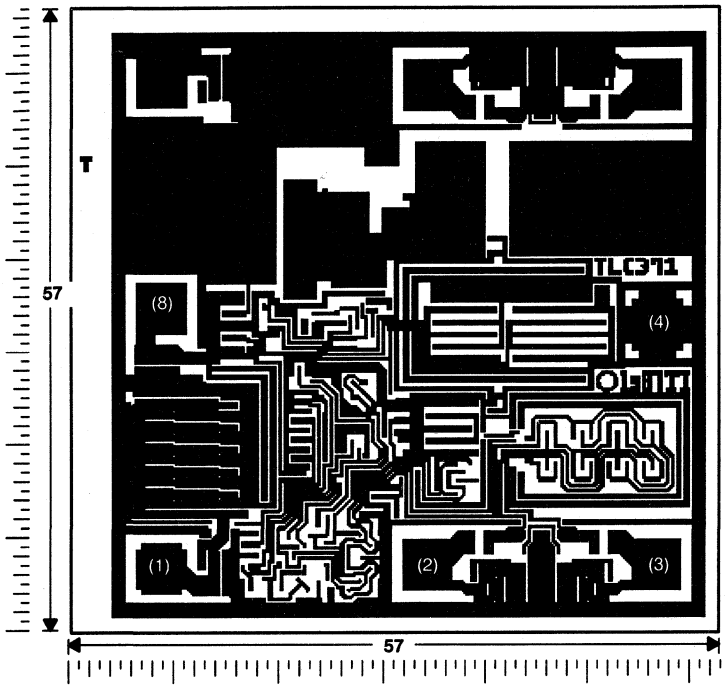


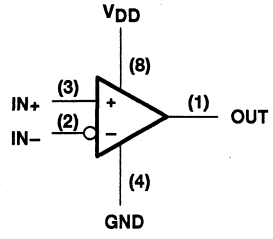
LinCMOS is a trademark of Texas Instruments Incorporated.

TLC371Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC371. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

NO BACKSIDE METALIZATION

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGED DEVICES		CHIP FORM (Y)†
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	5 mV	TLC371CD	TLC371CP	TLC371Y
– 40°C to 85°C	5 mV	TLC371ID	TLC371IP	—
– 55°C to 125°C	5 mV	TLC371MD	TLC371MP	—

† Chips are tested at T_A = 25°C. See TLC371Y for electrical characteristics.
The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TLC371CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ±18 V
Input voltage range, V_I ..... – 0.3 to 18 V
Output voltage, V_O ..... 18 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC371C ..... 0 to 70°C
TLC371I ..... – 40°C to 85°C
TLC371M ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	145 mW
P	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

recommended operating conditions

		TLC371C		TLC371I		TLC371M		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	3	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0	3.5	0	3.5	0	3.5	V
	V_{DD} = 10 V	0	8.5	0	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC371C			TLC371I			TLC371M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{IH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			3	µA
V_{OL}	Low-level output voltage	$V_{ID} = -1$ V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	$V_{ID} = -1$ V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V,	No load	25°C		75	150		75	150		75	150	µA
				Full range			200			200			200	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC371C, –40°C to 85°C for TLC371I, and –55°C to 125°C for TLC371M. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 5	100-mV input step with 5-mV overdrive		650		µs
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

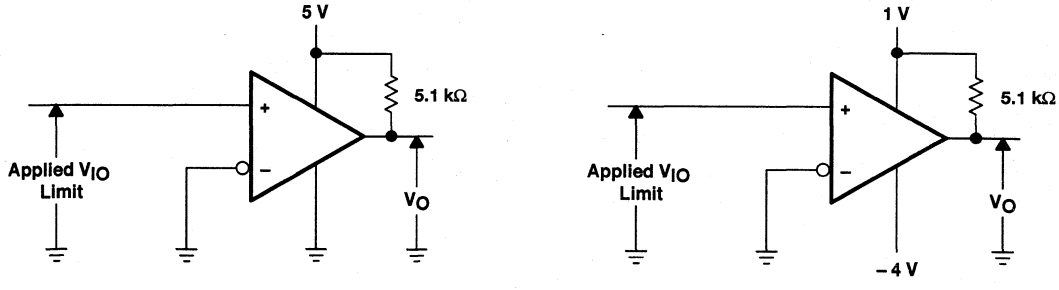
PARAMETER		TEST CONDITIONS	TLC371Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min		1	5	mV
I_{IO}	Input offset current			1	100	pA
I_{IB}	Input bias current			5	100	pA
V_{ICR}	Common-mode input voltage range		0 to V_{DD} – 1			V
I_{OH}	High-level output current			0.1		nA
V_{OL}	Low-level output voltage			150	400	mV
I_{OL}	Low-level output current		6	16		mA
I_{DD}	Supply current			75	150	μA

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC371 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0

(b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity, to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo-loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

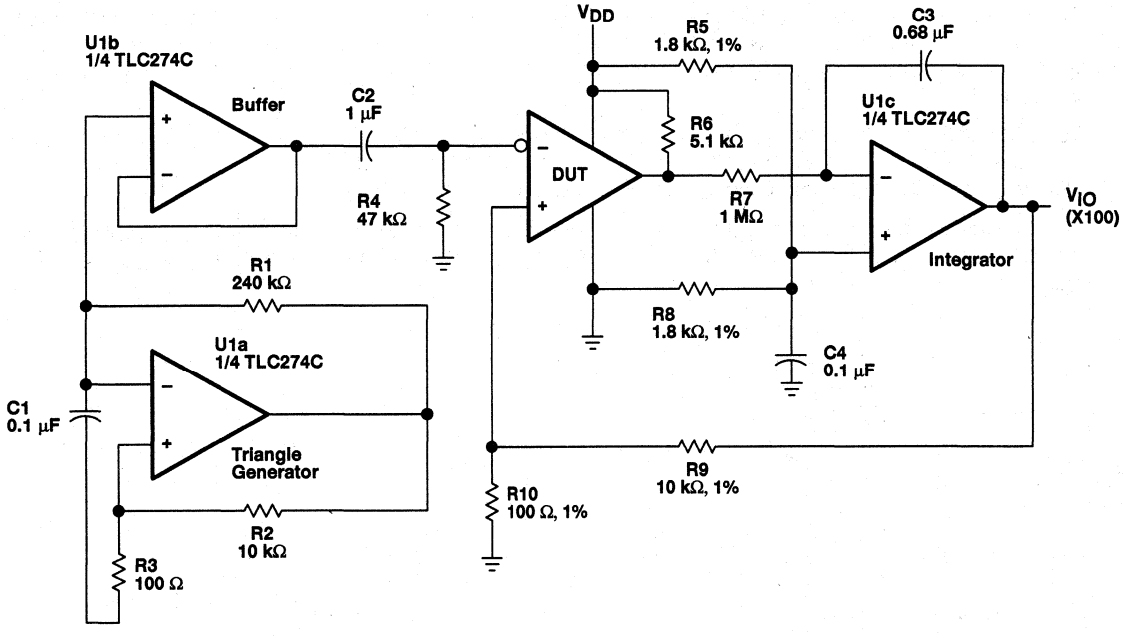
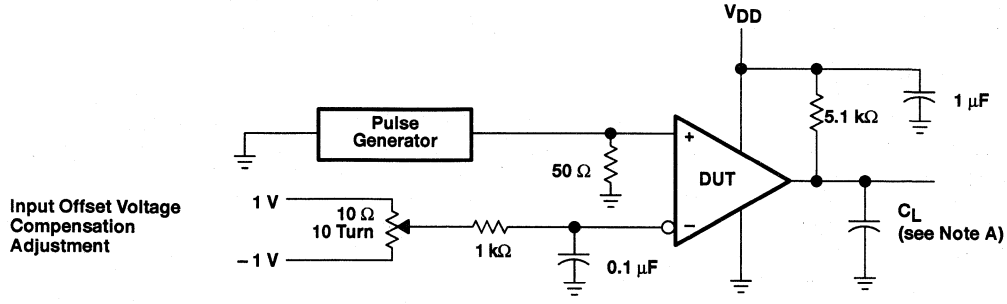


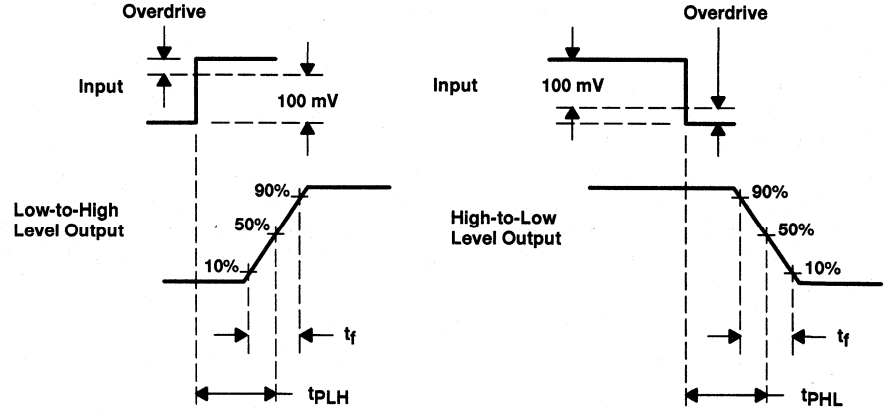
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. A low signal, for example 105 mV or 5 mV overdrive, causes the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise, and Fall Times Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a linear polysilicon-gate CMOS process. Primarily designed for single- supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. Further questions should be directed to the nearest TI sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual operational amplifier is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage build-up, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 4. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

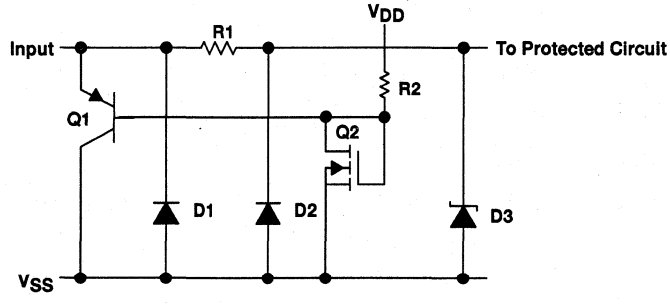


Figure 4. LinCMOS™ ESD-Protection Schematic

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PRINCIPLES OF OPERATION

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive-and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

circuit design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power-up or power-down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 5 and 6 show typical characteristics for input voltage vs input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 5. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 7).

PRINCIPLES OF OPERATION

circuit design considerations (continued)

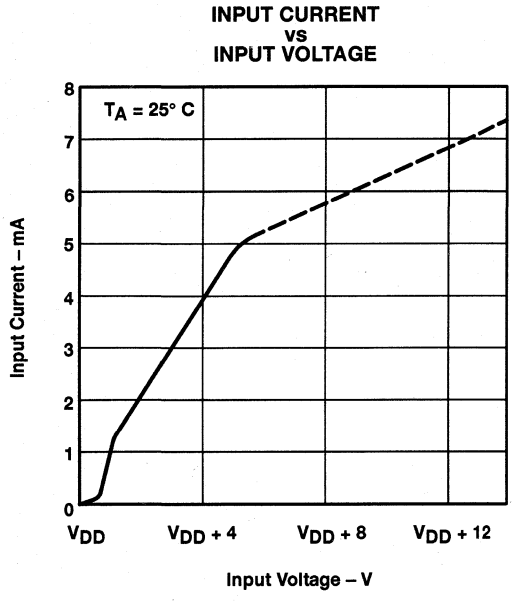


Figure 5

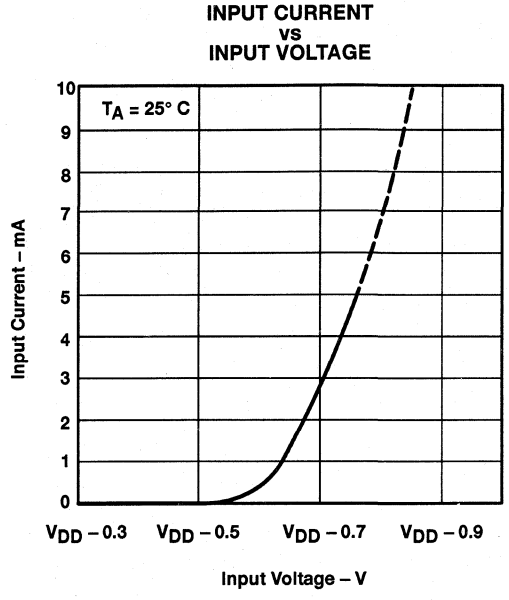
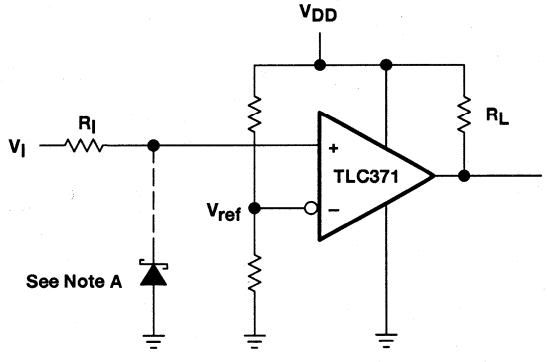


Figure 6



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

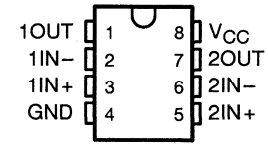
$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds V_{SS}, a Schottky clamp is required.

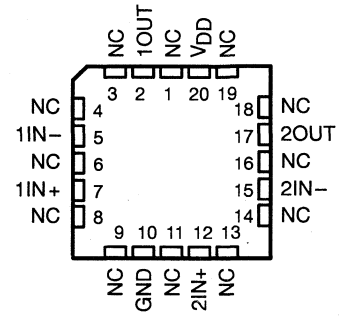
Figure 7. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages 2 V to 18 V**
- **Very Low Supply Current Drain 150 μA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-in ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Output Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM393**

TLC372C, TLC372I, TLC372M, TLC372Q
D, P, OR PW PACKAGE
TLC372M . . . JG PACKAGE
(TOP VIEW)



TLC372M . . . FK PACKAGE
(TOP VIEW)

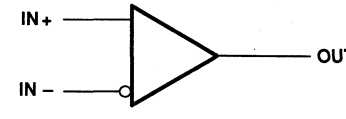


NC – No internal connection

description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)

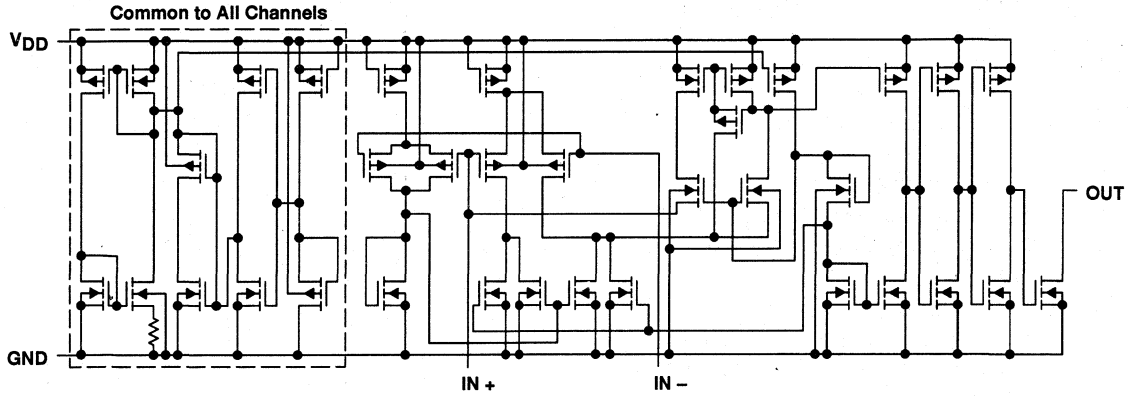


The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372C is characterized for operation from 0°C to 70°C. The TLC372I is characterized for operation from –40°C to 85°C. The TLC372M is characterized for operation over the full military temperature range of –55°C to 125°C. The TLC372Q is characterized for operation from –40°C to 125°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic (each comparator)



AVAILABLE OPTIONS

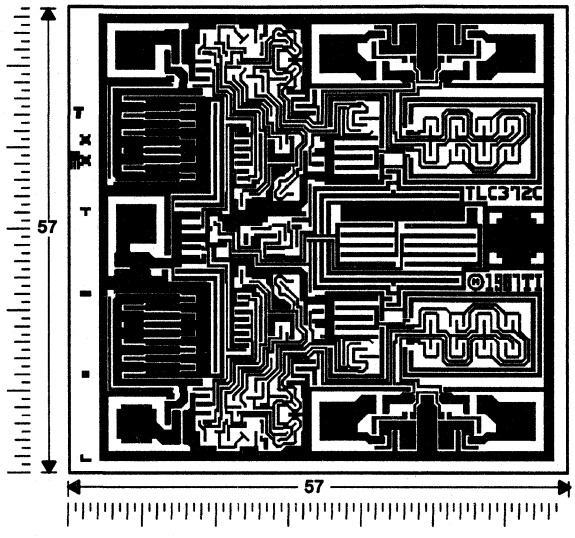
T_A	V_{IO} max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	5 mV	TLC372CD	—	—	TLC372CP	TLC372CPW	TLC372Y
–40°C to 85°C	5 mV	TLC372ID	—	—	TLC372IP	—	—
–55°C to 125°C	5 mV	TLC372MD	TLC372MFK	TLC372MJG	TLC372MP	—	—
–40°C to 125°C	5 mV	TLC372QD	—	—	TLC372QP	—	—

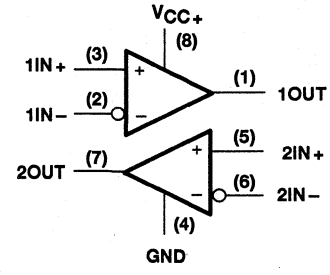
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC372CDR).

TLC372Y chip information

These chips, when properly assembled, display characteristics similar to the TLC372C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 3.6 × 3.6 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2 ..... ±18 V
Input voltage range, V_I ..... −0.3 V to 18 V
Output voltage, V_O ..... 18 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC372C ..... 0°C to 70°C
TLC372I ..... −40°C to 85°C
TLC372M ..... −55°C to 125°C
TLC372Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN –.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	145 mW
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW
PW	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A

recommended operating conditions

		TLC372C		TLC372I		TLC372M		TLC372Q		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0	3.5	0	3.5	0	3.5	0	3.5	V
	V_{DD} = 10 V	0	8.5	0	8.5	0	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	−40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC372C			TLC372I			TLC372M, TLC372Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4	25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			3	µA
V_{OL}	Low-level output voltage	$V_{ID} = -1$ V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	$V_{ID} = -1$ V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		150	300		150	300		150	300	µA
				Full range			400			400			400	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC372C, –40°C to 85°C for TLC372I, and –55°C to 125°C for TLC372M and –40°C to 125°C for TLC372Q. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONST		TLC372Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4		1	5	mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				5		pA
V_{ICR}	Common-mode input voltage range			0 to $V_{DD}-1$			V
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V		0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load		150	300	μA

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. IMPORTANT: See Parameter Measurement Information.

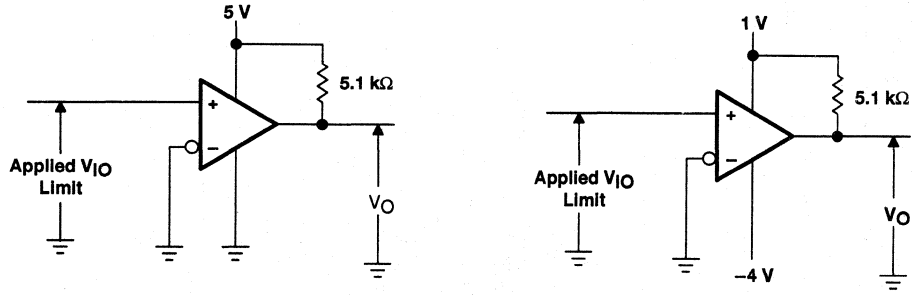
NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC372 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

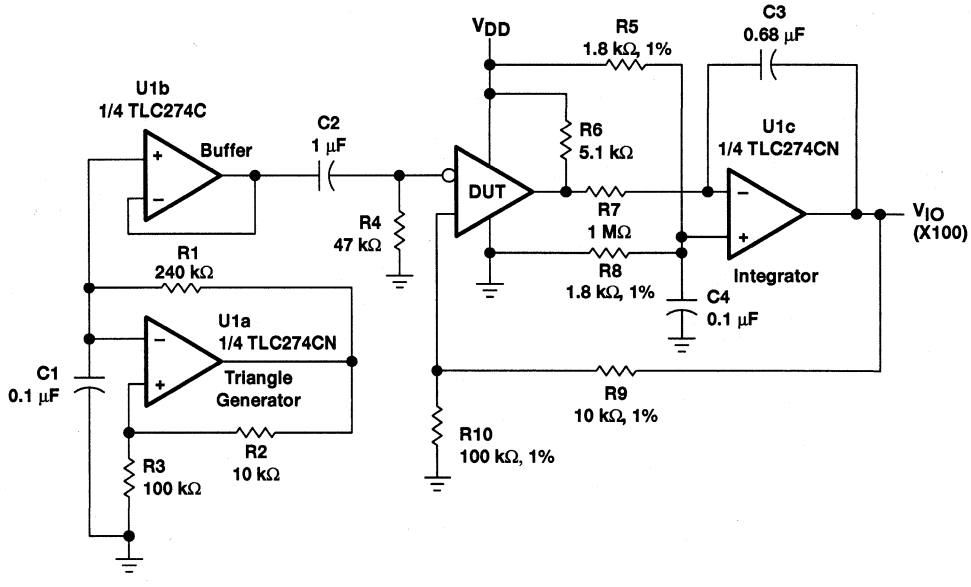
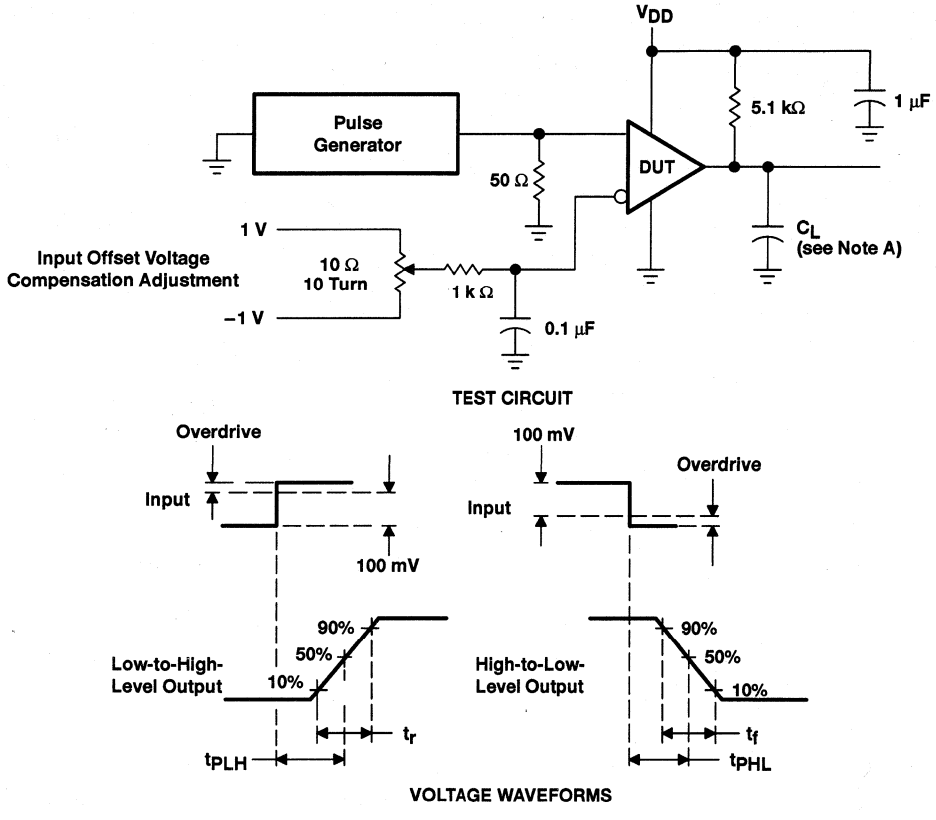


Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Response, Rise, and Fall Times Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a Linear polysilicon-gate complementary-MOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions, from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. Further questions should be directed to the nearest TI field sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g. during board assembly. If a circuit in which one amplifier from a dual operational amplifier is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage build up, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 4. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of TI's ESD-protection circuit is presented on the next page.

All input and output pins on LinCMOS and Advanced LinCMOS™ products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

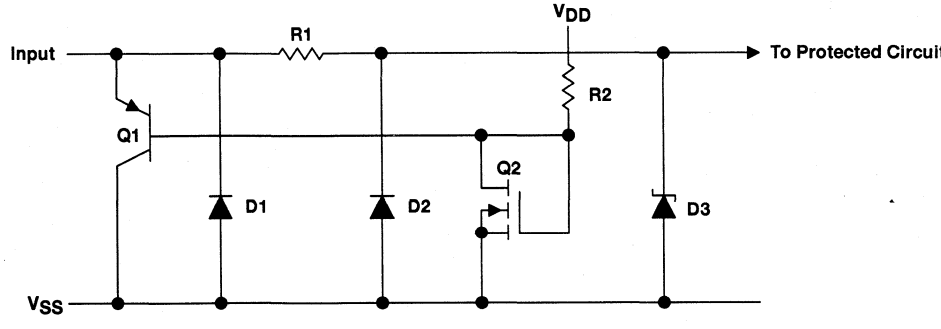


Figure 4. LinCMOS™ ESD-Protection Schematic

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

PRINCIPLES OF OPERATION

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive-and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} Of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 V to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded, and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is −0.3 V to −1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 5 and 6 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 5. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 7).

PRINCIPLES OF OPERATION

circuit-design considerations (continued)

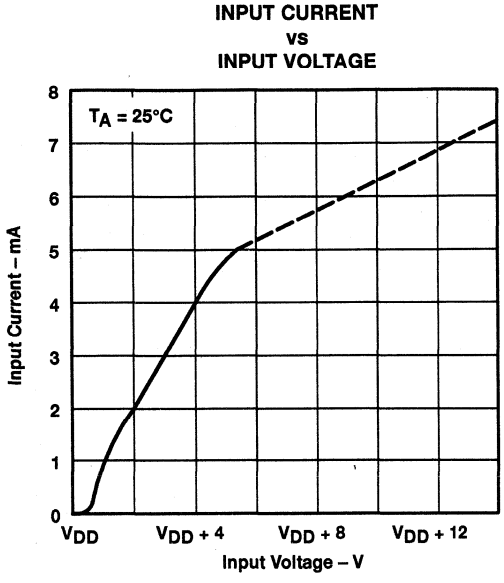


Figure 5

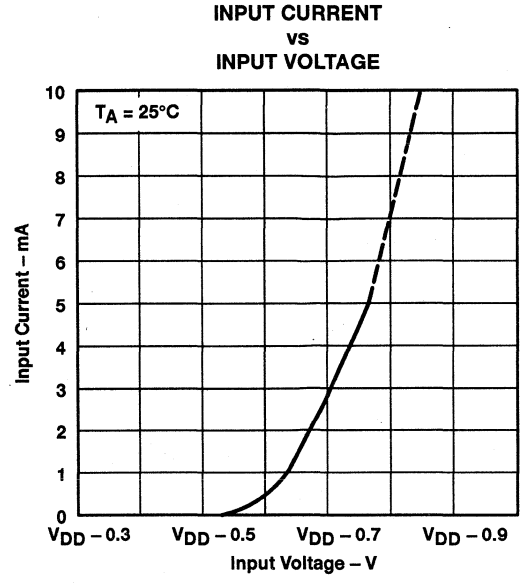
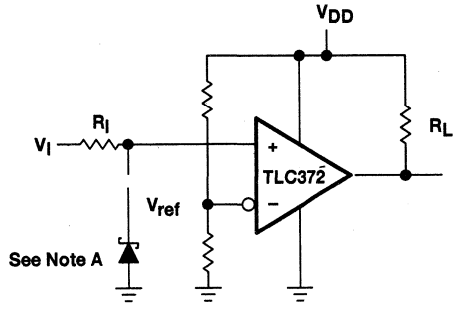


Figure 6



Positive Voltage Input Current Limit:

$$R_I = \frac{+V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

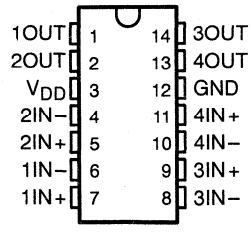
$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct output state is required when the negative input exceeds V_{SS}, a schottky clamp is required.

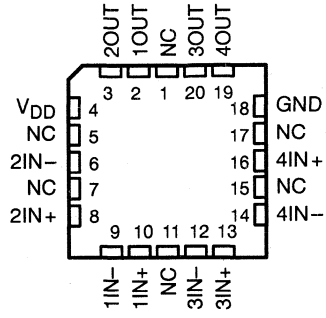
Figure 7. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages 2 V to 18 V**
- **Very Low Supply Current Drain 0.3 mA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM339**

D, J, N, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

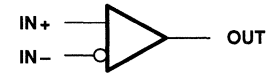


NC – No internal connection

description

These quadruple differential comparators are fabricated using LinCMOS™ technology and consist of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 2 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



The TLC374 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-833C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC374C is characterized for operation from 0°C to 70°C. The TLC374I is characterized for operation from −40° to 85°C. The TLC374M is characterized for operation over full military temperature range of −55°C to 125°C. The TLC374Q is characterized for operation from −40°C to 125°C.

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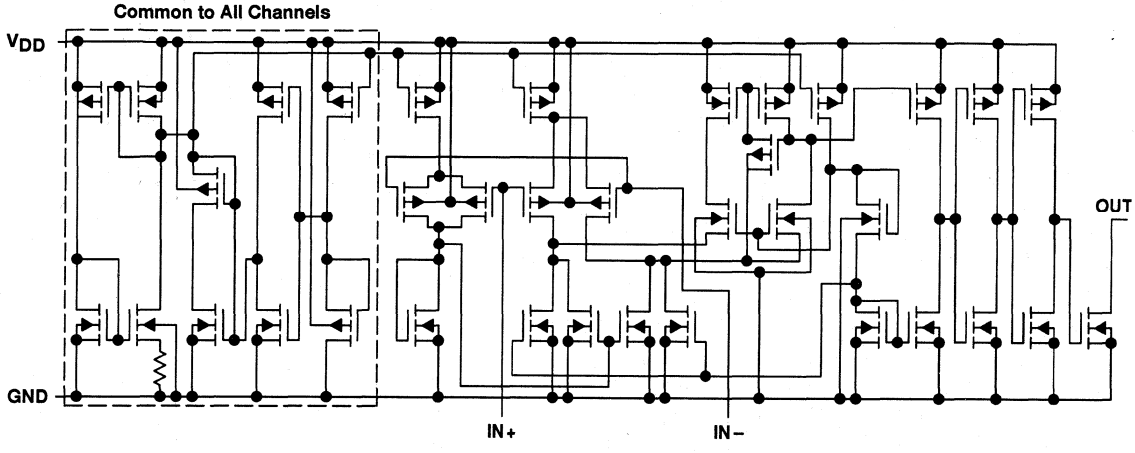
AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	5 mV	TLC374CD	—	—	TLC374CN	TLC374CPW	TLC374Y
−40°C to 85°C	5 mV	TLC374ID	—	—	TLC374IN	—	—
−55°C to 125°C	5 mV	TLC374MD	TLC374MFK	TLC374MJ	TLC374MN	—	—
−40°C to 125°C	5 mV	TLC374QD	—	—	TLC374QN	—	—

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC374CDR).

equivalent schematic (each comparator)

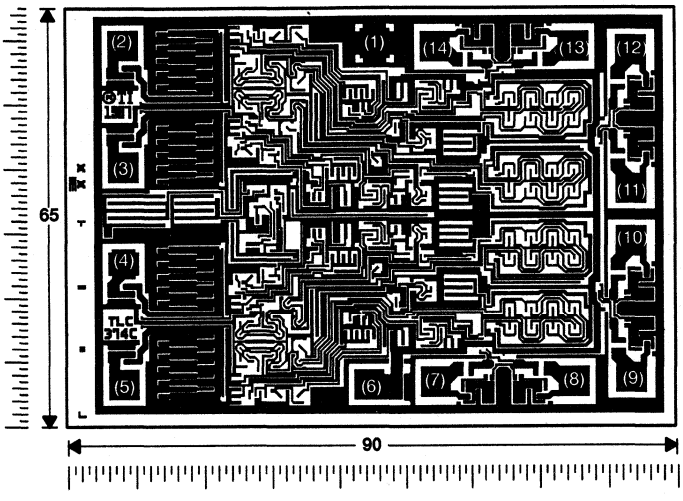


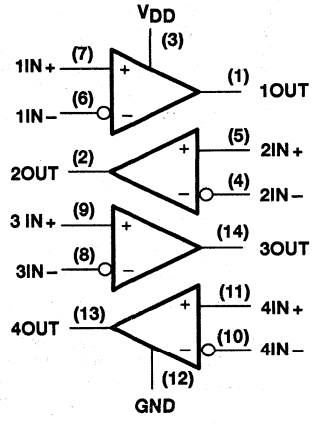
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLC374Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC374C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ±18 V
Input voltage, V_I ..... V_{DD}
Input voltage range, V_I ..... −0.3 V to 18 V
Output voltage, V_O ..... 18 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short circuit to ground (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC374C ..... 0°C to 70°C
TLC374I ..... −40°C to 85°C
TLC374M ..... −55°C to 125°C
TLC374Q ..... −40°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature range for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, N, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN −.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mV	7.6 mW/°C	84°C	500 mW	494 mW	190 mW
FK	500 mV	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J	500 mV	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
N	500 mV	9.2 mW/°C	95°C	500 mW	500 mW	230 mW
PW	700 mV	5.6 mW/°C	—	448 mW	—	—

recommended operating conditions

		TLC374C		TLC374I		TLC374M		TLC374Q		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	3	16	4	16	3	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0	3.5	0	3.5	0	3.5	0	3.5	V
	V_{DD} = 10 V	0	8.5	0	8.5	0	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	−40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC374C			TLC374I			TLC374M			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	$V_{ID} = -1$ V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	$V_{ID} = -1$ V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	$V_{ID} = -1$ V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	$V_{ID} = -1$ V,	No load	25°C		300	600		300	600		300	600	mA
				Full range			800			800			800	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC374C, –40°C to 85°C for TLC374I, and –55°C to 125°C for the TLC374M, and –40°C to 125°C for TLC374Q. MAX is 70°C for TLC374C, 85°C TLC374I, and 125°C for the TLC374M, and 125°C for TLC374Q. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC374C, TLC374I TLC374M, TLC374Q			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC374Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4		1	5	mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				5		pA
V_{ICR}	Common-mode input voltage range			0 to $V_{DD}-1$			V
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V		0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 mV	6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} =1 V,	No load		300	600	μA

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLC374Y			UNIT
			MIN	TYP	MAX	
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF†, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

† C_L includes probe and jig capacitance.
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC374 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity to the input offset voltage, the output changes state.

PARAMETER MEASUREMENT INFORMATION

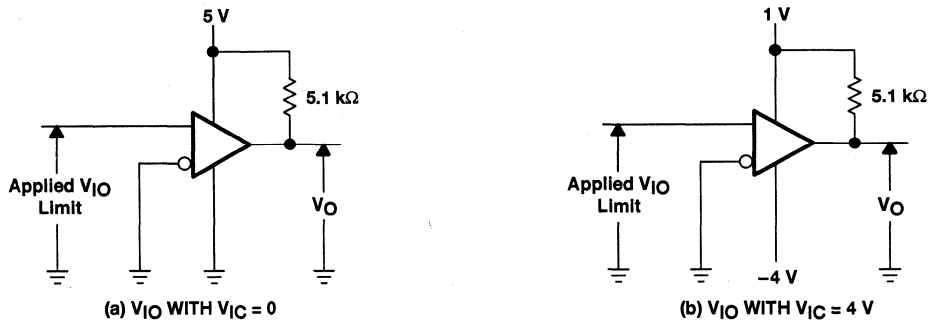


Figure 1. Method for Verifying That Input Offset Voltage is Within Specified Limits

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

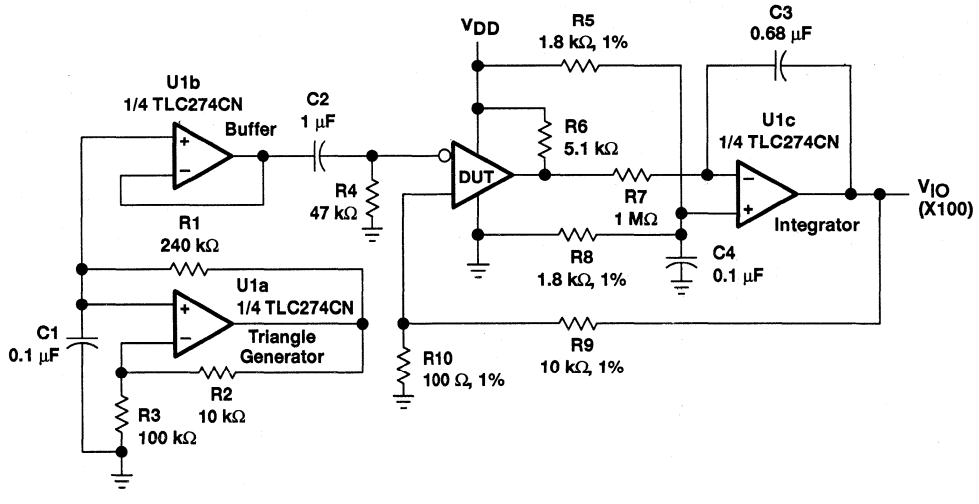
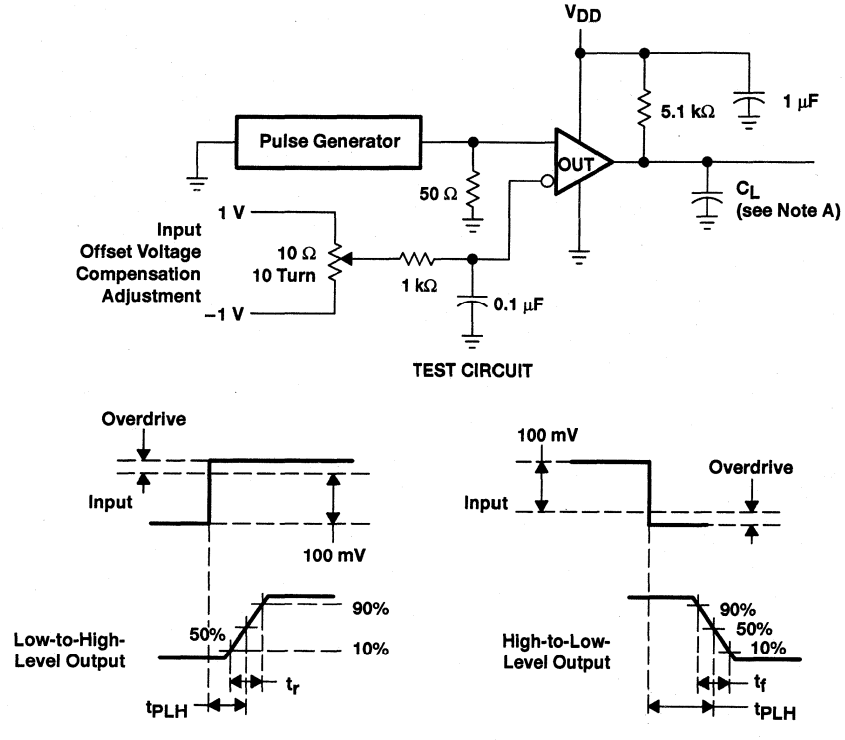


Figure 2. Test Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Response, Rise, and Fall Times Test Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

LinCMOS™ process

LinCMOS™ process is a linear polysilicon-gate complimentary-MOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. Further questions should be directed to the nearest TI field sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g. during board assembly. If a circuit in which one amplifier from a dual operational amplifier is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage build up, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 4. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of TI's ESD-protection circuit is presented on the next page.

All input an output pins of LinCMOS™ and Advanced LinCMOS™ products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

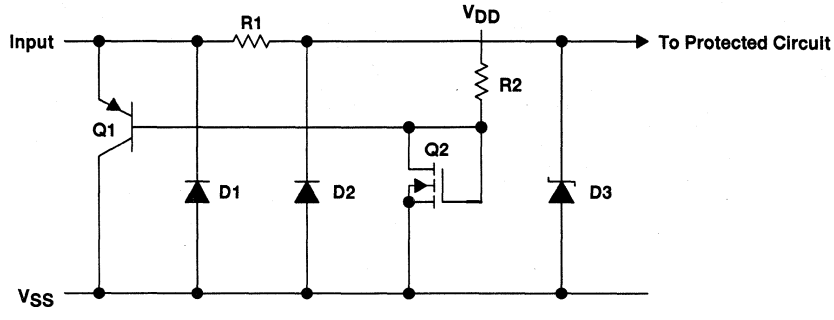


Figure 4. LinCMOS™ ESD-Protection Schematic

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PRINCIPLES OF OPERATION

Input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on V_{DD} by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 as Q1 saturates forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn on Q2. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of d3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward-biased. The voltage seen by the protected circuit is −0.3 V to −1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuits environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 5 and 6 show typical characteristics for input voltage vs input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. The input current should be externally limited even through internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 5. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2, and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 7).

PRINCIPLES OF OPERATION

circuit-design considerations (continued)

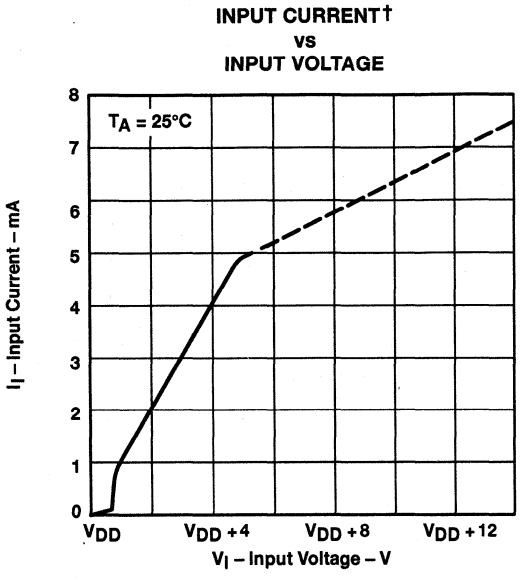


Figure 5

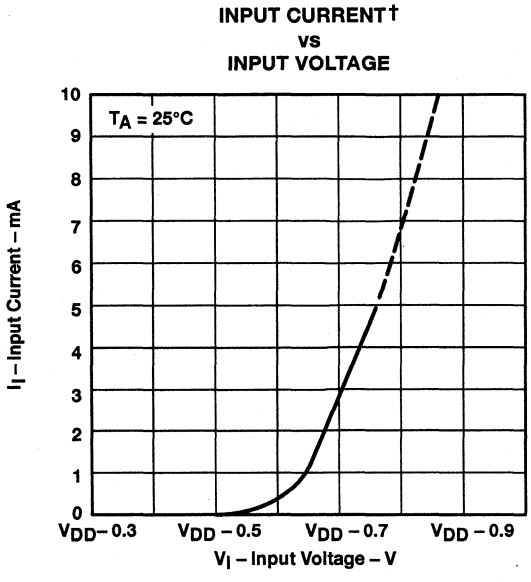
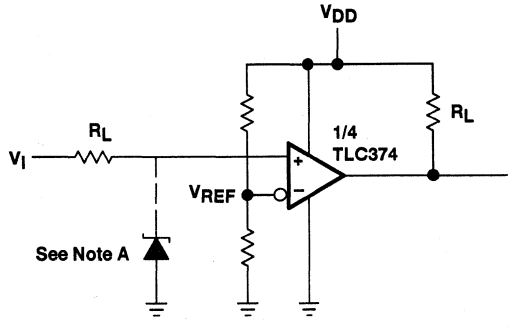


Figure 6

† The dashed line identifies an area of operation where some degradation of parametric performance may be experienced.



Positive Voltage Input Current Limit:

$$R_I = \frac{+V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (0.3\ V)}{5\ mA}$$

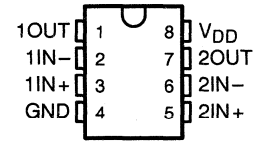
NOTE A: If the correct output state is required when the negative input exceeds V_{SS}, a schotty clamp is required.

Figure 7. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

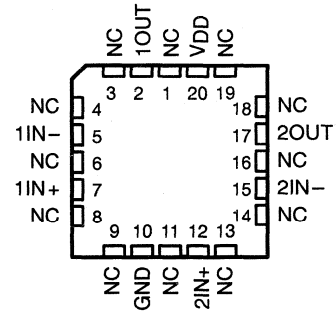
SLCS115 – DECEMBER 1986 – REVISED JANUARY 1992

- **Very Low Power . . . 110 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.5 μs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  TLC393C . . . 3 V to 16 V
  TLC393I . . . 3 V to 16 V
  TLC393M . . . 4 V to 16 V
- **On-Chip ESD Protection**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

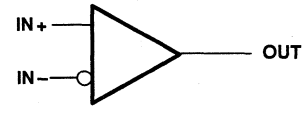
description

The TLC393 consists of dual independent micropower voltage comparators designed to operate from a single supply. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of loads and supplies. For a similar device with a push-pull output configuration (see the TLC3702 data sheet).

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC393C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC393I is characterized for operation over the extended industrial temperature range of – 40°C to 85°C. The TLC393M is characterized for operation over the full military temperature range of – 55°C to 125°C.

symbol (each comparator)



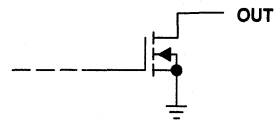
AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC393CD	—	—	TLC393CP
– 40°C to 85°C	5 mV	TLC393ID	—	—	TLC393IP
– 55°C to 125°C	5 mV	TLC393MD	TLC393MFK	TLC393MJG	TLC393MP

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC393CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

schematic



OPEN-DRAIN CMOS OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... – 0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ± 18 V
Input voltage range, V_I ..... – 0.3 V to V_{DD}
Output voltage range, V_O ..... – 0.3 V to V_{DD}
Input current, I_I ..... ± 5 mA
Output current, I_O (each output) ..... 20 mA
Total supply current into V_{DD} ..... 40 mA
Total current out of GND ..... 40 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TLC393C ..... 0°C to 70°C
TLC393I ..... – 40°C to 85°C
TLC393M ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

recommended operating conditions

	TLC393C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC393C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			0°C to 70°C	0 to V_{DD} – 1.5			
CMMR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	µA
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		22	40	µA
			0°C to 70°C			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC393I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC393I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
						7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			– 40°C to 85°C	0 to V_{DD} – 1.5			
CMMR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			– 40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			– 40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	µA
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		22	40	µA
			– 40°C to 85°C			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC393M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		V_{DD} – 1.5	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC393M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			– 55°C to 125°C	0 to V_{DD} – 1.5			
CMMR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		84		
			– 55°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			– 55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		22	40	µA
			– 55°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V (with a 2.5-kΩ load to V_{DD}).

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

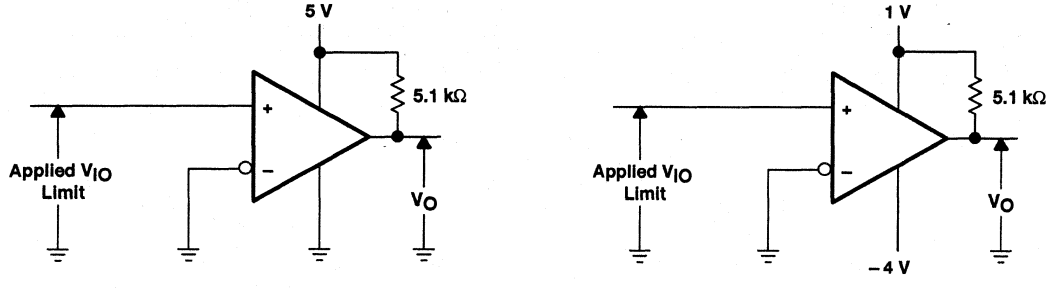
PARAMETER		TEST CONDITIONS		TLC393C, TLC393I TLC393M			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.1		
t_{PHL}	Propagation delay time, high-to-low-level output	V_I = 1.4-V step at IN+			1.1		
		f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4-V step at IN+			0.10		
t_f	Fall time, output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		22		ns

PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection ratio, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

The voltage divider formed by R9 and R10 provides an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

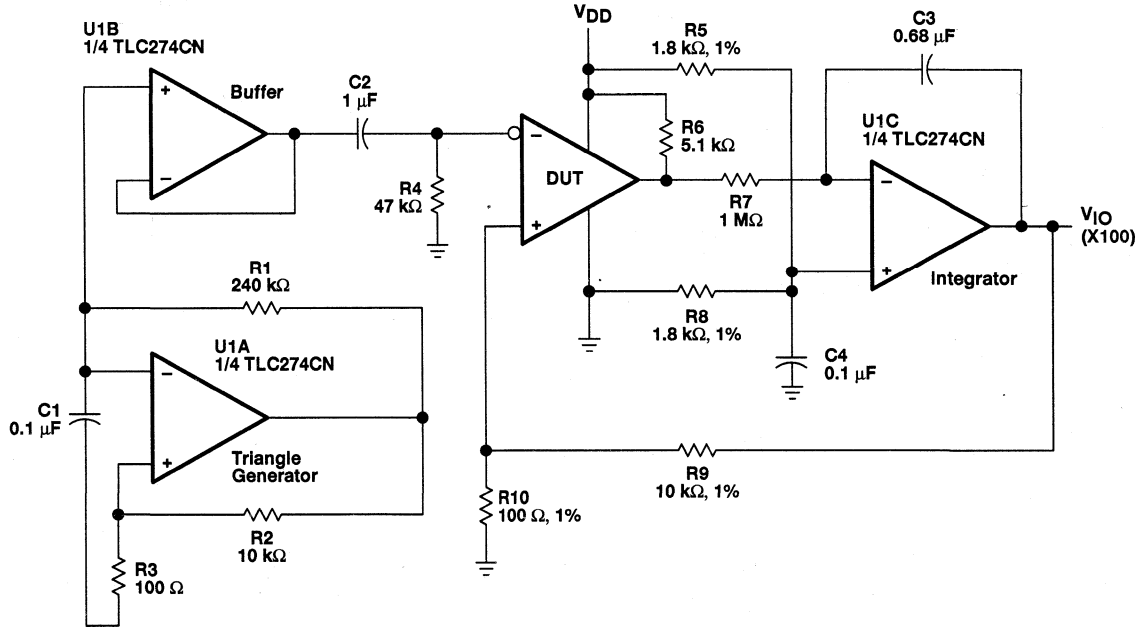
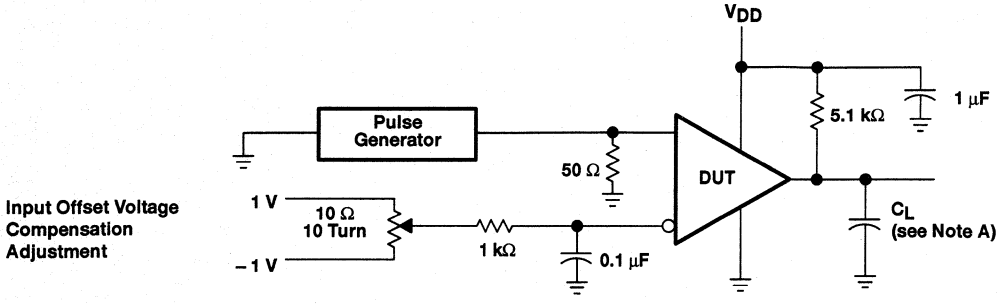


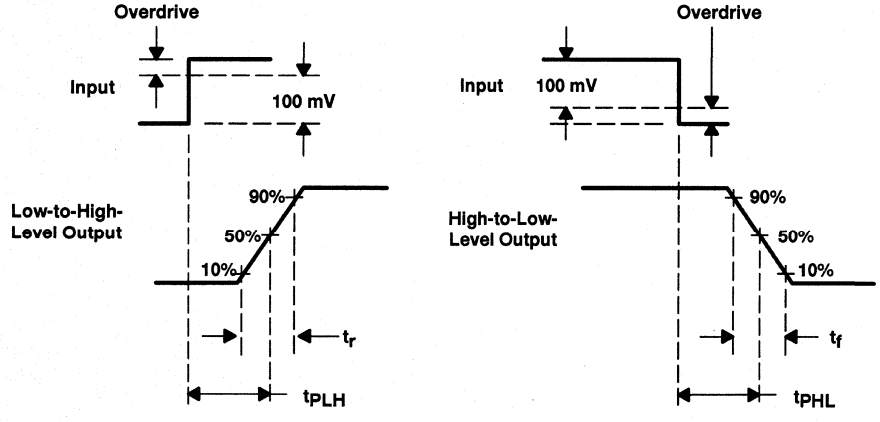
Figure 2. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example, 105 mV or 5 mV overdrive, causes the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise Time, and Fall Time Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Free-air temperature	6
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	7
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	8 9
I_{OH}	Low-level output current	vs High-level output voltage vs Free-air temperature	10 11
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	12 13
t_{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	14
t_{PHL}	High-to-low level output propagation delay time	vs Supply voltage	15
	Low-to-high-level output response	Low-to-high level output propagation delay time	16
	High-to-low level output response	High-to-low level output propagation delay time	17
t_f	Fall time	vs Supply voltage	18

DISTRIBUTION OF INPUT OFFSET VOLTAGE

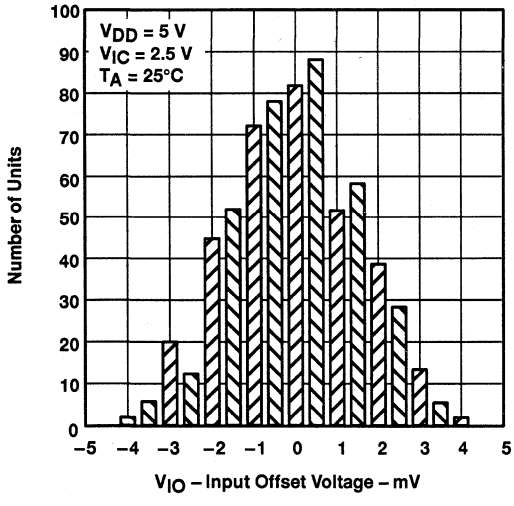


Figure 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

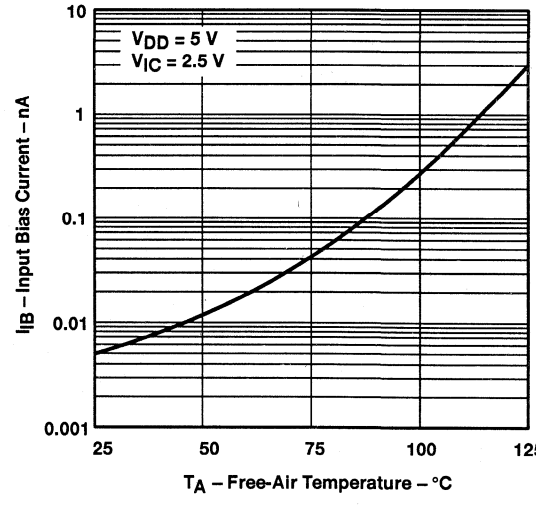


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

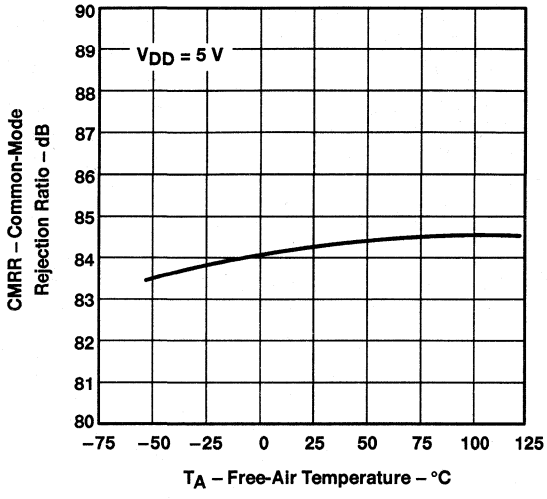


Figure 6

SUPPLY VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

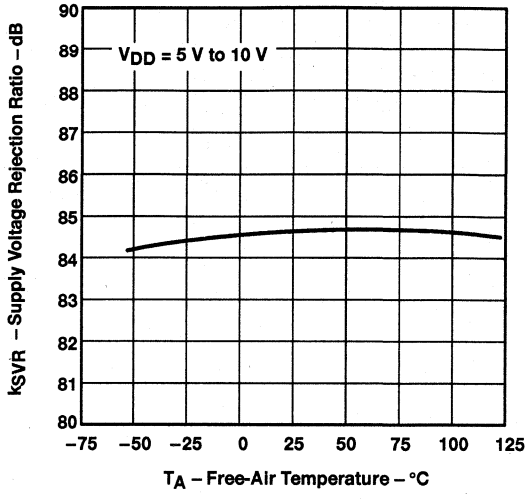


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

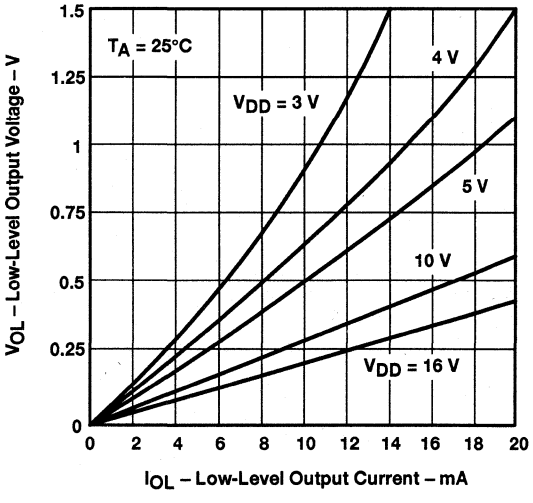


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

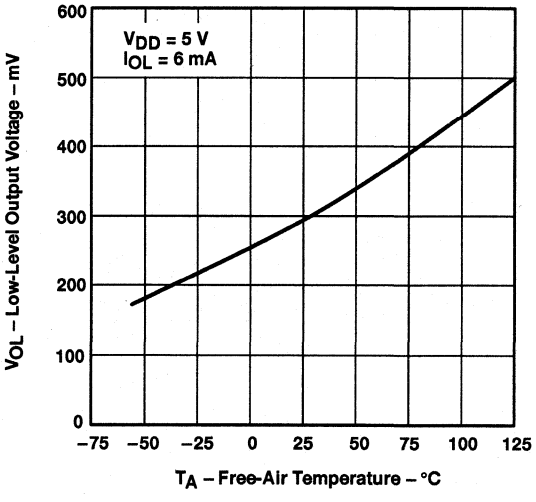


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

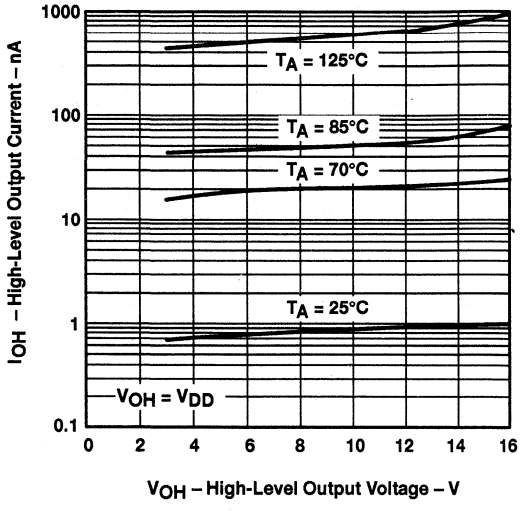


Figure 10

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

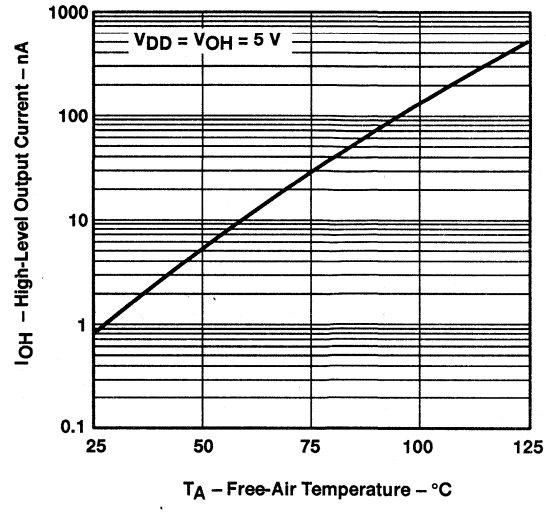


Figure 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

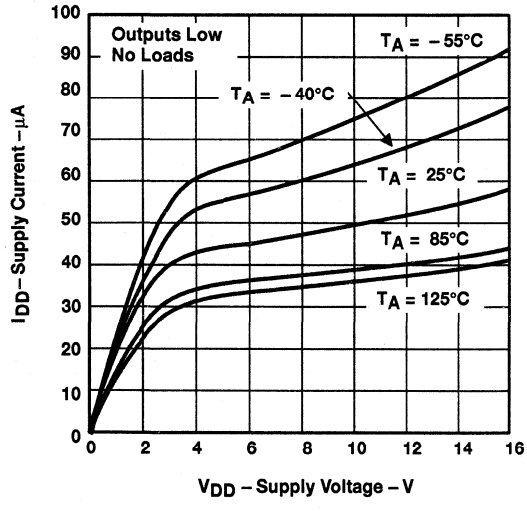


Figure 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

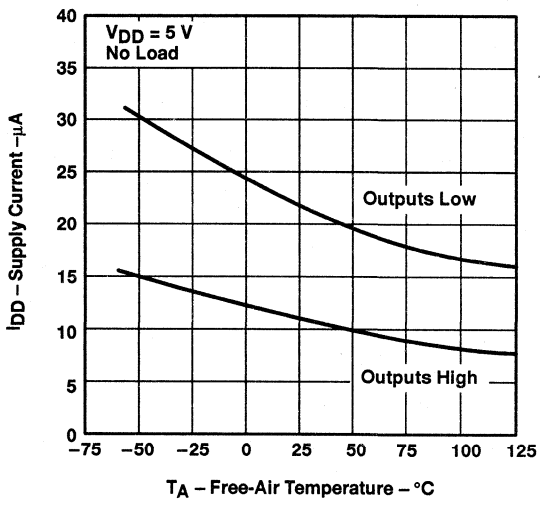


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

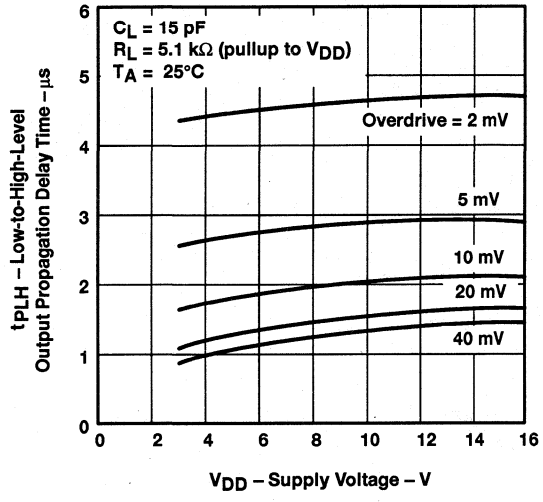


Figure 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

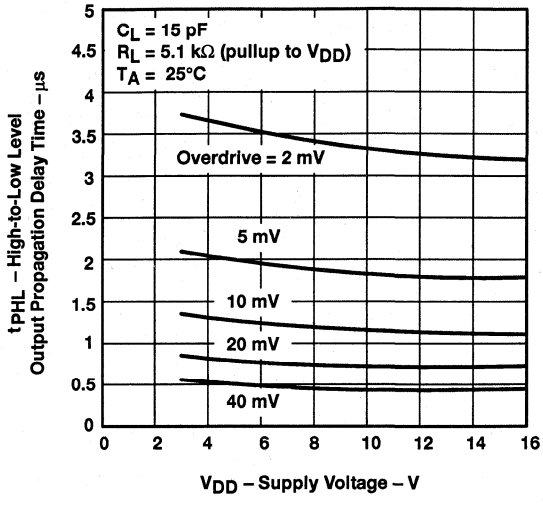


Figure 15

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS INPUT OVERDRIVES

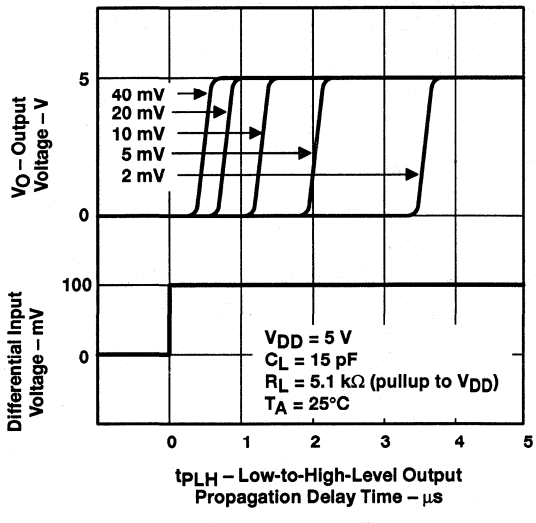


Figure 16

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS INPUT OVERDRIVES

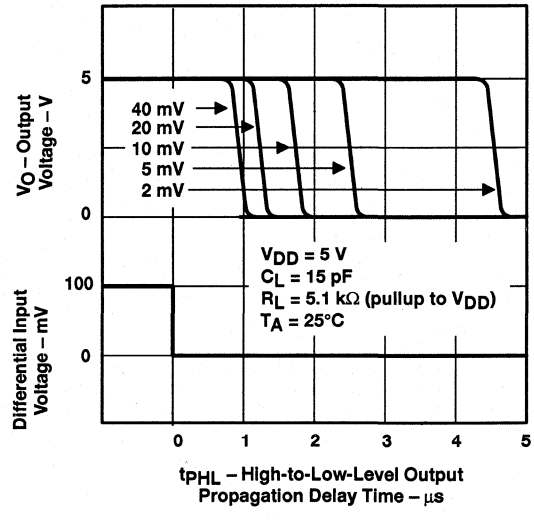


Figure 17

TYPICAL CHARACTERISTICS

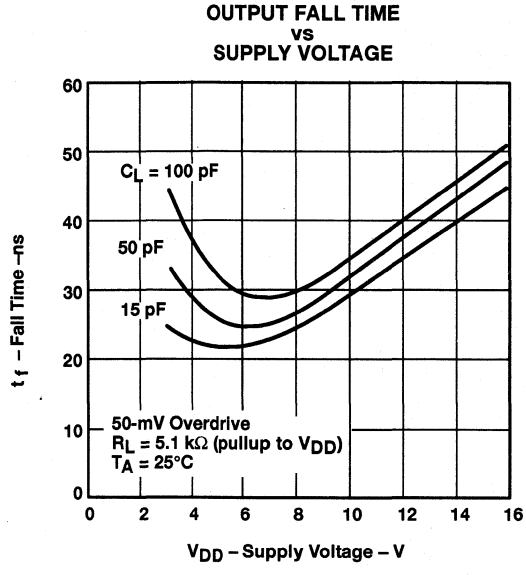


Figure 18

APPLICATION INFORMATION

The input should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not be damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between – 0.2 V and 4 V to assure proper device operation.

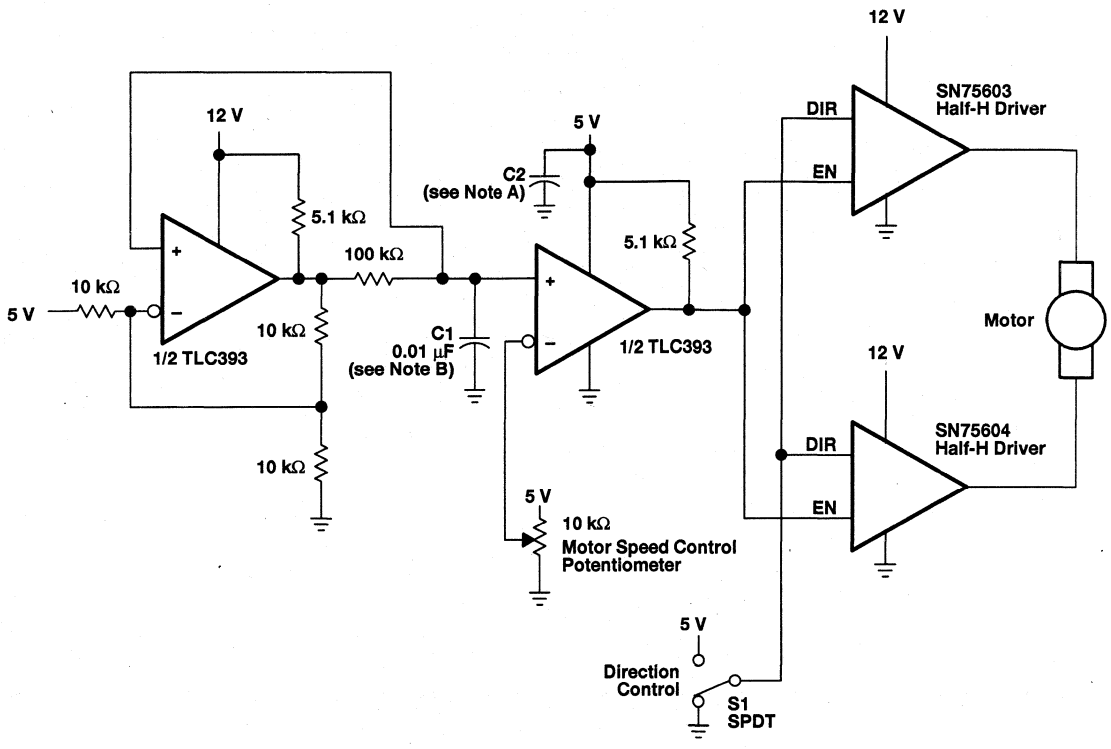
To assure reliable operation, the supply should be decoupled with a capacitor (0.1-μF) positioned as close to the device as possible.

The TLC393 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

	FIGURE
Pulse-width-modulated motor speed controller	19
Enhanced supply supervisor	20
Two-phase nonoverlapping clock generator	21
Micropower switching regulator	28

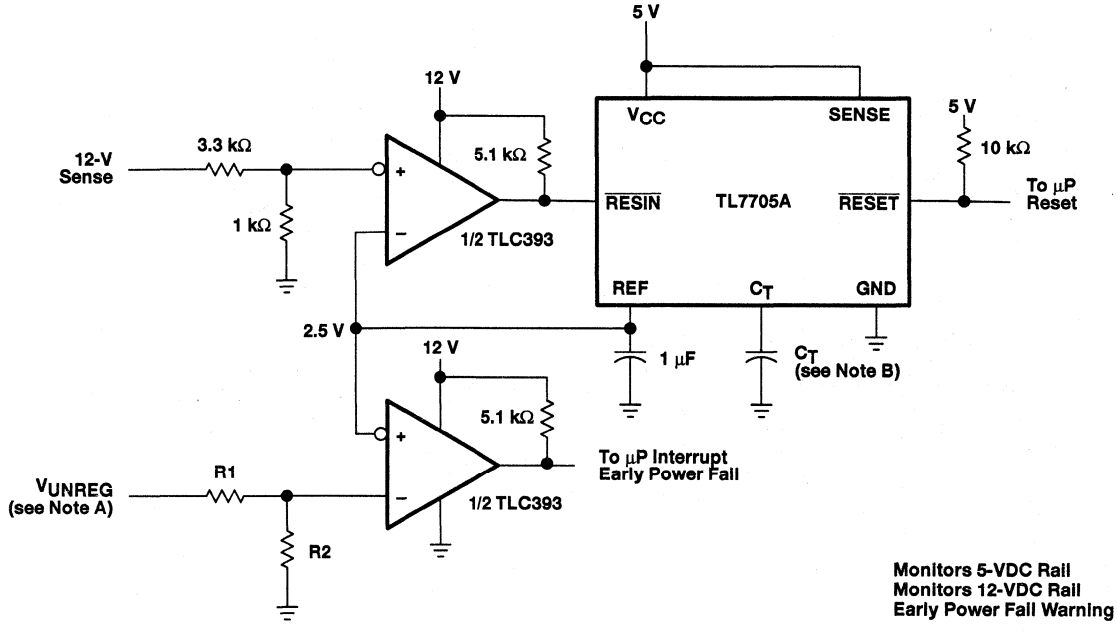
APPLICATION INFORMATION



NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency.

Figure 19. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

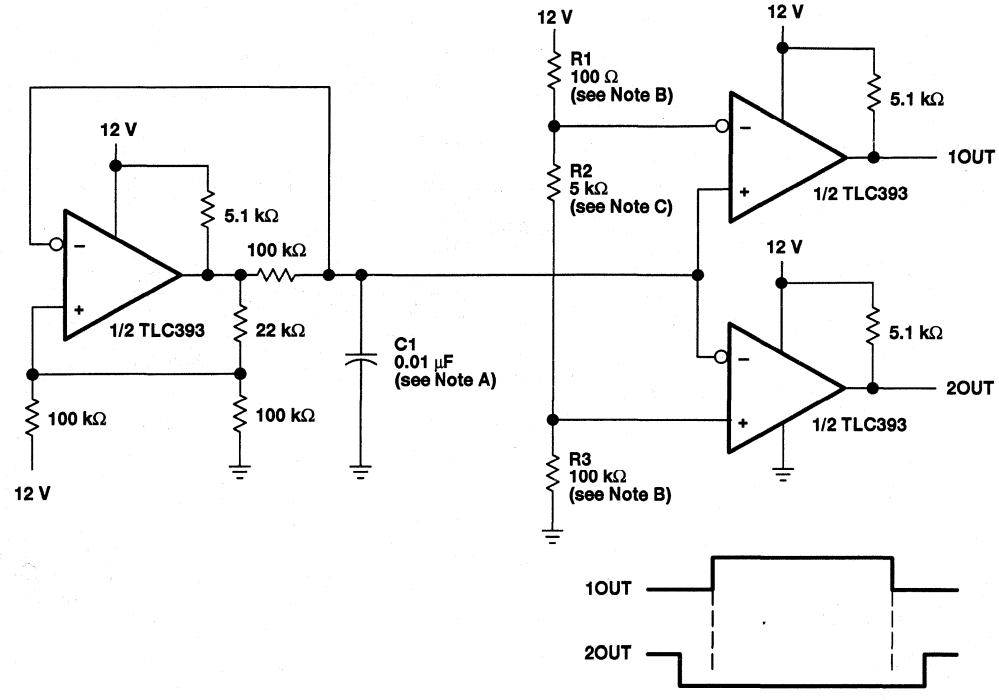


NOTES: A. $V_{UNREG} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor

APPLICATION INFORMATION

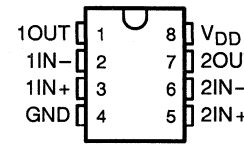


NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\ k\Omega)C1$
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

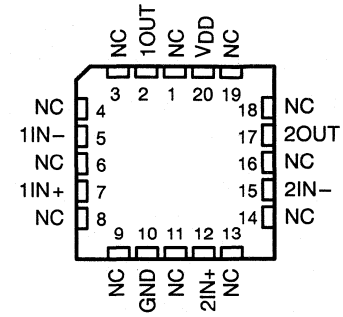
Figure 21. Two-Phase Nonoverlapping Clock Generator

- **Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, $I_O = \pm 8$ mA**
- **Very Low Power . . . 100 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.7 μs Typ With 5-mV Overdrive**
- **Single-Supply Operation . . . 3 V to 16 V**
  TLC3702M . . . 4 V to 16 V
- **On-Chip ESD Protection**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



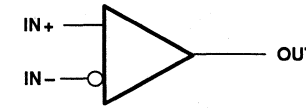
NC – No internal connection

description

The TLC3702 consists of two independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use 1/20th the power for similar response times. The push-pull CMOS output stage drives capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3702I is characterized for operation over the extended industrial temperature range of – 40°C to 85°C. The TLC3702M is characterized for operation over the full military temperature range of – 55°C to 125°C. The TLC3702Q is characterized for operation from – 40°C to 125°C.

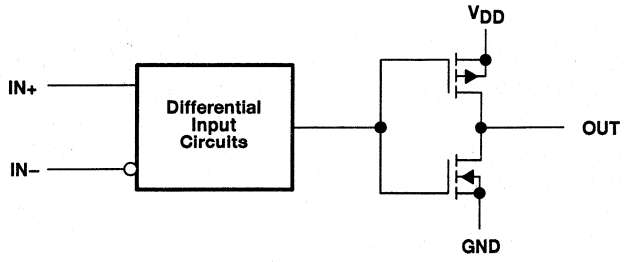
AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGES			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC3702CD	—	—	TLC3702CP
– 40°C to 85°C	5 mV	TLC3702ID	—	—	TLC3702IP
– 55°C to 125°C	5 mV	—	TLC3702MFK	TLC3702MJG	—
– 40°C to 125°C	5 mV	—	—	TLC3702QJG	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC3702CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... – 0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ± 18 V
Input voltage range, V_I ..... – 0.3 to V_{DD}
Output voltage range, V_O ..... – 0.3 to V_{DD}
Input current, I_I ..... ± 5 mA
Output current, I_O (each output) ..... ± 20 mA
Total supply current into V_{DD} ..... 40 mA
Total current out of GND ..... 40 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC3702C ..... 0 to 70°C
TLC3702I ..... – 40°C to 85°C
TLC3702M ..... – 55°C to 125°C
TLC3702Q ..... – 40°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	TLC3702C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC3702C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min,	See Note 3	25°C		1.2	5	mV
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				70°C			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				0°C to 70°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C		84		dB
				70°C		84		
				0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				70°C		85		
				0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				70°C			375	
I_{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		18	40	µA
				0°C to 70°C			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3702I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC3702I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min,	See Note 3	25°C		1.2	5	mV
				– 40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				85°C			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				– 40°C to 85°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C		84		dB
				85°C		84		
				– 40°C		83		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				85°C		85		
				– 40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				85°C			400	
I_{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		18	40	µA
				– 40°C to 85°C			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3702M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC3702M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min,	See Note 3	25°C		1.2	5	mV
				– 55°C to 125°C				
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				– 55°C to 125°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C		84		dB
				125°C		83		
				– 55°C		82		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		85		
				– 55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				125°C			500	
I_{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		18	40	µA
				– 55°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3702Q			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC3702Q			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min,	See Note 3	25°C		1.2	5	mV
				– 40°C to 125°C				
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				– 40°C to 125°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C		84		dB
				125°C		83		
				– 40°C		83		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		85		
				– 40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				125°C			500	
I_{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		18	40	µA
				– 40°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC3702C, TLC3702I TLC3702M, TLC3702Q			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
t_{PHL}	Propagation delay time, high-to-low-level output†	V_I = 1.4 V step at IN +			1.1		
		f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN +			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

† Simultaneous switching of inputs causes degradation in output response.

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. Further questions should be directed to the nearest TI field sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

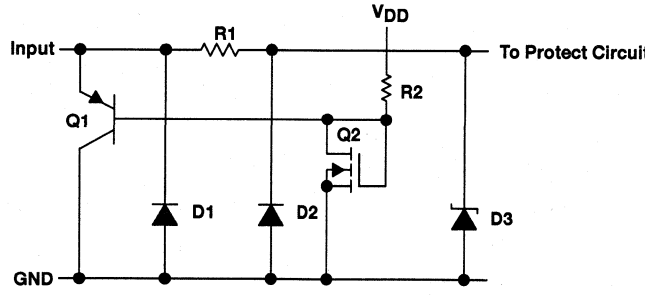


Figure 1. LinCMOS™ ESD-Protection Schematic

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PRINCIPLES OF OPERATION

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figure 2 and Figure 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

PRINCIPLES OF OPERATION

circuit-design considerations (continued)

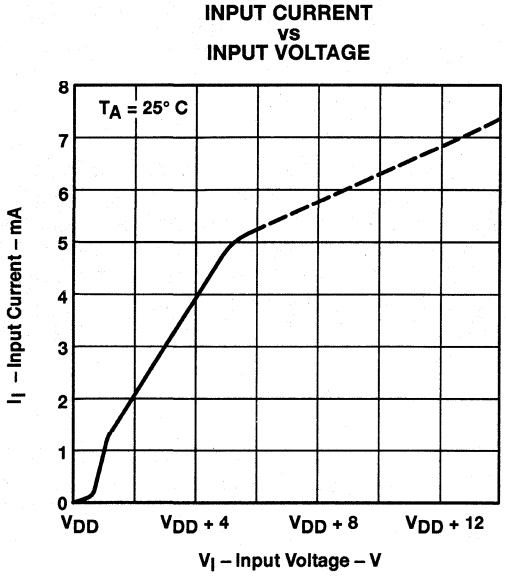


Figure 2

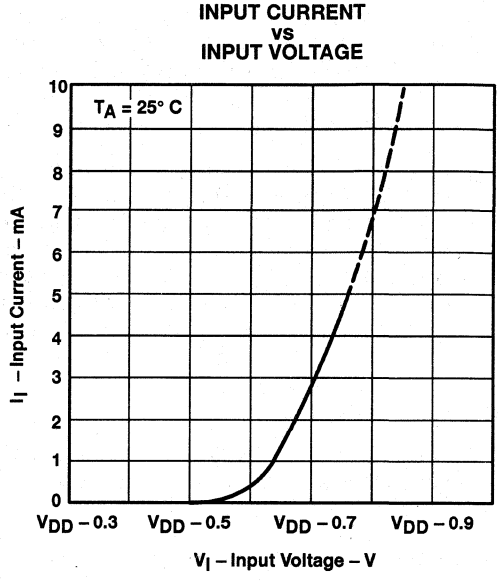
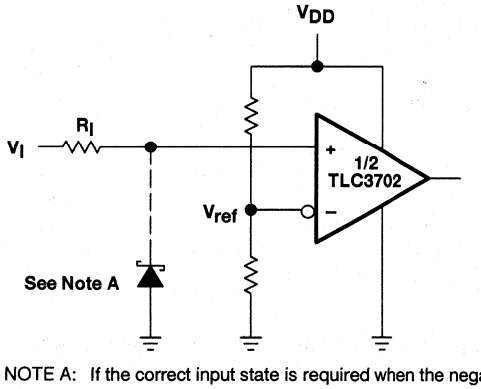


Figure 3



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

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PARAMETER MEASUREMENT INFORMATION

The TLC3702 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

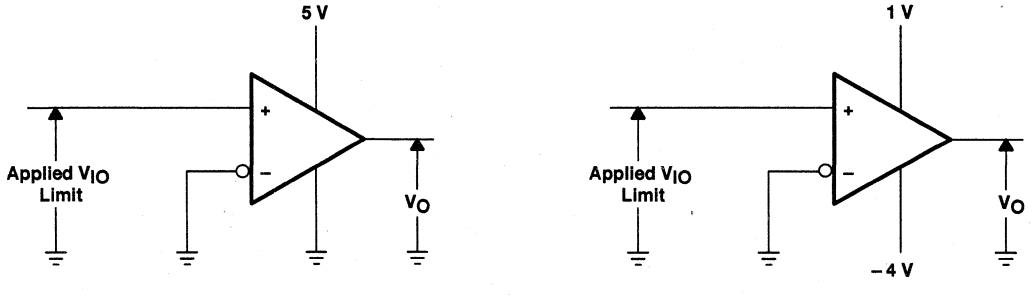
A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 5(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

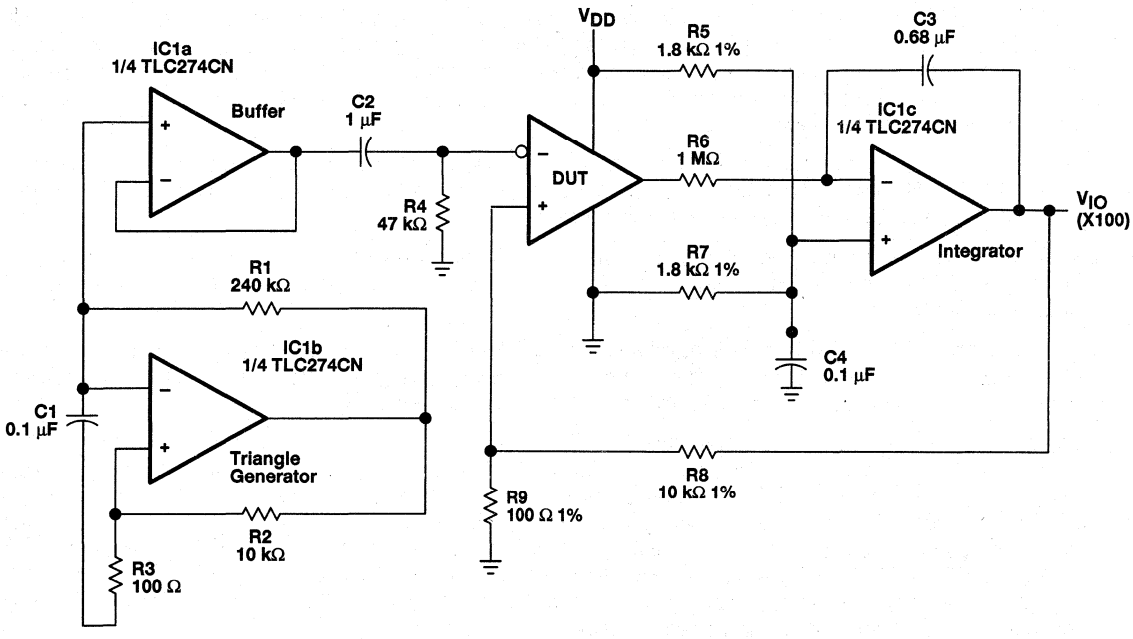
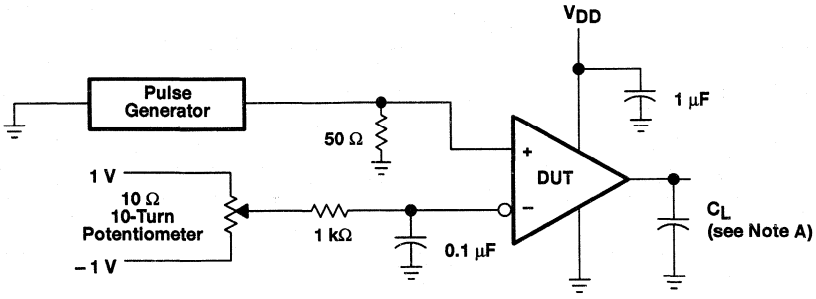


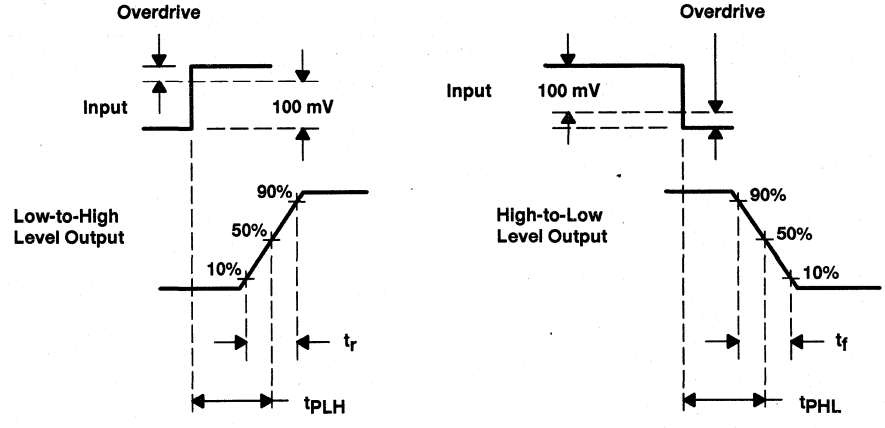
Figure 6. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 7, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Table of Graphs

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DISTRIBUTION OF INPUT OFFSET VOLTAGE

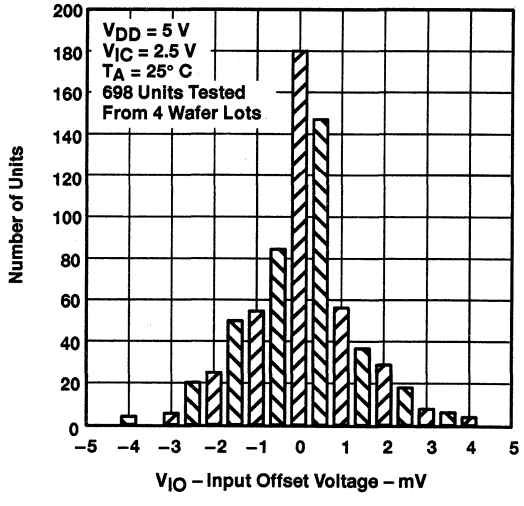


Figure 8

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

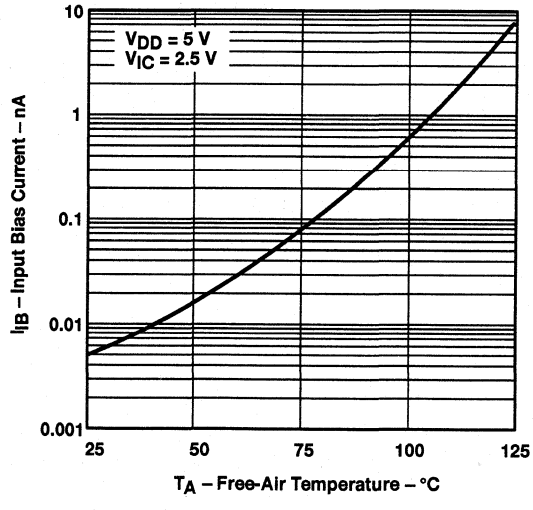


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

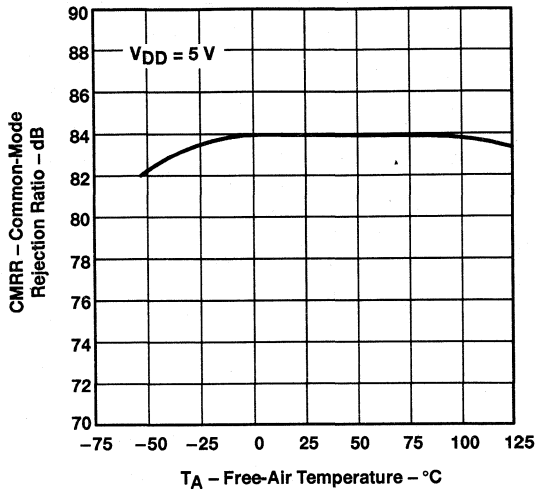


Figure 10

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

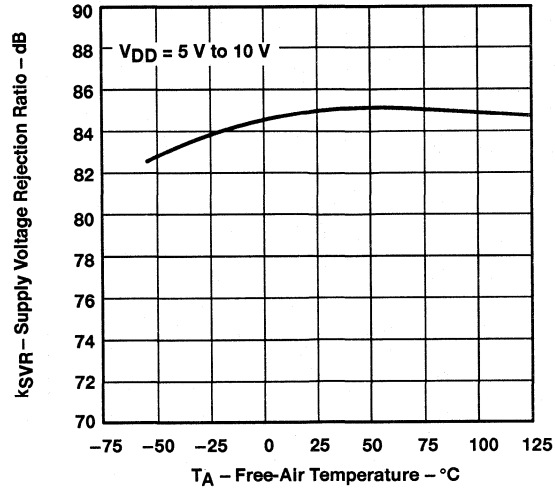


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

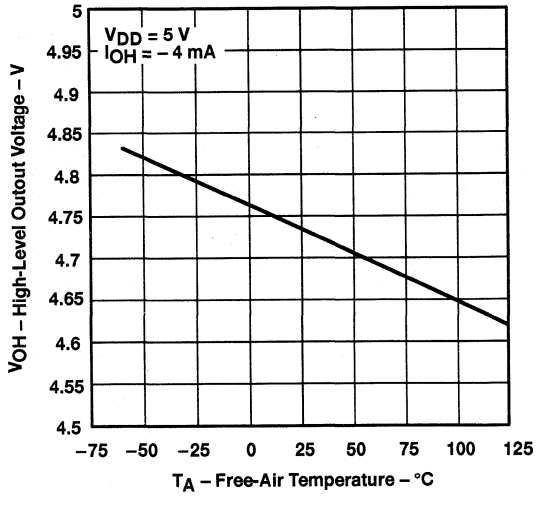


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

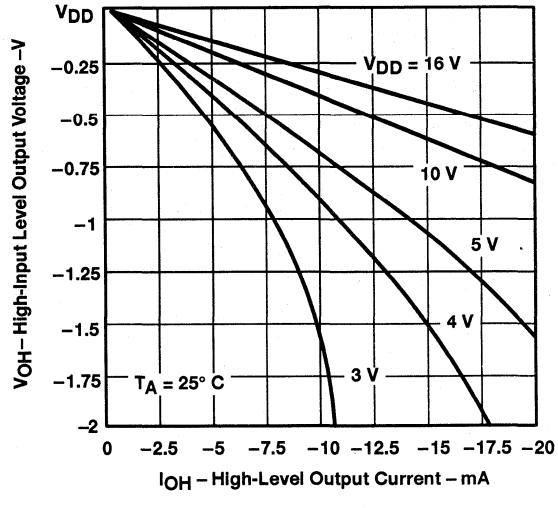


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

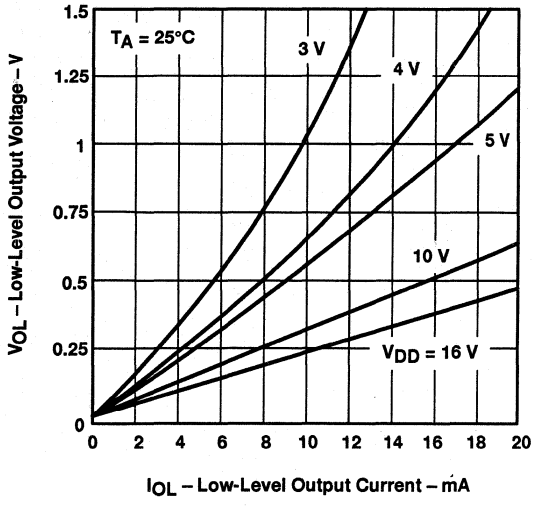


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

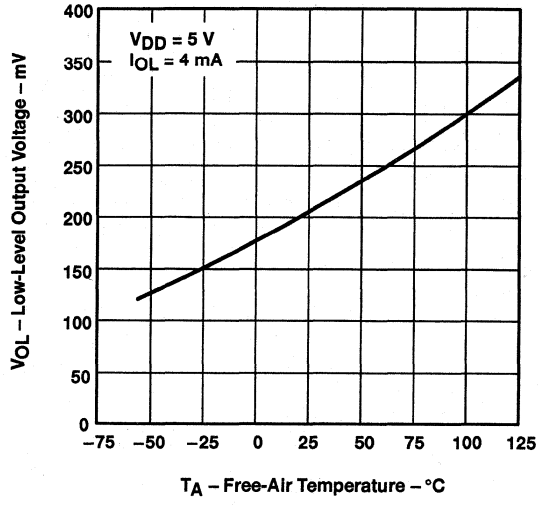


Figure 15

OUTPUT TRANSITION TIME vs LOAD CAPACITANCE

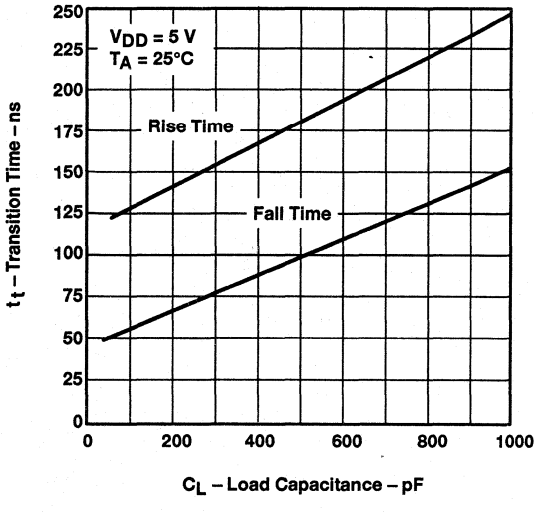


Figure 16

SUPPLY CURRENT RESPONSE TO AN OUTPUT VOLTAGE TRANSITION

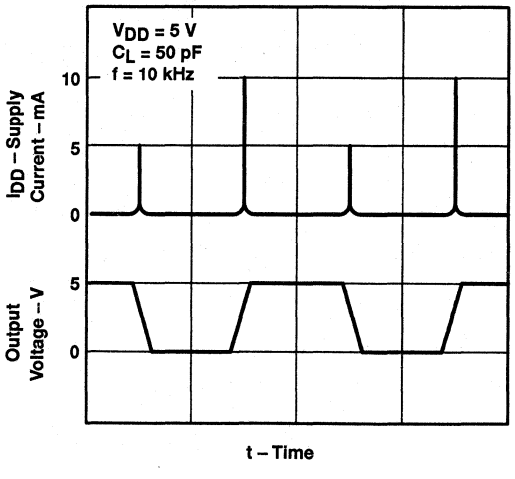


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

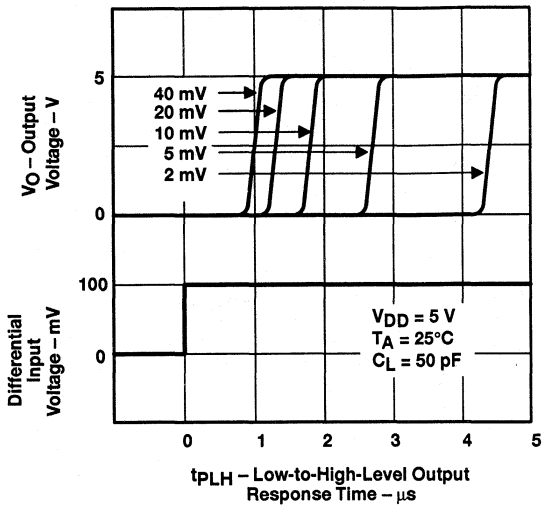


Figure 18

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

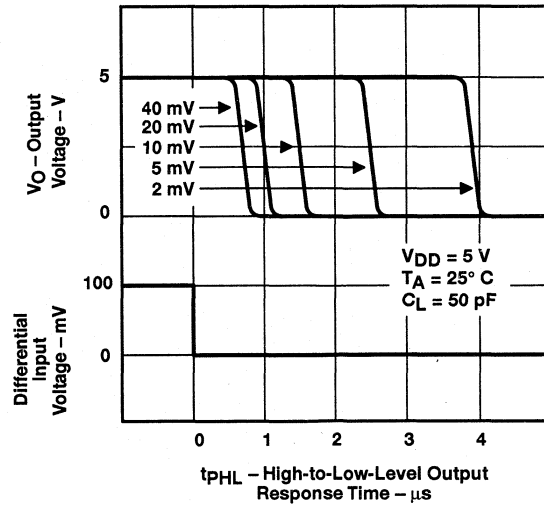


Figure 19

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

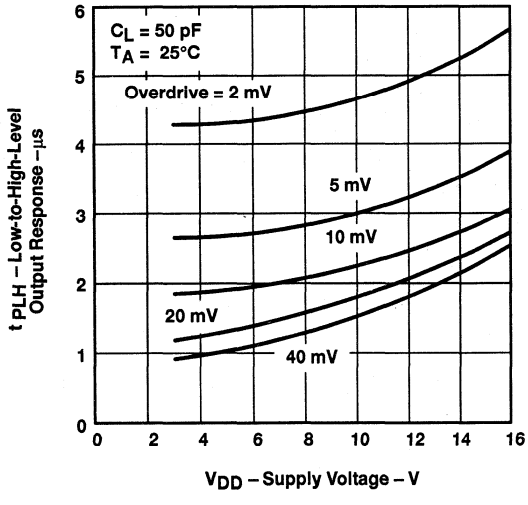


Figure 20

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

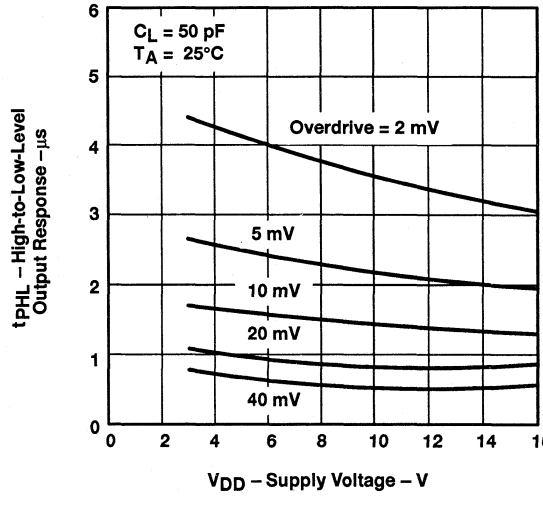


Figure 21

TYPICAL CHARACTERISTICS†

AVERAGE SUPPLY CURRENT (PER COMPARATOR) vs FREQUENCY

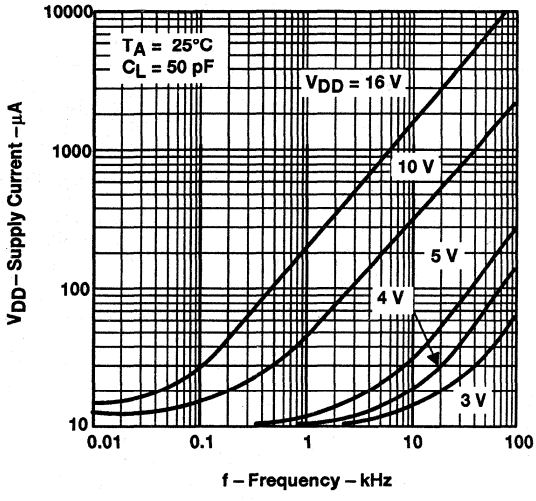


Figure 22

SUPPLY CURRENT vs SUPPLY VOLTAGE

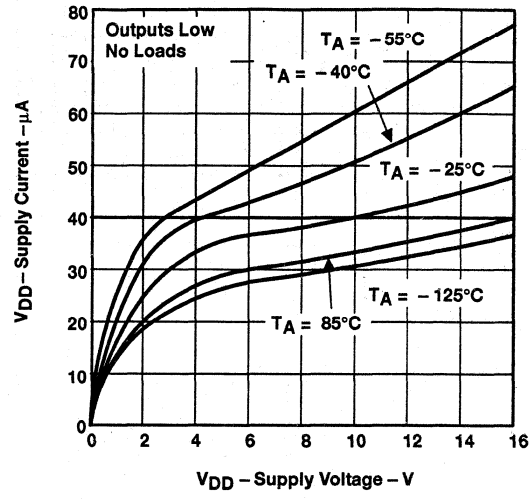


Figure 23

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

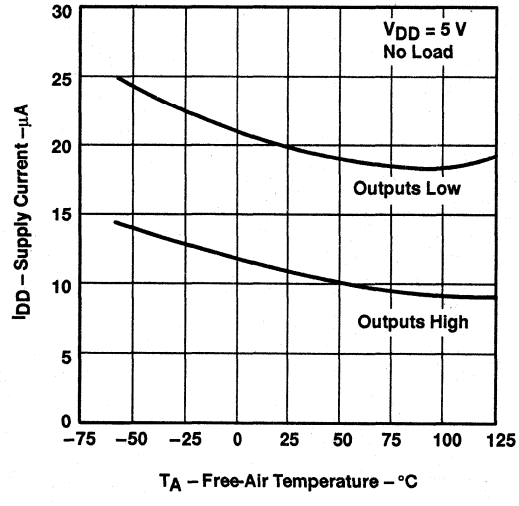


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

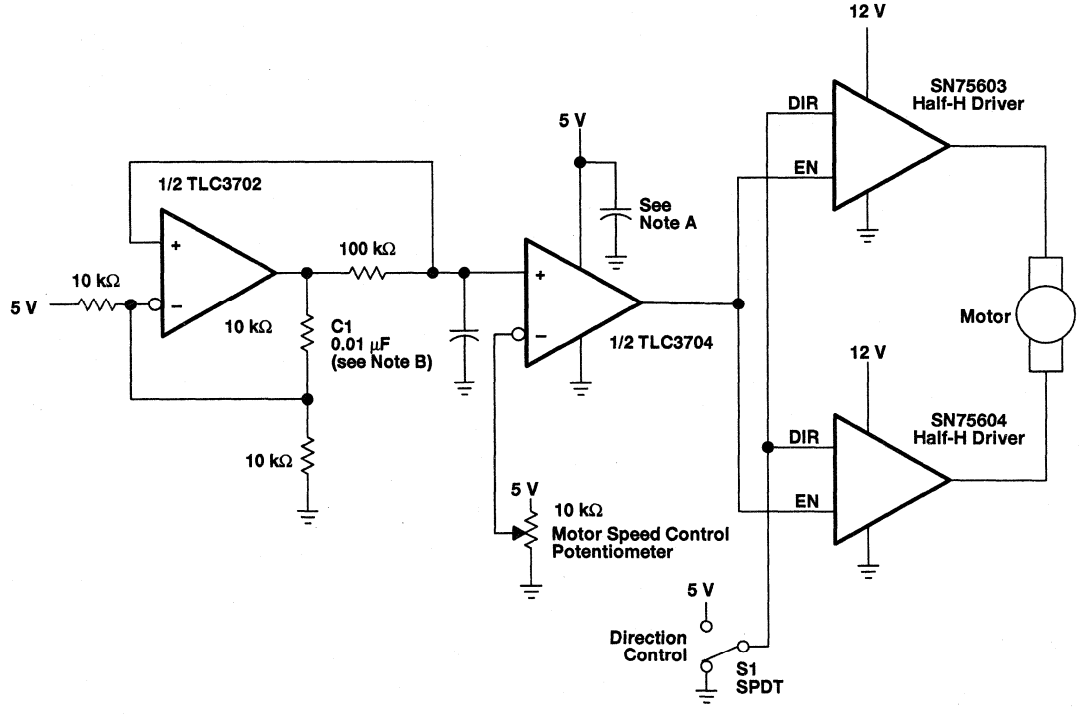
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between – 0.2 V and 4 V to ensure proper device operation.

To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) that is positioned as close to the device as possible.

The TLC3702 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

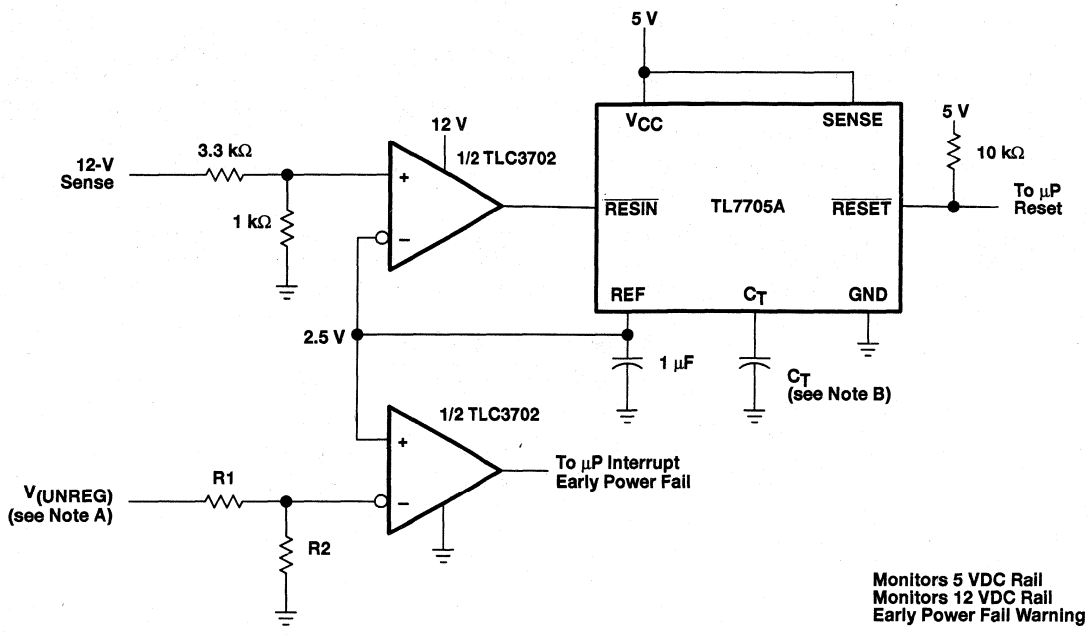
	FIGURE
Pulse-width-modulated motor speed controller	25
Enhanced supply supervisor	26
Two-phase nonoverlapping clock generator	27
Micropower switching regulator	28



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency.

Figure 25. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

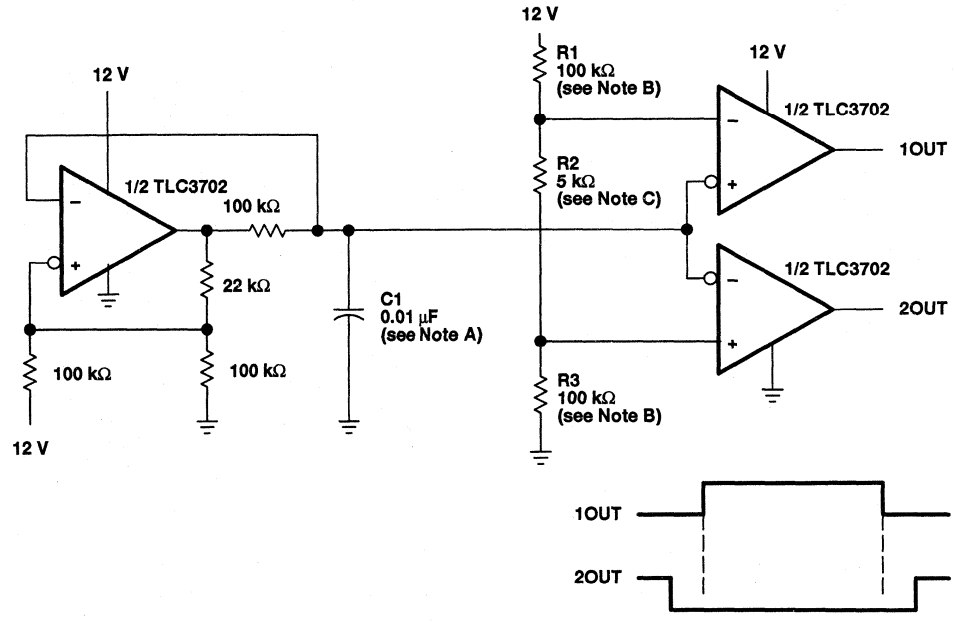


NOTES: A. $V_{(UNREG)} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 26. Enhanced Supply Supervisor

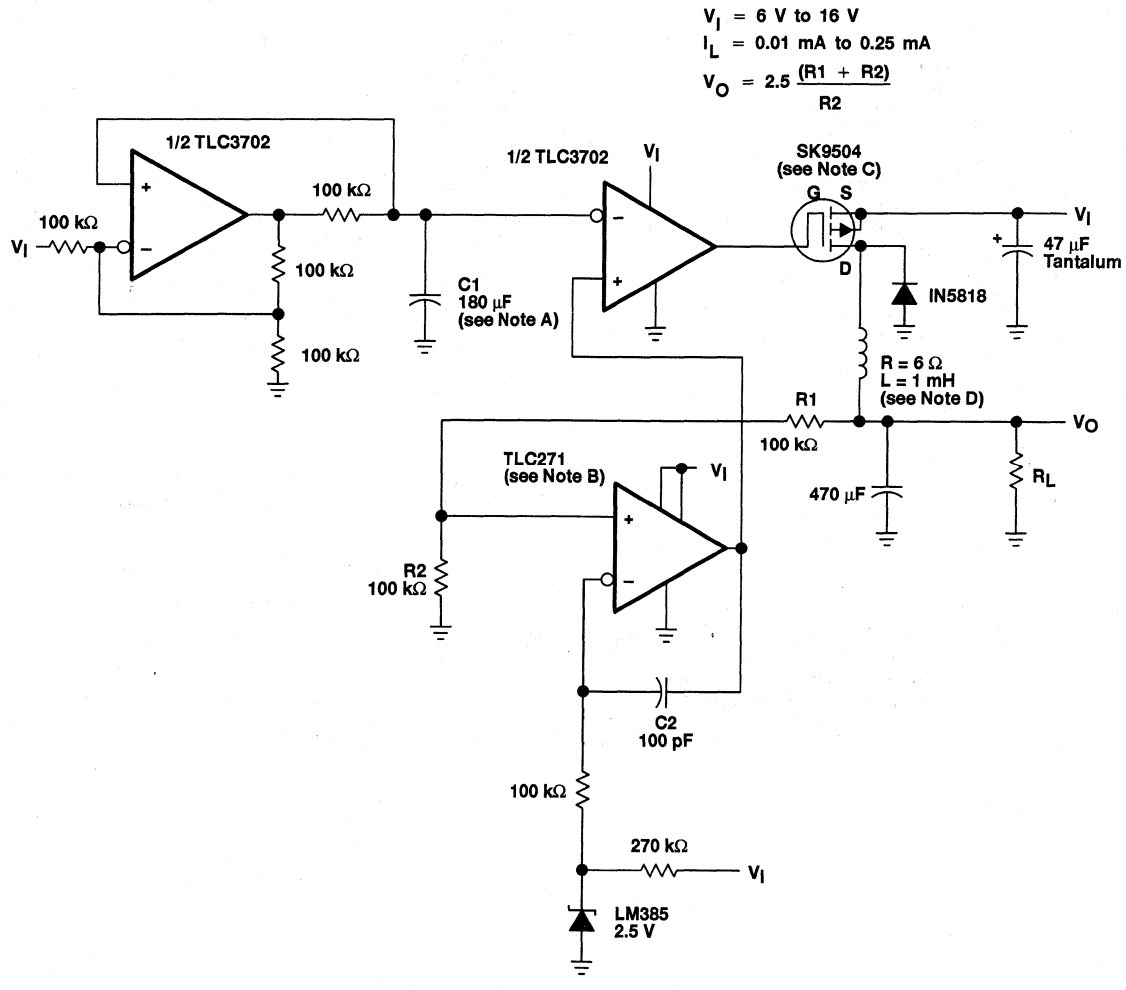
APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency where:
1/f = 1.85(100 kΩ)C1
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

Figure 27. Two-Phase Nonoverlapping Clock Generator

APPLICATION INFORMATION



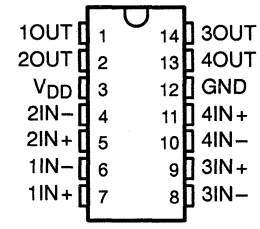
NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 – Tie pin 8 to pin 7 for low bias operation
C. SK9504 – VDS = 40 V
IDS = 1 A
D. To achieve microampere current drive, the inductance of the circuit must be increased.

Figure 28. Micropower Switching Regulator

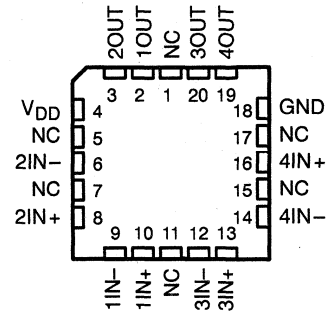
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, $I_O = \pm 8$ mA**
- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.7 μs Typ With 5-mV Overdrive**
- **Single Supply Operation . . . 3 V to 16 V**
  TLC3704M . . . 4 V to 16 V
- **On-Chip ESD Protection**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



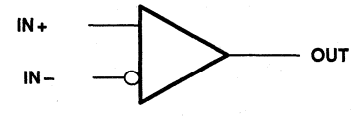
NC – No internal connection

description

The TLC3704 consists of four independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use 1/20th the power for similar response times. The push-pull CMOS output stage drives capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



The TLC3704C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3704I is characterized for operation over the extended industrial temperature range of – 40°C to 85°C. The TLC3704M is characterized for operation over the full military temperature range of – 55°C to 125°C. The TLC3704Q is characterized for operation from – 40°C to 125°C.

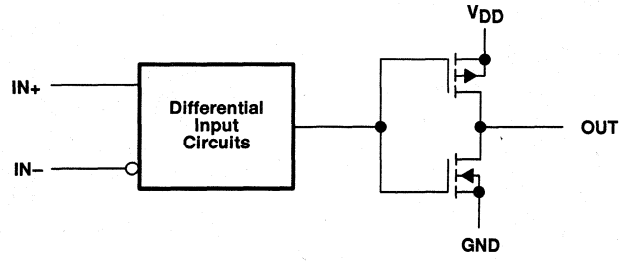
AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC3704CD	—	—	TLC3704CN
– 40°C to 85°C	5 mV	TLC3704ID	—	—	TLC3704IN
– 55°C to 125°C	5 mV	—	TLC3704MFK	TLC3704MJ	—
– 40°C to 125°C	5 mV	—	—	TLC3704QJ	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC3704CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... – 0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) ..... ± 18 V
Input voltage range, V_I ..... – 0.3 to V_{DD}
Output voltage range, V_O ..... – 0.3 to V_{DD}
Input current, I_I ..... ± 5 mA
Output current, I_O (each output) ..... ± 20 mA
Total supply current into V_{DD} ..... 40 mA
Total current out of GND ..... 60 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC3704C ..... 0 to 70°C
TLC3704I ..... – 40°C to 85°C
TLC3704M ..... – 55°C to 125°C
TLC3704Q ..... – 40°C to 125°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	N/A

recommended operating conditions

	TLC3704C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC3704C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min,	See Note 3	25°C		1.2	5	mV
				0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				70°C			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				0°C to 70°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C		84		dB
				70°C		84		
				0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				70°C		85		
				0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				70°C			375	
I_{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		35	80	μA
				0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3704I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC3704I			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, $V_{IC} = V_{ICR}$min, See Note 3	25°C		1.2	5	mV
			–40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			–40°C to 85°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			–40°C		83		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			–40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = –4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OH} = 4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		35	80	µA
			–40°C to 85°C			125	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3704M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC3704M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min,	See Note 3	25°C		1.2	5	mV
				–55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				–55°C to 125°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C		84		dB
				125°C		83		
				–55°C		82		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		85		
				–55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V,	I_{OH} = –4 mA	25°C	4.5	4.7		V
				125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OH} = 4 mA	25°C		210	300	mV
				125°C			500	
I_{DD}	Supply current (both comparators)	Outputs low,	No load	25°C		35	80	µA
				–55°C to 125°C			175	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3704Q			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD} − 1.5	V
High-level output current, I_{OH}			− 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	− 40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC3704Q			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min, See Note 3	25°C		1.2	5	mV
			−40°C to 125°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} − 1			V
			−40°C to 125°C	0 to V_{DD} − 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		83		
			−40°C		83		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			−40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OH} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		35	80	µA
			−40°C to 125°C			175	

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC3704C, TLC3704I TLC3704M, TLC3704Q			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4-V step at IN+			1.1		
t_{PHL}	Propagation delay time, high-to-low-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4-V step at IN+			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

† Simultaneous switching of inputs causes degradation in output response.

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. Further questions should be directed to the nearest TI field sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

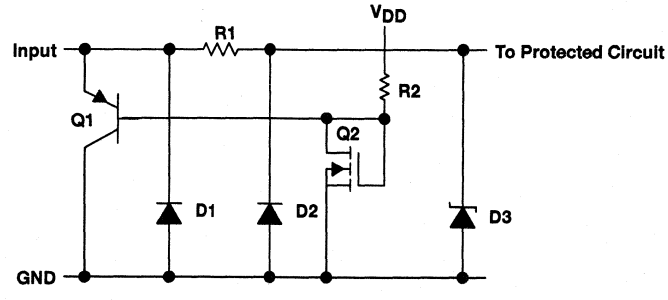


Figure 1. LinCMOS™ ESD-Protection Schematic

Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

PRINCIPLES OF OPERATION

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 2 and 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limit the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

circuit-design considerations (continued)

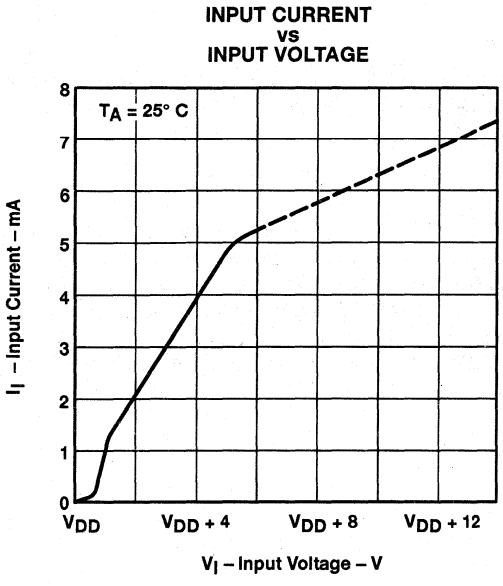


Figure 2

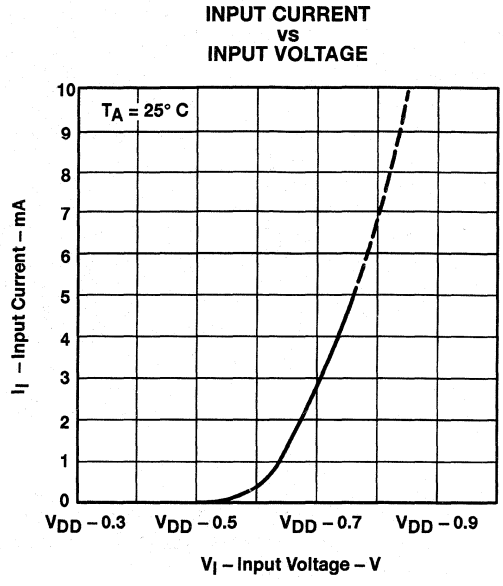
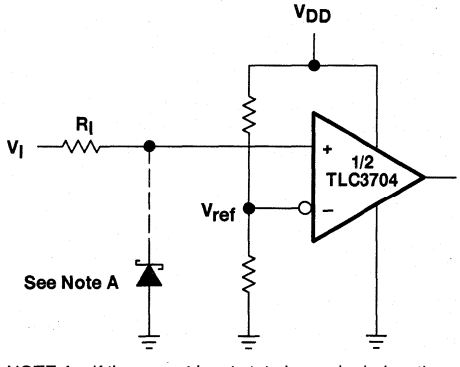


Figure 3



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

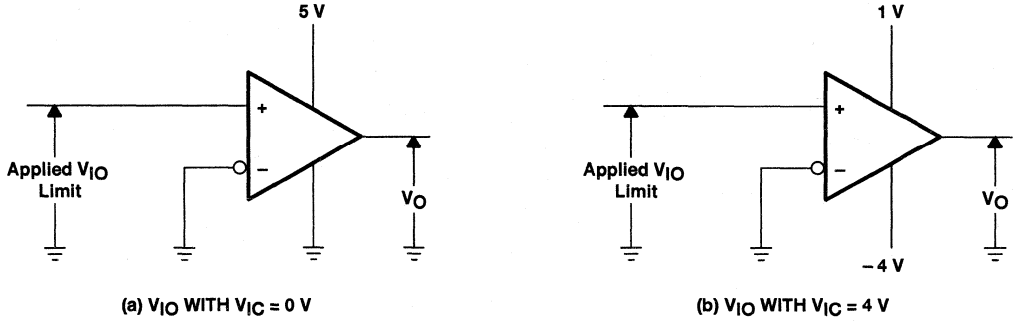
Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

PARAMETER MEASUREMENT INFORMATION

The TLC3704 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 5(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides an increase in the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

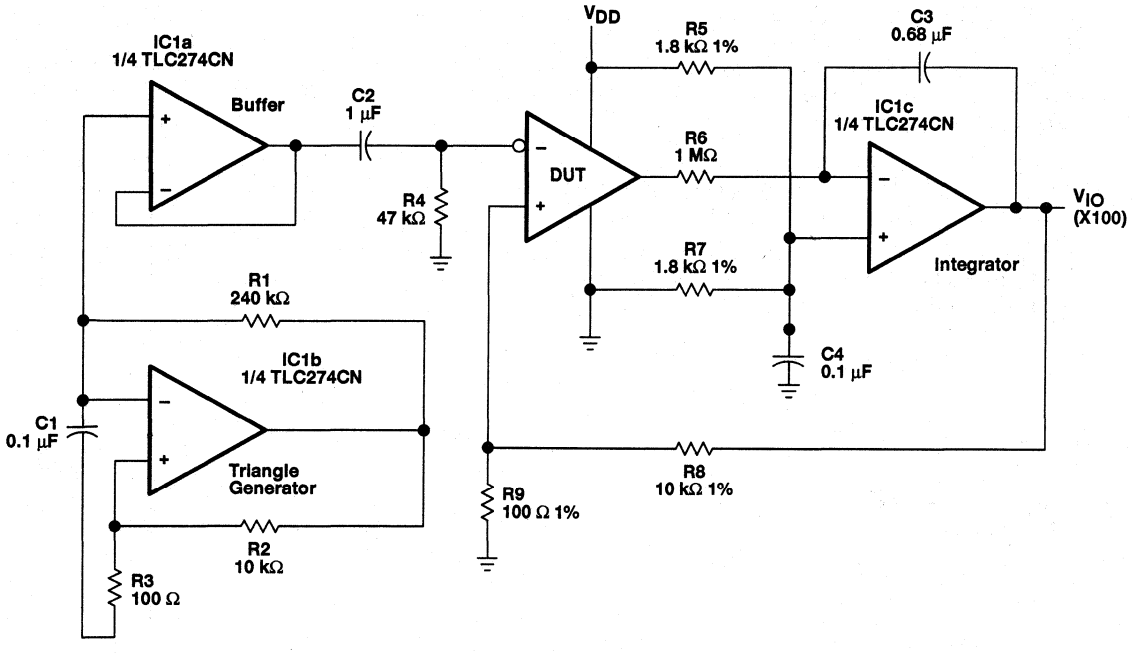
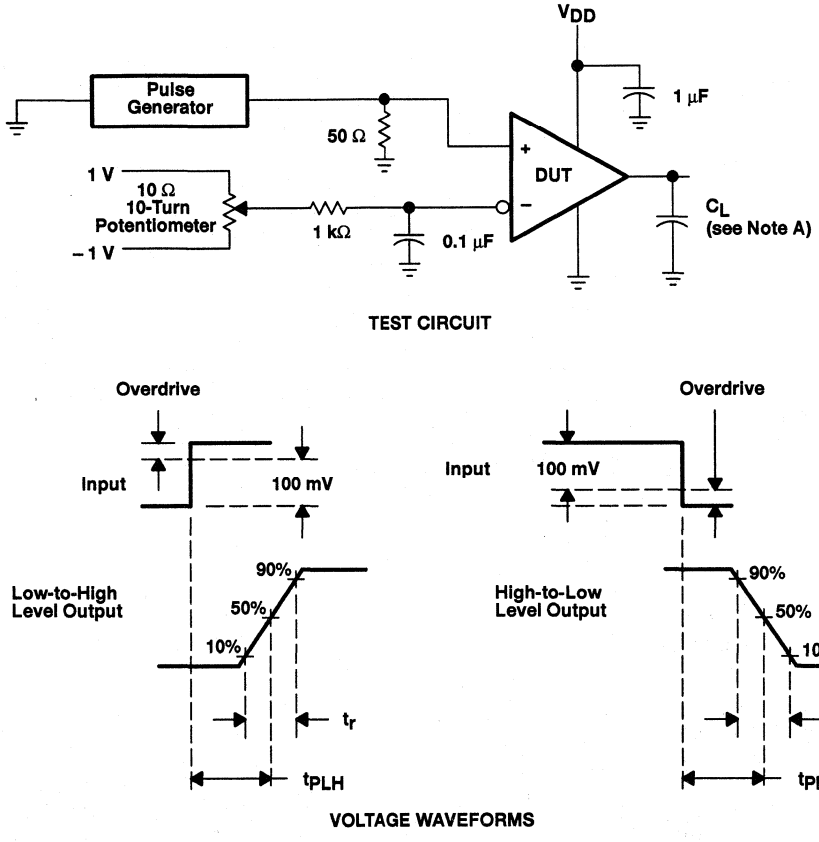


Figure 6. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 7, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	8
I_{IB}	Input bias current	vs Free-air temperature	9
CMRR	Common-mode rejection ratio	vs Free-air temperature	10
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	11
V_{OH}	High-level output current	vs Free-air temperature vs High-level output current	12 13
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	14 15
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	Supply current response	vs Time	17
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I_{DD}	Supply current	vs Frequency vs Supply voltage vs Free-air temperature	22 23 24

DISTRIBUTION OF INPUT OFFSET VOLTAGE

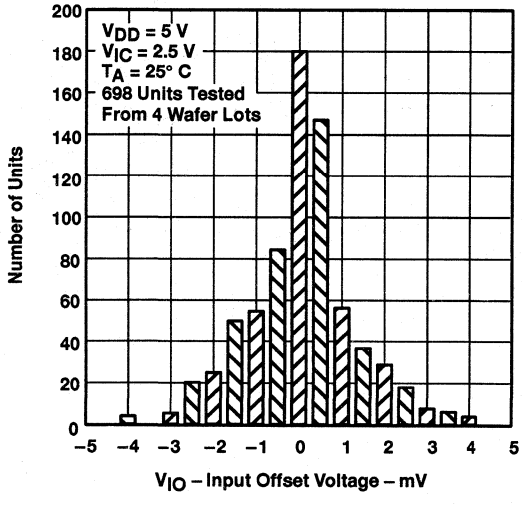


Figure 8

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

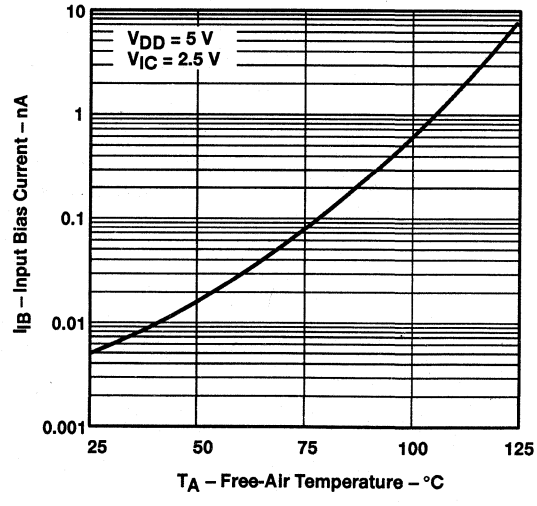


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

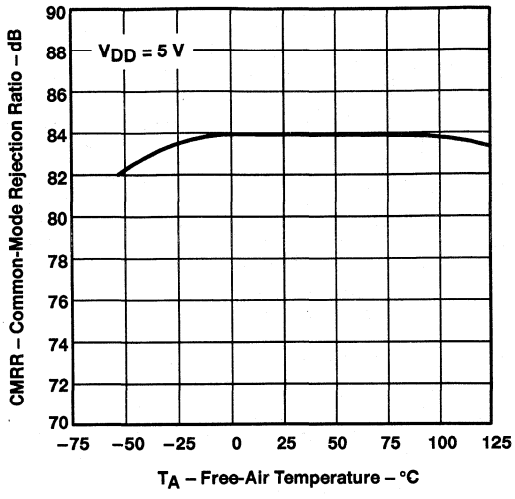


Figure 10

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

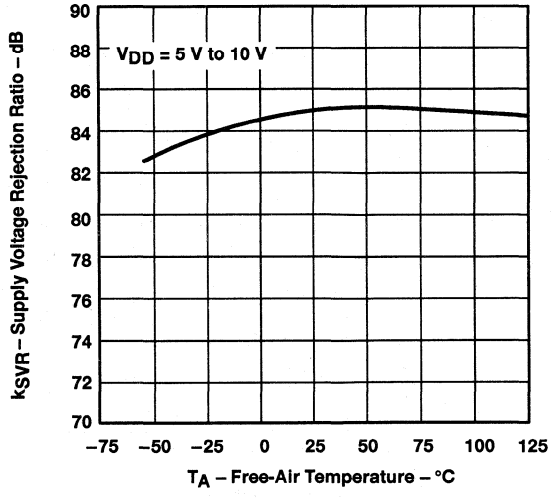


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

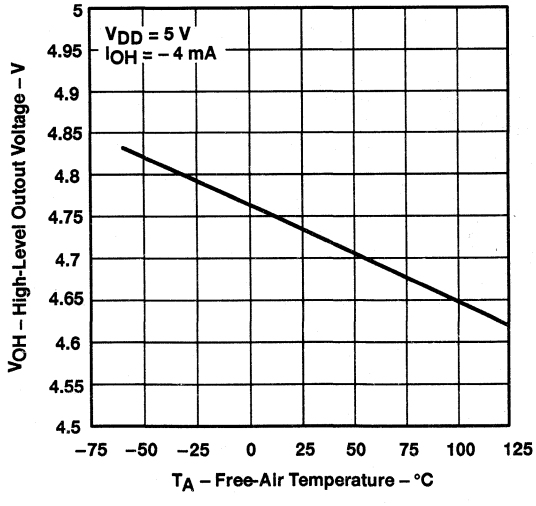


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

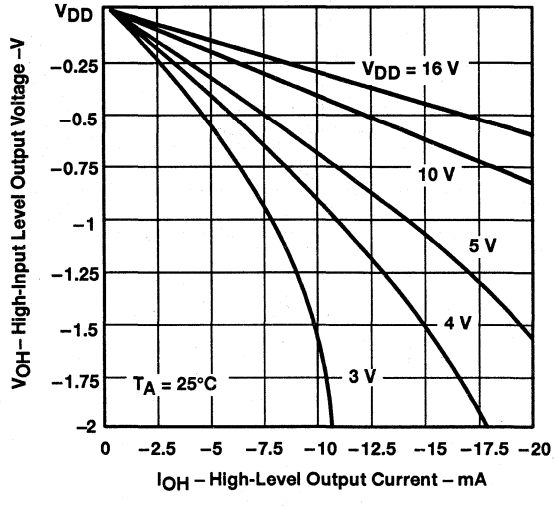


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

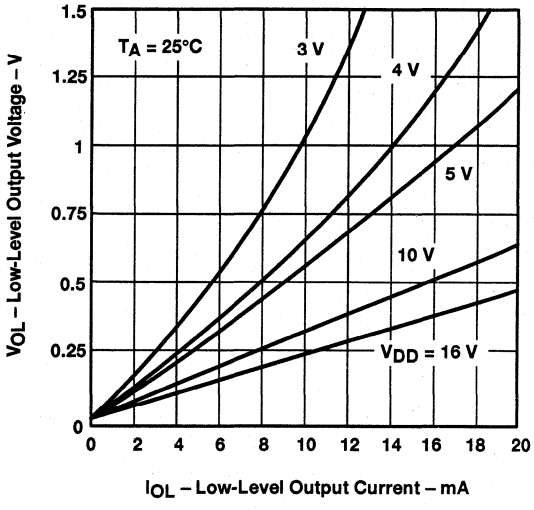


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

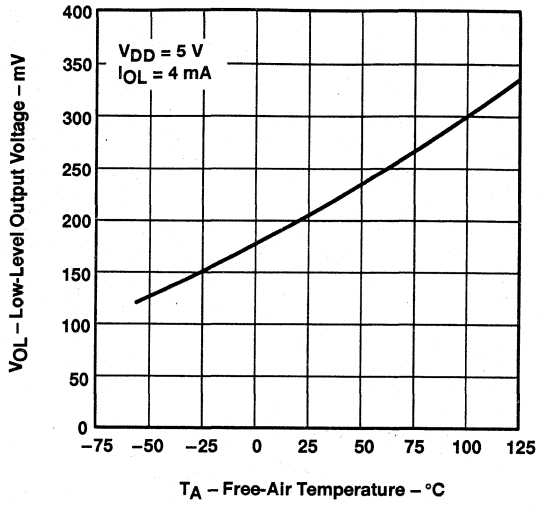


Figure 15

OUTPUT TRANSITION TIME
vs
LOAD CAPACITANCE

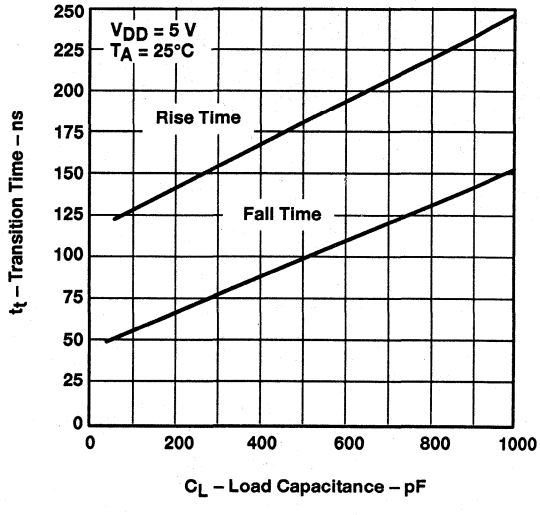


Figure 16

SUPPLY CURRENT RESPONSE
TO AN OUTPUT VOLTAGE TRANSITION

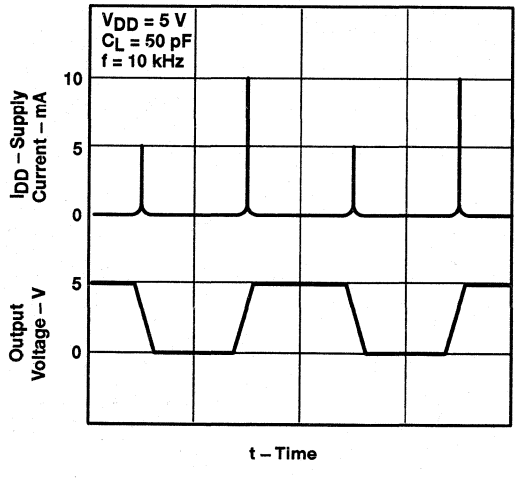


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

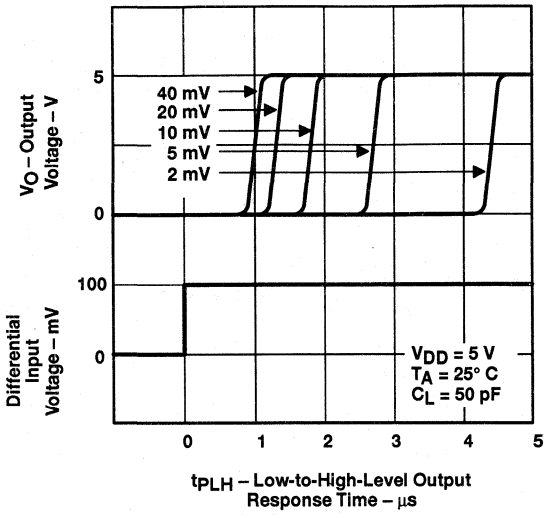


Figure 18

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

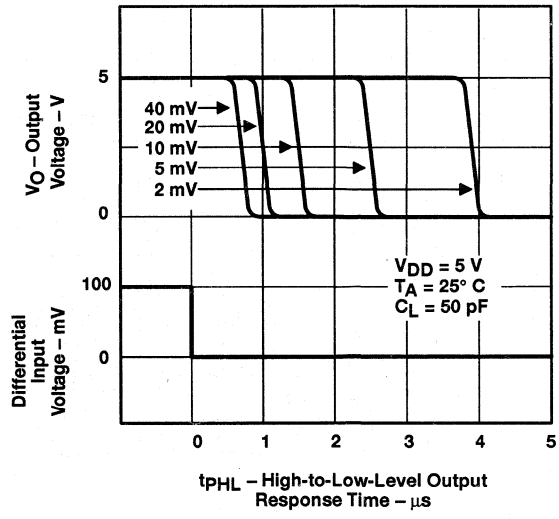


Figure 19

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

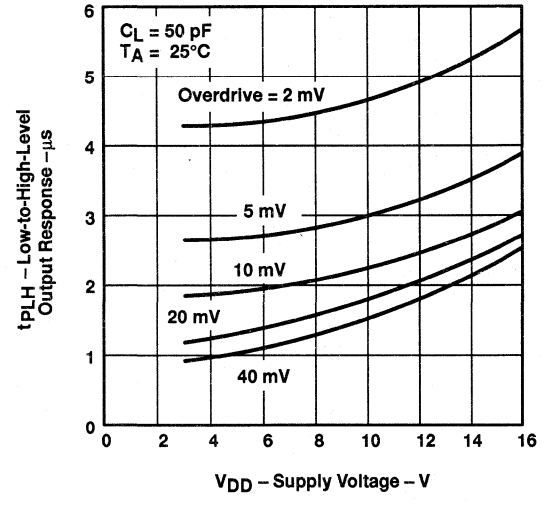


Figure 20

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

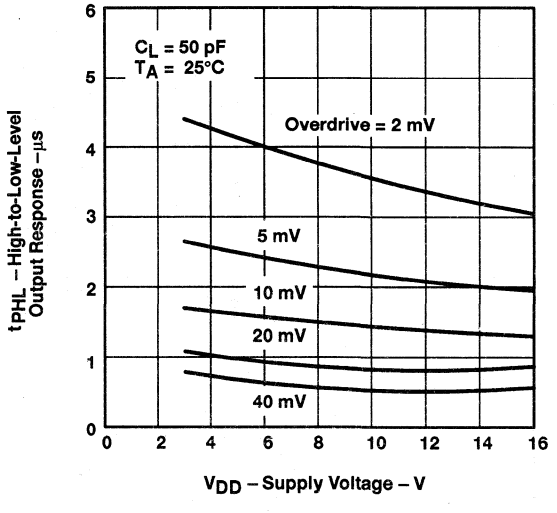


Figure 21

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT (PER COMPARATOR) vs FREQUENCY

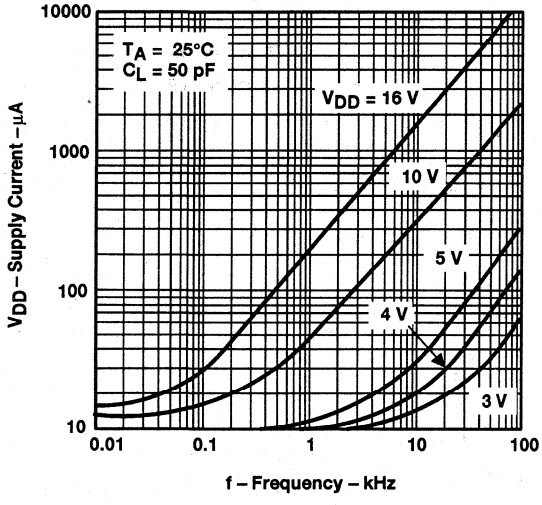


Figure 22

SUPPLY CURRENT vs SUPPLY VOLTAGE

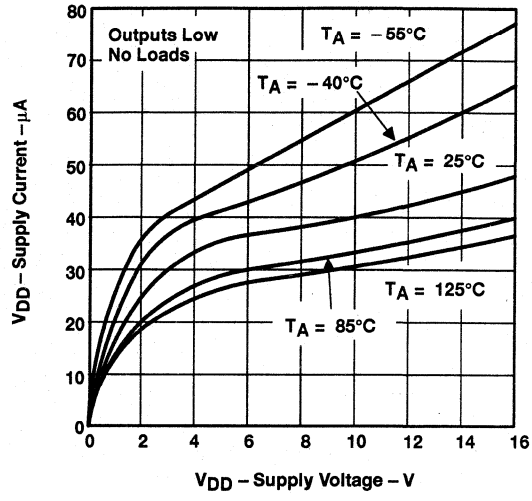


Figure 23

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

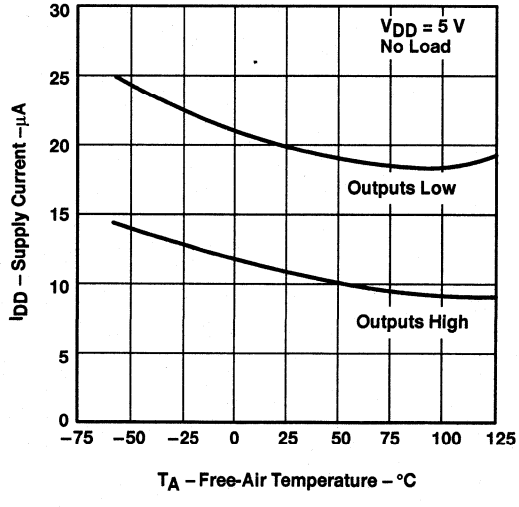


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

APPLICATION INFORMATION

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between –0.2 V and 4 V to ensure proper device operation. To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) that is positioned as close to the device as possible.

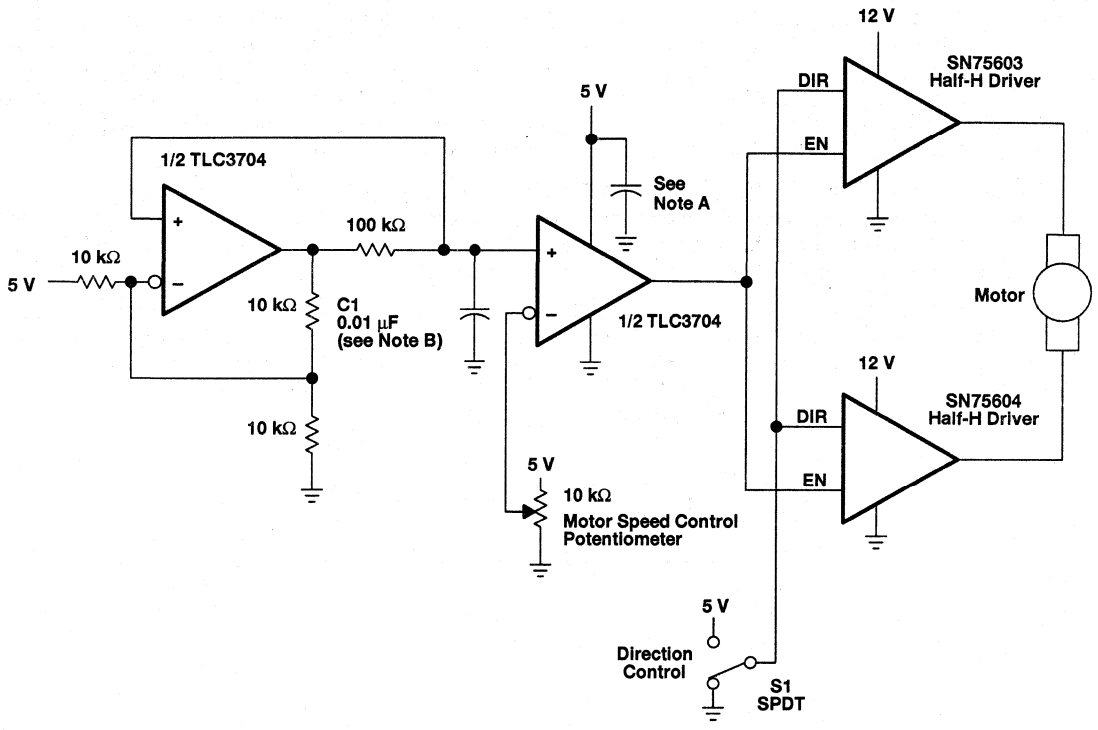
Output and supply current limitations should be watched carefully since the TLC3704 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground can only be an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC3704 has internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

	FIGURE
Pulse-width-modulated motor speed controller	25
Enhanced supply supervisor	26
Two-phase nonoverlapping clock generator	27
Micropower switching regulator	28

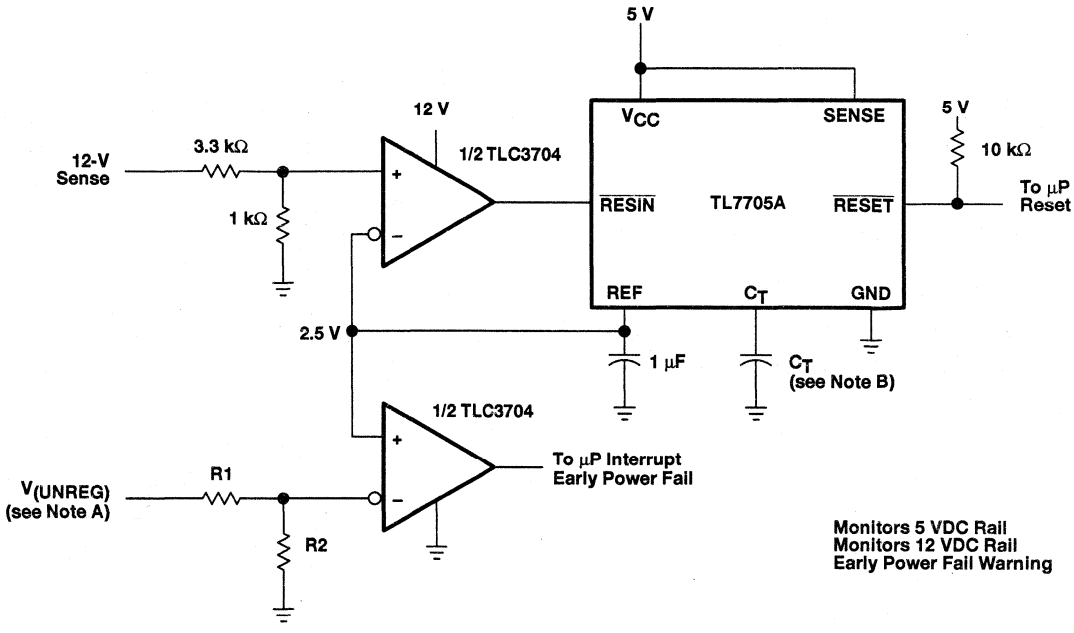
APPLICATION INFORMATION



NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency

Figure 25. Pulse-Width-Modulated Motor Speed Controller

APPLICATION INFORMATION

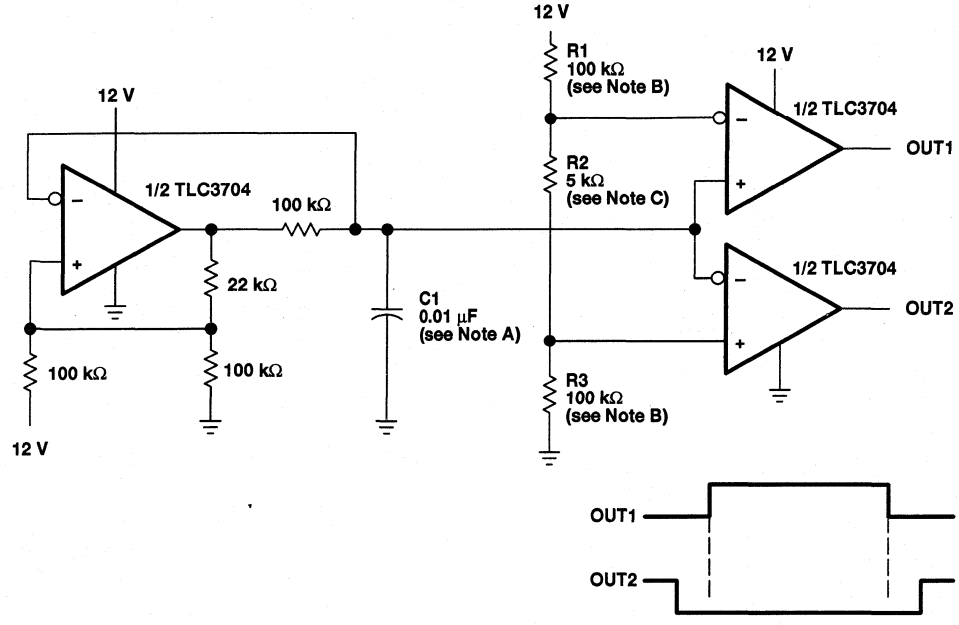


NOTES: A. $V_{(UNREG)} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of C_T determines the time delay of reset.

Figure 26. Enhanced Supply Supervisor

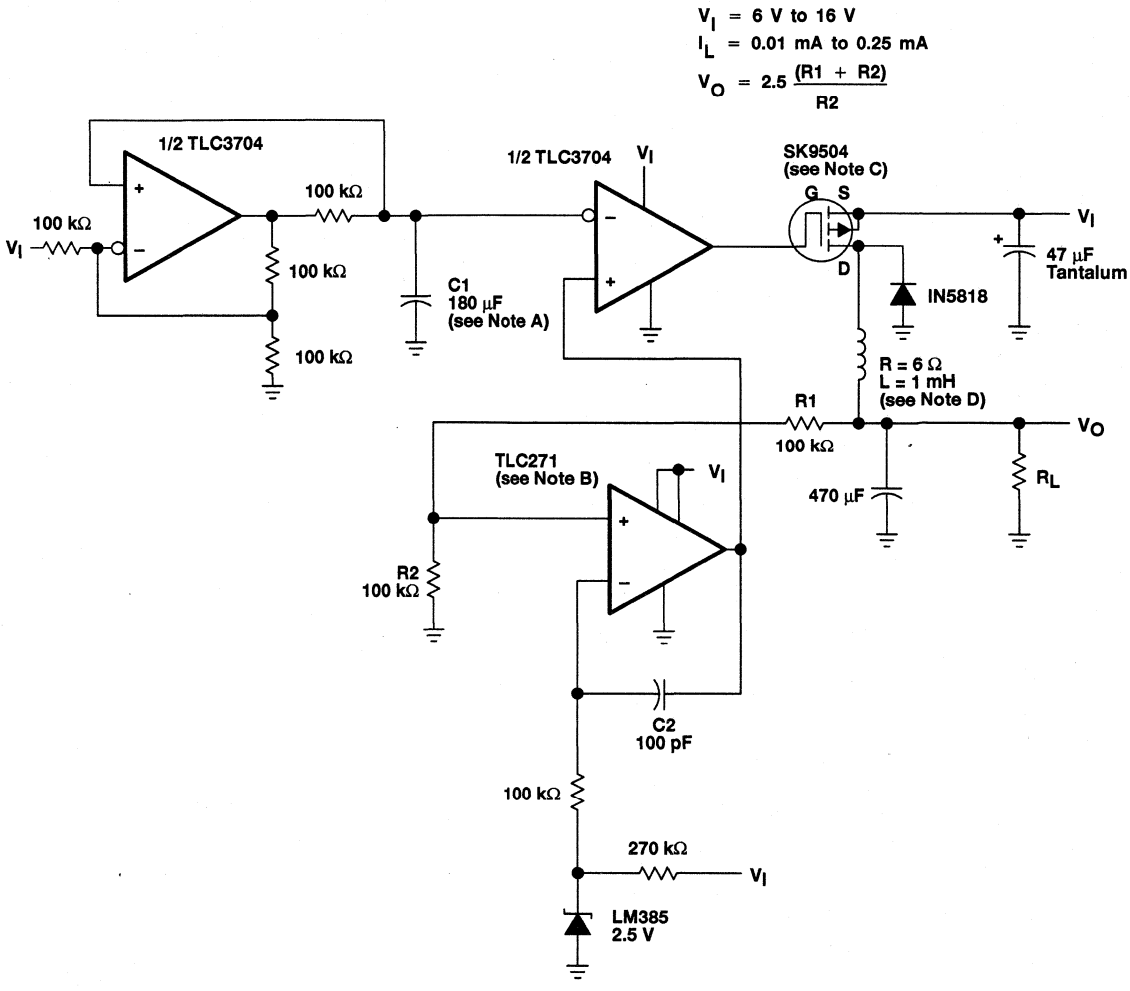
APPLICATION INFORMATION



NOTES: A. Adjust C1 for a change in oscillator frequency where:
$1/f = 1.85(100\ k\Omega)C1$
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

Figure 27. Two-Phase Nonoverlapping Clock Generator

APPLICATION INFORMATION



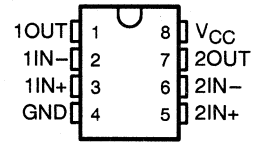
NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 – Tie pin 8 to pin 7 for low bias operation
C. SK9504 – VDS = 40 V
IDS = 1 Awill
D. To achieve microampere current drive, the inductance of the circuit must be increased.

Figure 28. Micropower Switching Regulator

SLCS121A – AUGUST 1993 – REVISED APRIL 1994

- **Low-Voltage and Single-Supply Operation**
  V_{CC} = 2 V to 7 V
- **Common-Mode Voltage Range Includes Ground**
- **Fast Response Time**
  450 ns Typ (TLV2393)
- **Low Supply Current**
  0.16 mA Typ (TLV1393)
- **Fully Specified at 3-V and 5-V Supply Voltages**

D, P, OR PW PACKAGE
(TOP VIEW)



description

The TLV1393 and the TLV2393 are dual differential comparators built using a new Texas Instruments low-voltage, high-speed bipolar process. These devices have been specifically developed for low-voltage, single-supply applications. Their enhanced performance makes them excellent replacements for the LM393 in today's improved 3-V and 5-V system designs.

The TLV1393, with its typical supply current of only 0.16 mA, is ideal for low-power systems. Response time has also been improved to 0.7 µs. For higher-speed applications, the TLV2393 features excellent ac performance with a response time of just 0.45 µs, three times that of the LM393.

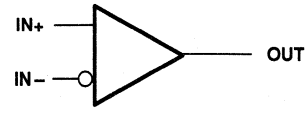
Package availability for these devices includes the TSSOP (thin-shrink small-outline package). With a maximum thickness of 1.1 mm and a package area that is 25% smaller than the standard surface-mount package, the TSSOP is ideal for high-density circuits, particularly in hand-held and portable equipment.

AVAILABLE OPTIONS

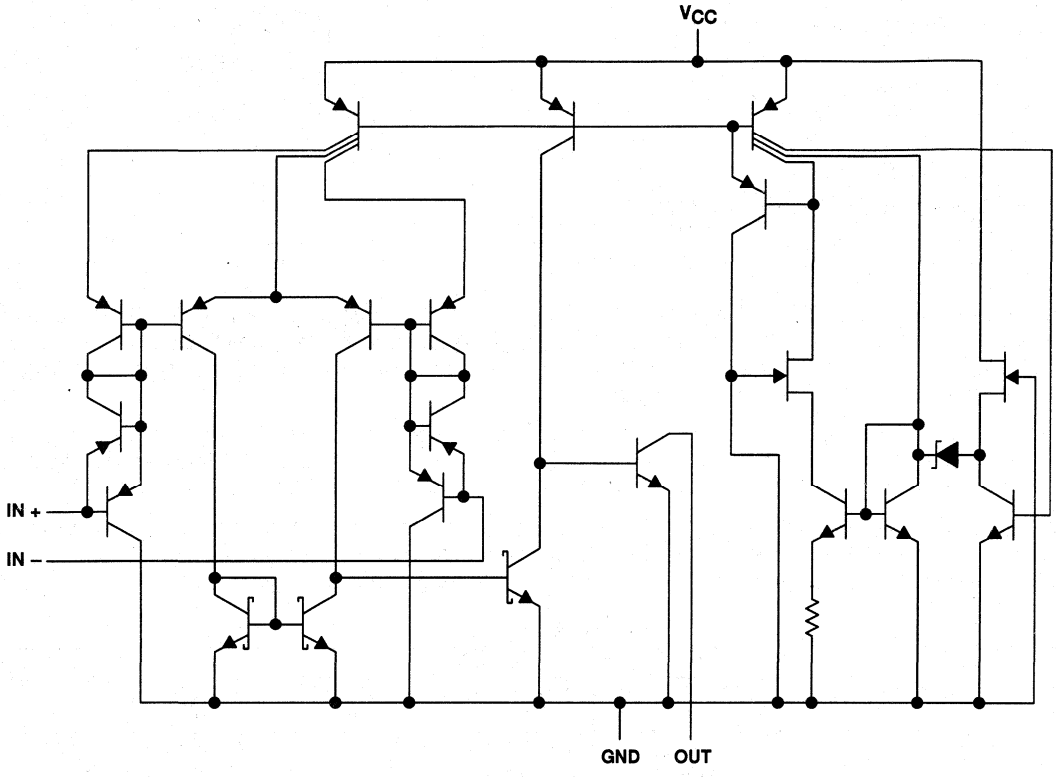
T_A	PACKAGED DEVICES					CHIP FORM (Y)
	SUPPLY CURRENT (TYP)	RESPONSE TIME (TYP)	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)†	
–40°C to 105°C	0.16 mA	0.7 µs	TLV1393ID	TLV1393IP	TLV1393IPWLE	TLV1393Y
	1.1 mA	0.45 µs	TLV2393ID	TLV2393IP	TLV2393IPWLE	TLV2393Y

† The PW packages are only available left-ended taped and reeled (e.g., TLV1393IPWLE).

symbol (each comparator)

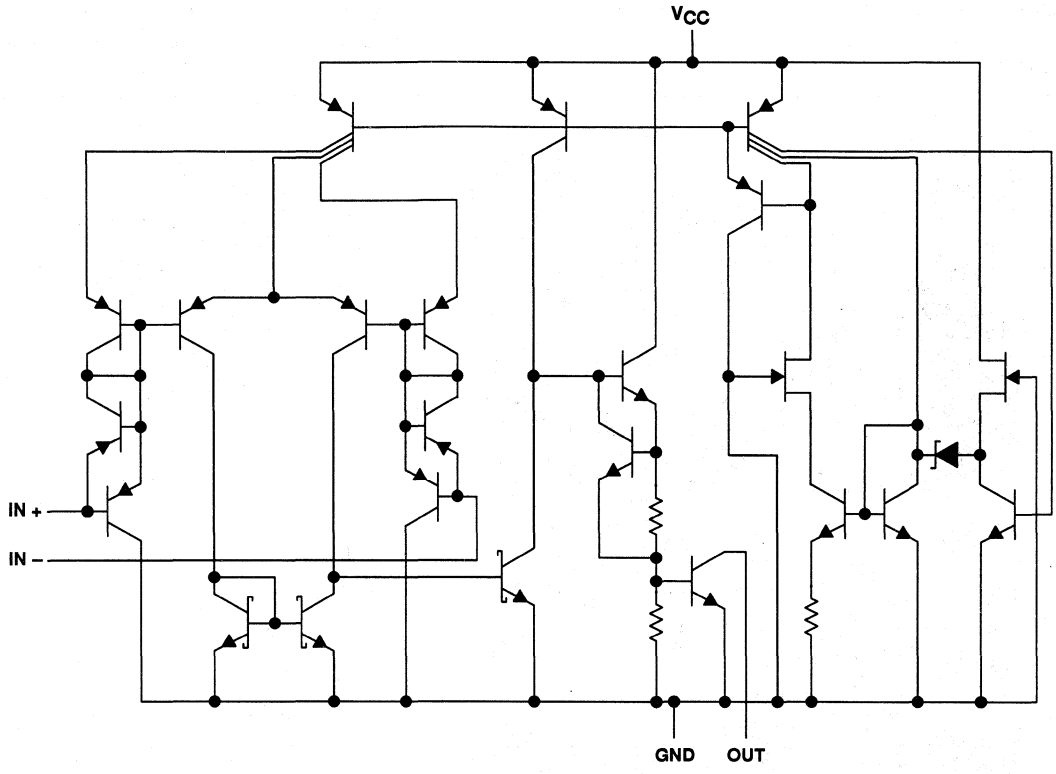


TLV1393, TLV1393Y equivalent schematic (each comparator)



COMPONENT COUNT	
Transistors	44
Resistors	1
Diodes	7
Epi-FET	2

TLV2393, TLV2393Y equivalent schematic (each comparator)

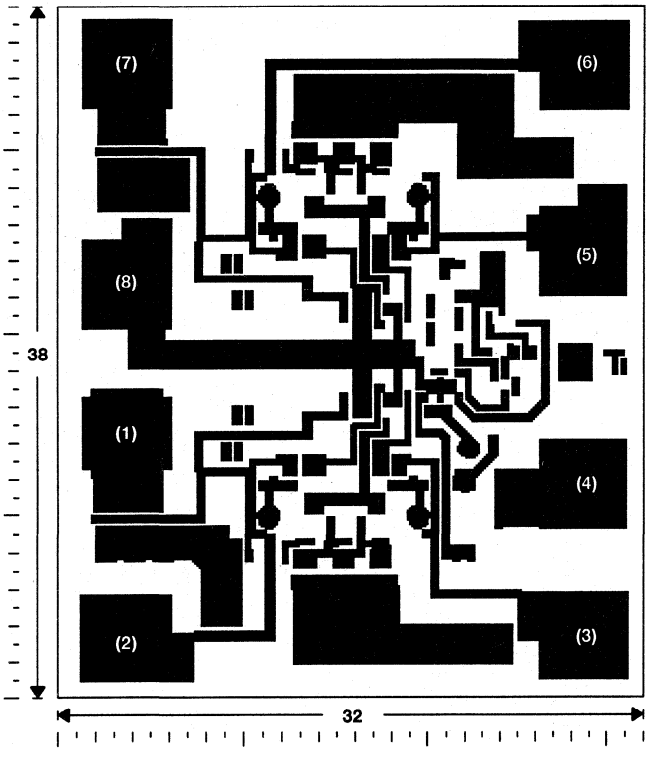


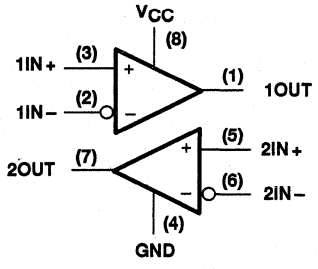
COMPONENT COUNT	
Transistors	44
Resistors	1
Diodes	7
Epi-FET	2

TLV1393Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV1393. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 13 TYPICAL

BONDING PADS: 3.54 × 3.54 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

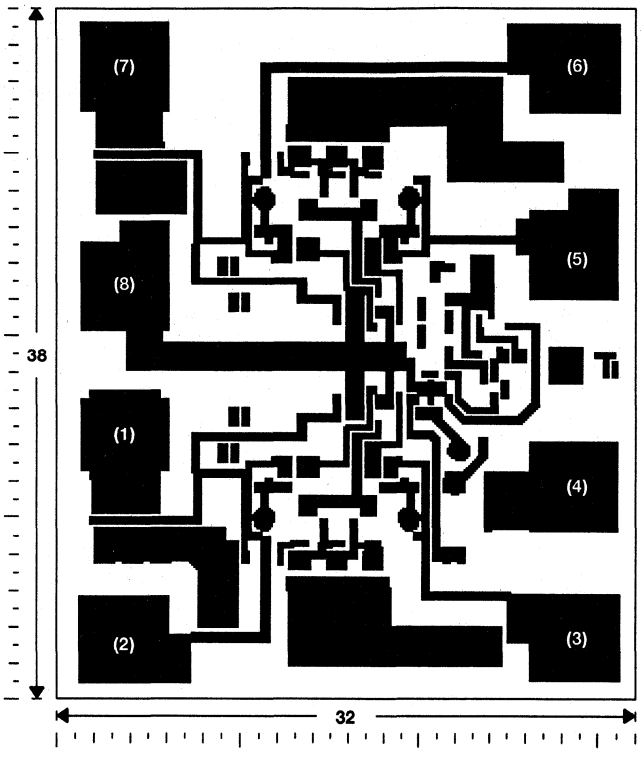
ALL DIMENSIONS ARE IN MILS.

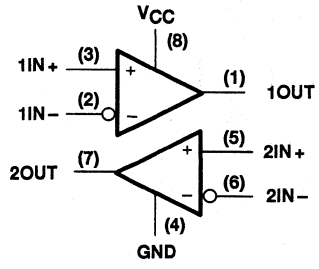
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TLV2393Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2393. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 3.6 × 3.6 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Differential input voltage, V_{ID} (see Note 2) ..... 7 V
Input voltage, V_I (any input) ..... 7 V
Output voltage, V_O ..... 7 V
Output current, I_O (each output) ..... 20 mA
Duration of short-circuit current to GND (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 105°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network GND.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. Short circuits from the outputs to V_{CC} can cause excessive heating and eventual destruction of the chip.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	2	7	V
Operating free-air temperature, T_A	−40	105	°C

electrical characteristics, V_{CC} = 3 V

PARAMETER		TEST CONDITIONS	T_A†	TLV1393			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min	25°C		1.5	5	mV
			Full range		120	9	
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
			Full range	0 to V_{CC} – 2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 500 µA	Full range		120	300	mV
I_{IO}	Input offset current	V_O = 1.4 V	25°C		5	50	nA
			Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		–40	–250	nA
			Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V, V_{OH} = 5 V	Full range			100	
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	25°C	500			µA
I_{CCH}	High-level supply current	V_O = V_{OH}	25°C		160	250	µA
			Full range			300	
I_{CCL}	Low-level supply current	V_O = V_{OL}	25°C		160	250	
			Full range			300	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV1393			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.7		µs

electrical characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV1393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range			9	
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{CC}-1.5$	0 to $V_{CC}-1.2$		V
				Full range	0 to $V_{CC}-2$			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 500 µA	Full range		120	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–40	–250	nA
				Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	600			µA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		200	300	µA
				Full range			350	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		200	300	
				Full range			350	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV1393			UNIT
			MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 kΩ		0.65		µs
	TTL-level input step,	R_L connected to 5 V through 5.1 kΩ		0.18		

electrical characteristics, V_{CC} = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV1393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–40	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	500			µA
I_{CCH}	High-level supply current	V_O = V_{OH}		160	250	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		160	250	

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV1393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.7		µs

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV1393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–40	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	600			µA
I_{CCH}	High-level supply current	V_O = V_{OH}		200	300	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		200	300	

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV1393Y			UNIT
			MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 kΩ		0.65		µs
	TTL-level input step,	R_L connected to 5 V through 5.1 kΩ		0.18		

electrical characteristics, V_{CC} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range			9	
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{CC}-1.5$	0 to $V_{CC}-1.2$		V
				Full range	0 to $V_{CC}-2$			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 1 mA	25°C		80	300	mV
		V_{ID} = –1 V,	I_{OL} = 4 mA	Full range		250	700	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–100	–250	nA
				Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	4			mA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		450	600	µA
				Full range			700	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		1.1	1.3	mA
				Full range			1.4	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2393			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.45	1	µs

electrical characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2393			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V,	$V_{IC} = V_{ICR}$min	25°C		1.5	5	mV
				Full range			9	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
				Full range	0 to V_{CC} – 2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 1 mA	25°C		70	300	mV
		V_{ID} = –1 V,	I_{OL} = 4 mA	Full range		200	700	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–100	–250	nA
				Full range			–400	
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 3 V	25°C		0.1		nA
		V_{ID} = 1 V,	V_{OH} = 5 V	Full range			100	
I_{OL}	Low-level output current	V_{ID} = –1 V,	V_{OL} = 1.5 V	25°C	6			mA
I_{CCH}	High-level supply current	$V_O = V_{OH}$		25°C		550	700	µA
				Full range			800	
I_{CCL}	Low-level supply current	$V_O = V_{OL}$		25°C		1.2	1.5	mA
				Full range			1.6	

† Full range is –40°C to 105°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2393			UNIT
			MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive,	R_L connected to 5 V through 5.1 kΩ		0.4	0.8	µs
	TTL-level input step,	R_L connected to 5 V through 5.1 kΩ		0.15	0.3	

electrical characteristics, V_{CC} = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 1 mA		80	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–100	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	4			mA
I_{CCH}	High-level supply current	V_O = V_{OH}		450	600	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		1.1	1.3	mA

switching characteristics, V_{CC} = 3 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.45	1	µs

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLV2393Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = V_{ICR}min		1.5	5	mV
V_{ICR}	Common-mode input voltage range		0 to V_{CC} – 1.5	0 to V_{CC} – 1.2		V
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OL} = 1 mA		70	300	mV
I_{IO}	Input offset current	V_O = 1.4 V		5	50	nA
I_{IB}	Input bias current	V_O = 1.4 V		–100	–250	nA
I_{OH}	High-level output current	V_{ID} = 1 V, V_{OH} = 3 V		0.1		nA
I_{OL}	Low-level output current	V_{ID} = –1 V, V_{OL} = 1.5 V	6			mA
I_{CCH}	High-level supply current	V_O = V_{OH}		550	700	µA
I_{CCL}	Low-level supply current	V_O = V_{OL}		1.2	1.5	mA

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	TLV2393Y			UNIT
		MIN	TYP	MAX	
Response time	100-mV input step with 5-mV overdrive, R_L connected to 5 V through 5.1 kΩ		0.4	0.8	µs
	TTL-level input step, R_L connected to 5 V through 5.1 kΩ		0.15	0.3	

TYPICAL CHARACTERISTICS

TLV1393 LOW-TO HIGH-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

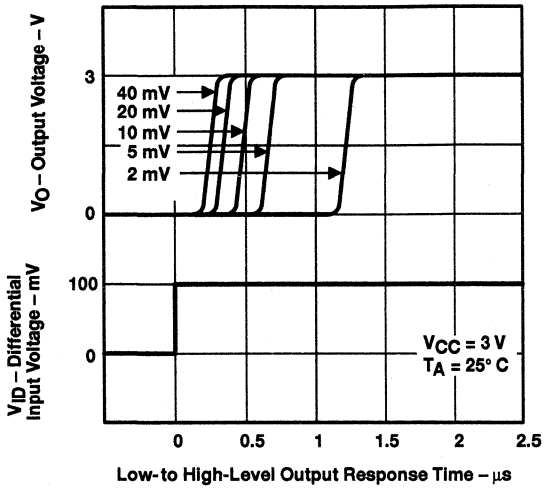


Figure 1

TLV1393 HIGH-TO LOW-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

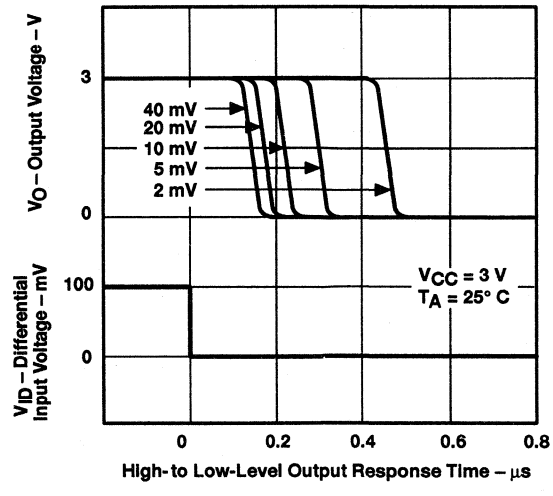


Figure 2

TLV1393 LOW-TO HIGH-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

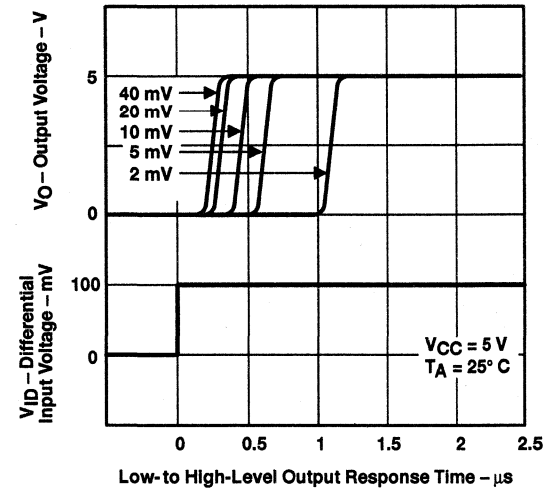


Figure 3

TLV1393 HIGH-TO LOW-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

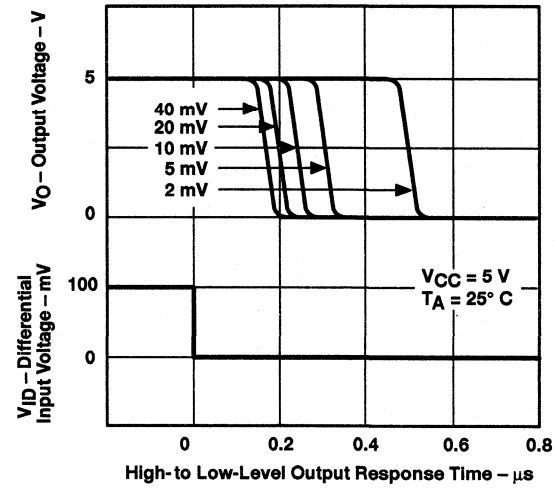


Figure 4

TYPICAL CHARACTERISTICS

TLV2393 LOW-TO HIGH-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

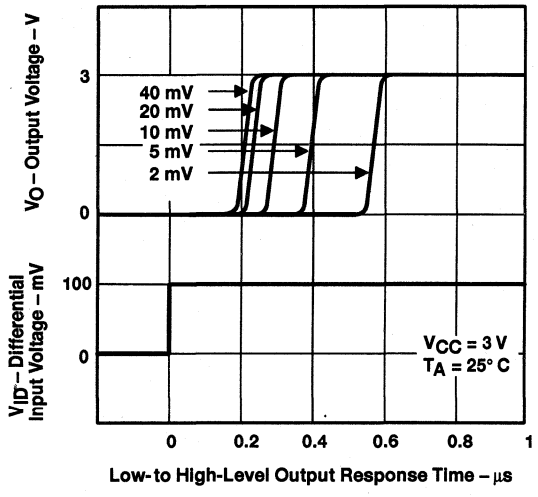


Figure 5

TLV2393 HIGH-TO LOW-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

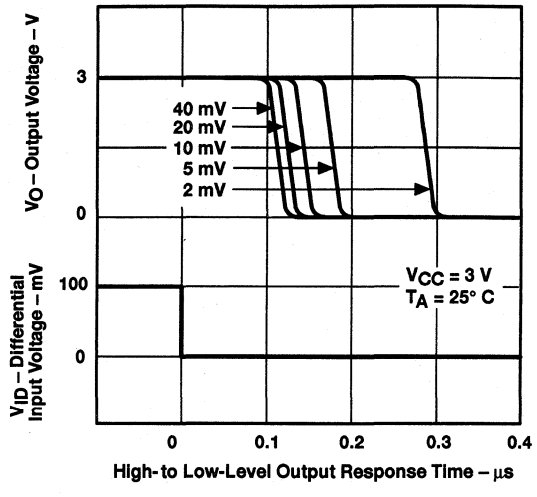


Figure 6

TLV2393 LOW-TO HIGH-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

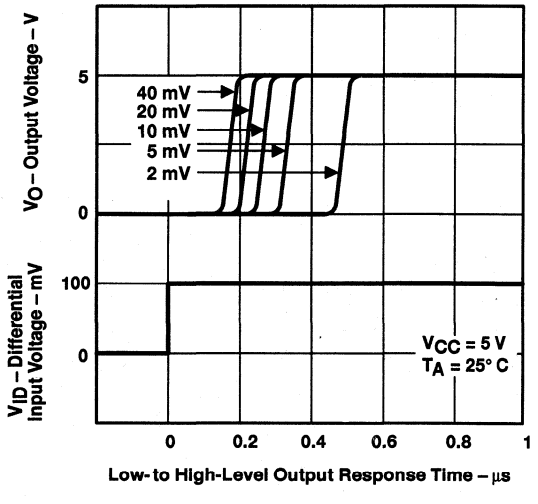


Figure 7

TLV2393 HIGH-TO LOW-LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES

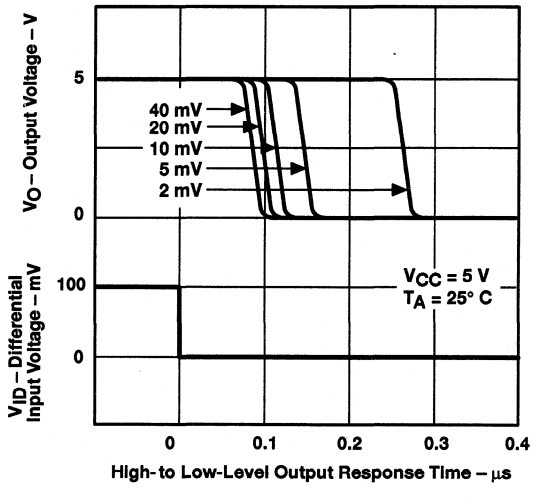
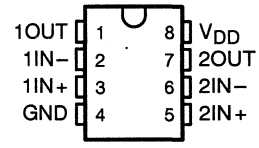


Figure 8

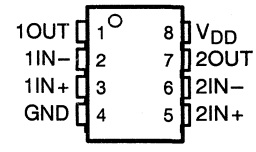
SLCS011 – MAY 1992

- **Wide Range of Supply Voltages 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Very-Low Supply-Current Drain 120 μA Typ at 3 V**
- **Output Compatible With TTL, MOS, and CMOS**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Built-In ESD Protection**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

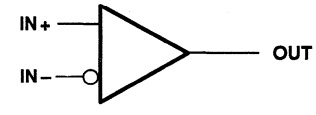


NC – No internal connection

description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and to operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120 μA.

symbol (each comparator)



The TLV2352 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352 is fully characterized at 3 V and 5 V for operation from – 40°C to 85°C.

The TLV2352 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

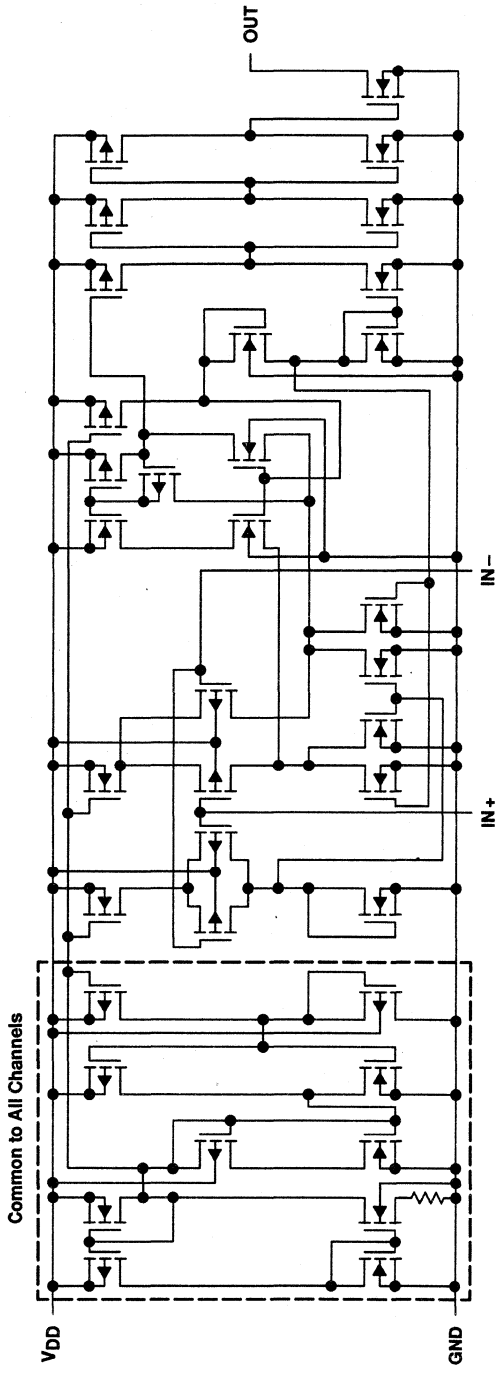
T_A	V_{IO}max at 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	5 mV	TLV2352ID	TLV2352IP	TLV2352IPWLE	TLV2352Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).
The PW packages are only available left-ended taped and reeled (e.g., TLV2352IPWLE)

These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic



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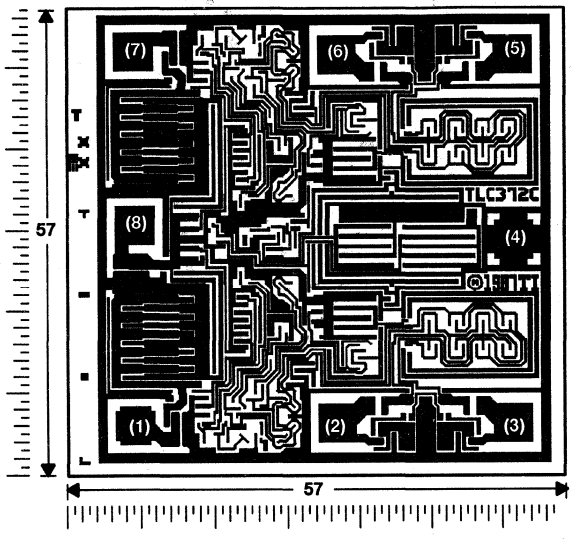
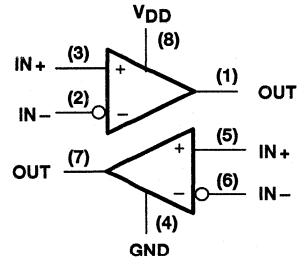
TLV2352Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±8 V
Input voltage range, V_I ..... −0.3 to 8 V
Output voltage, V_O ..... 8 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short-circuit current to GND (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	0	1.75	V
	V_{DD} = 5 V	0	3.75	
Operating free-air temperature, T_A		−40	85	°C

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electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS		T_A‡	TLV2352I						UNIT
					V_{DD} = 3 V			V_{DD} = 5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4	25°C		1	5		1	5	mV
				Full range			7			7	
I_{IO}	Input offset current			25°C		1			1		pA
				85°C			1			1	nA
I_{IB}	Input bias current			25°C		5			5		pA
				85°C			2			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to 2			0 to 4			V
				Full range	0 to 1.75			0 to 3.75			
I_{OH}	High-level output current	V_{ID} = 1 V		25°C		0.1			0.1		nA
				Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 2 mA	25°C		115	300		150	400	mV
				Full range			600			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V,	No load	25°C		120	250		140	300	µA
				Full range			350			400	

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.
‡ Full range is −40°C to 85°C. IMPORTANT: See Parameter Measurement Information.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2352I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, C_L = 15 pF§,	See Note 5	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2352I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, C_L = 15 pF§,	See Note 5	100-mV input step with 5-mV overdrive		650		ns
			TTL-level input step		200		

§ C_L includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

electrical characteristics at specified free-air temperature, T_A = 25°C†

PARAMETER		TEST CONDITIONS		TLV2352Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4		1	5		1	5	mV
I_{IO}	Input offset current				1			1		pA
I_{IB}	Input bias current				5			5		pA
V_{ICR}	Common-mode input voltage range			0 to 2			0 to 4			V
I_{OH}	High-level output current	V_{ID} = 1 V			0.1			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V	I_{OL} = 2 mA		115	300		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V	No load		120	250		140	300	µA

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

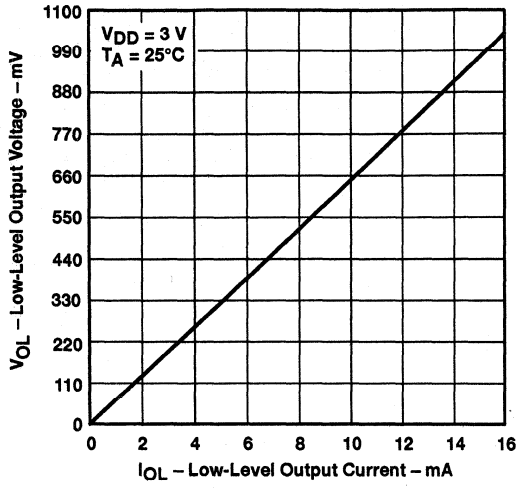


Figure 1

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

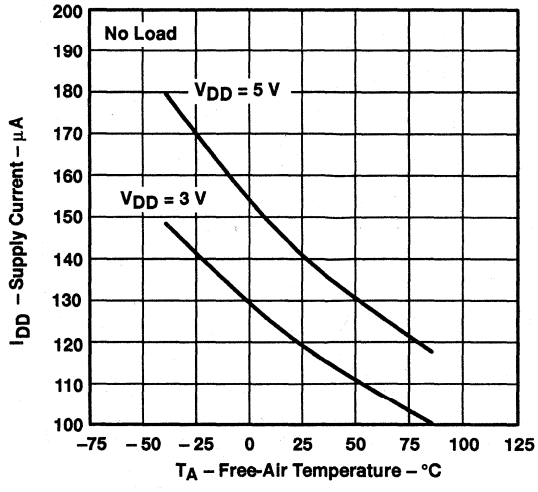


Figure 2

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

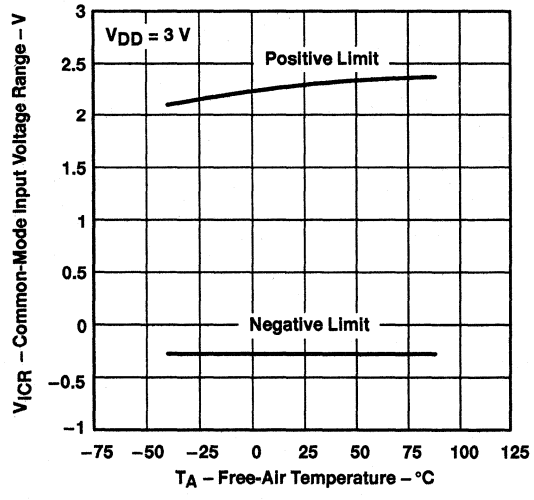


Figure 3

OUTPUT FALL TIME
vs
CAPACITIVE LOAD

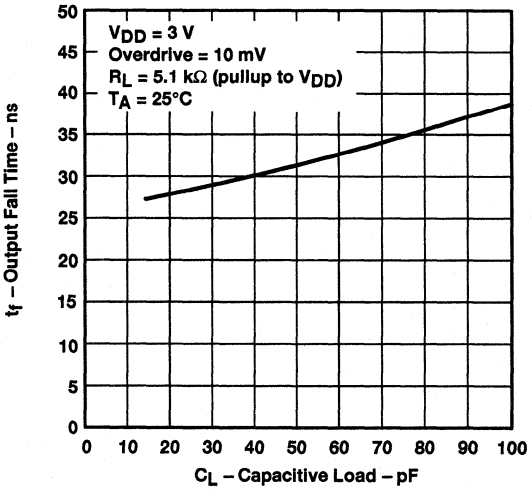


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

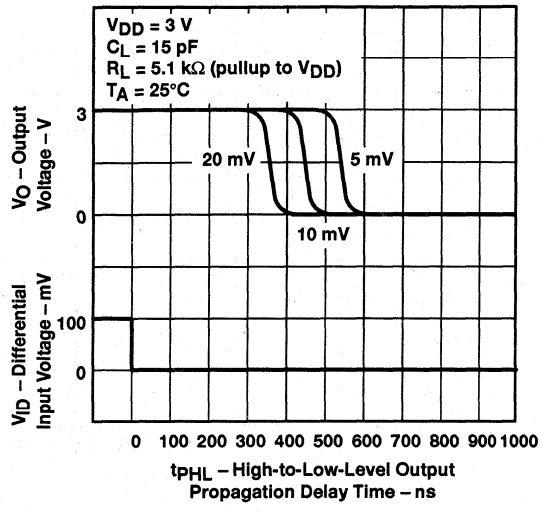


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

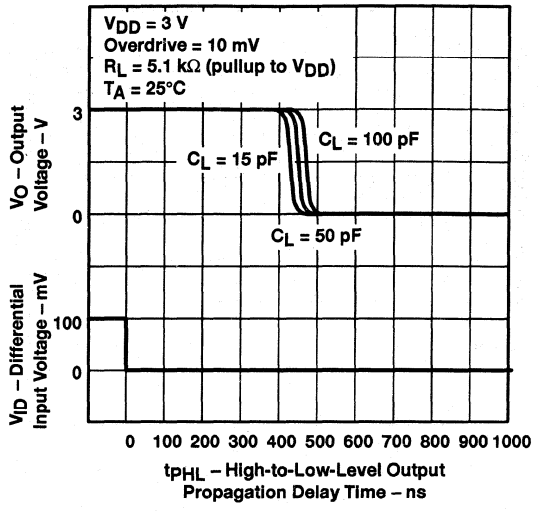


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

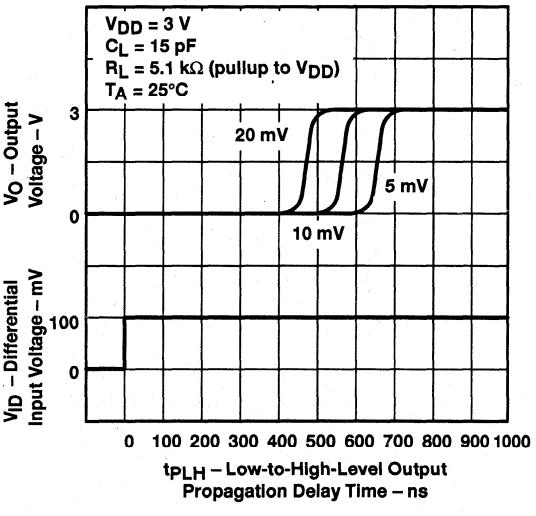


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

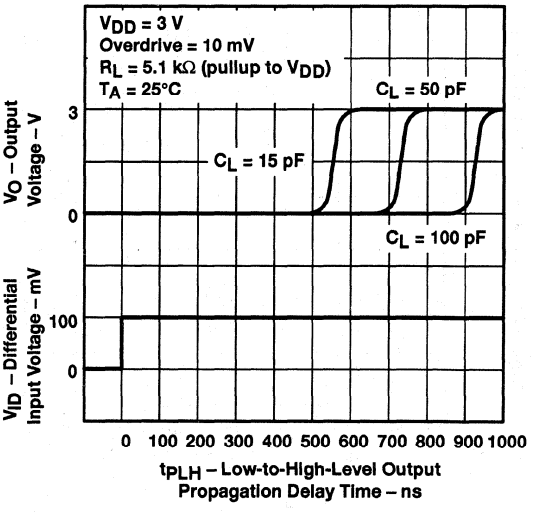


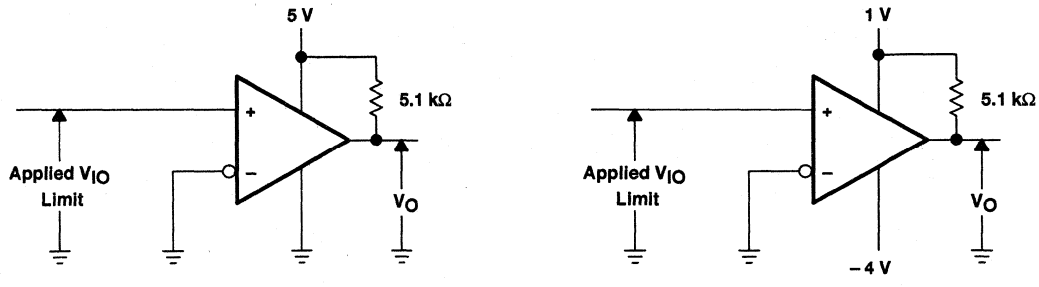
Figure 8

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} WITH V_{IC} = 4 V

Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

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Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

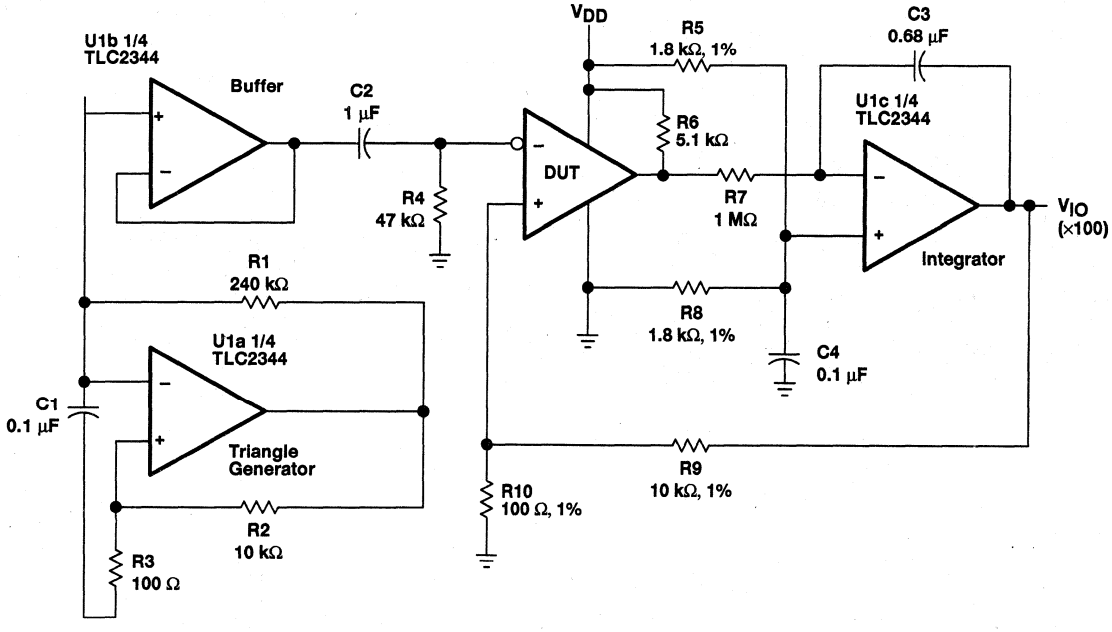
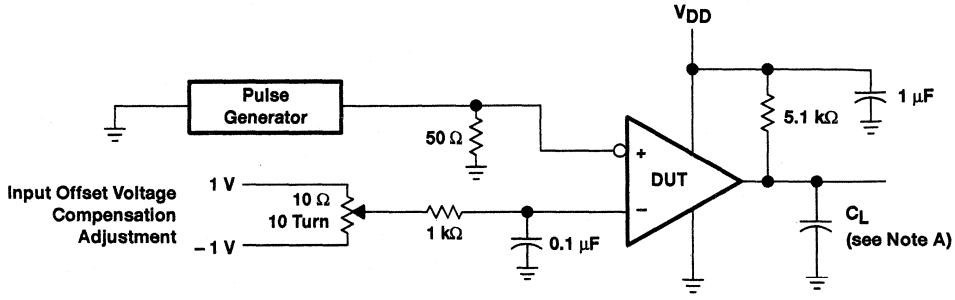


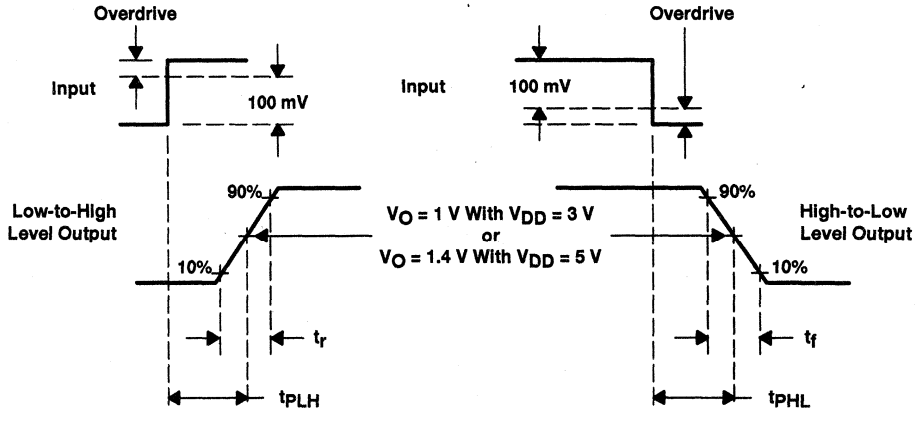
Figure 10. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 V with V_{DD} = 5 V. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change states.



TEST CIRCUIT



VOLTAGE WAVEFORMS

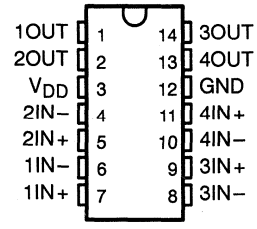
NOTE A: C_L includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

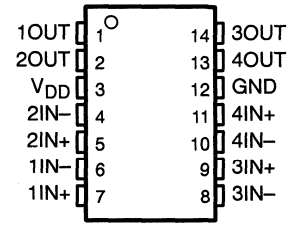
SLCS012 – MAY 1992

- **Wide Range of Supply Voltages 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Very-Low Supply-Current Drain 240 μA Typ at 3 V**
- **Common-Mode Input Voltage Range Includes Ground**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Output Compatible With TTL, MOS, and CMOS**
- **Built-In ESD Protection**

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

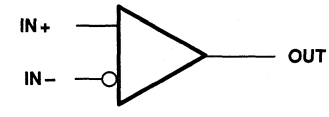


description

The TLV2354 consists of four independent, low-power comparators specifically designed for single power-supply applications and to operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 240 μA.

The TLV2354 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2354 is fully characterized for operation from – 40°C to 85°C.

symbol (each comparator)



The TLV2354 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

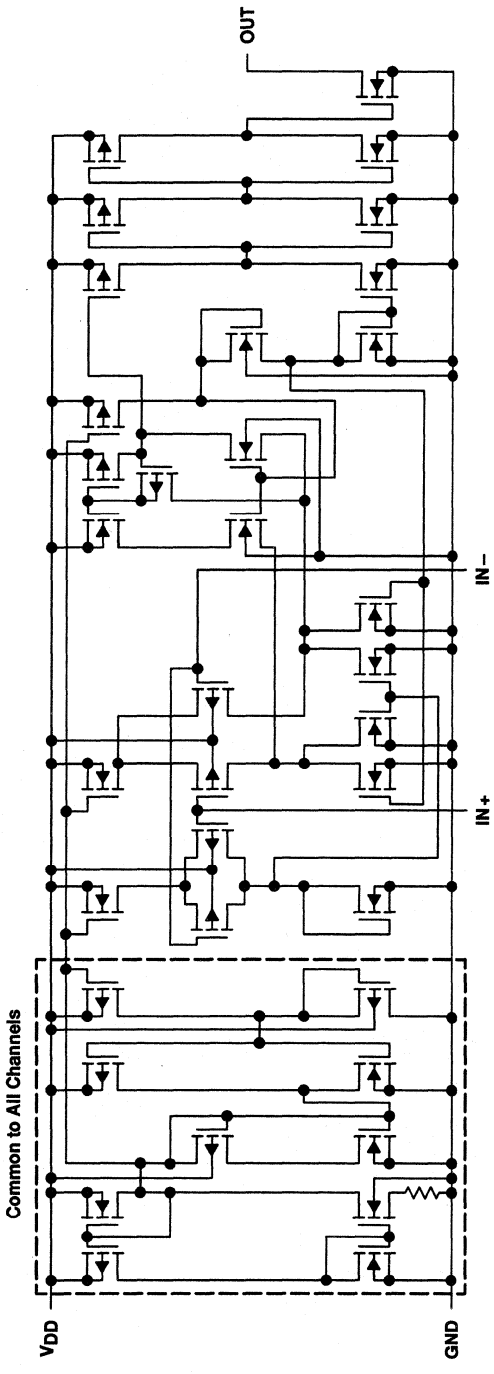
T_A	V_{IO}max at 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–40°C to 85°C	5 mV	TLV2354ID	TLV2354IN	TLV2354IPWLE	TLV2354Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).
The PW packages are only available left-ended taped and reeled (e.g., TLV2354IPWLE)

These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LinCMOS is a trademark of Texas Instruments Incorporated.

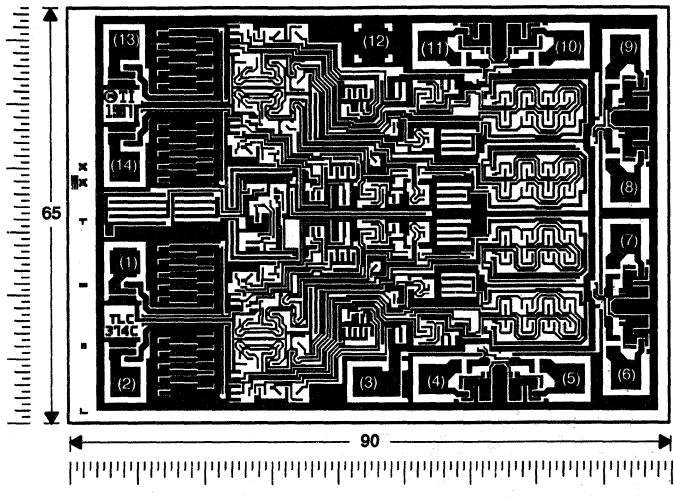
equivalent schematic

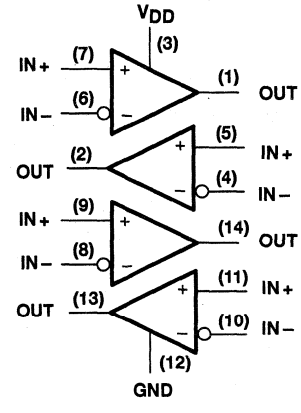


TLV2354Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2354. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±8 V
Input voltage range, V_I ..... −0.3 to 8 V
Output voltage, V_O ..... 8 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short-circuit current to GND (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	346 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	0	1.75	V
	V_{DD} = 5 V	0	3.75	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS		T_A‡	TLV2354I						UNIT
					V_{DD} = 3 V			V_{DD} = 5 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4	25°C		1	5		1	5	mV
				Full range			7			7	
I_{IO}	Input offset current			25°C		1			1		pA
				85°C			1			1	nA
I_{IB}	Input bias current			25°C		5			5		pA
				85°C			2			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to 2			0 to 4			V
				Full range	0 to 1.75			0 to 3.75			
I_{OH}	High-level output current	V_{ID} = 1 V		25°C		0.1			0.1		nA
				Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 2 mA	25°C		115	300		150	400	mA
				Full range			600			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V,	No load	25°C		240	500		290	600	μA
				Full range			700			800	

† All characteristics are measured with zero common-mode input voltage unless otherwise noted.
‡ Full range is −40°C to 85°C. IMPORTANT: See Parameter Measurement Information.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2354I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, See Note 5	C_L = 15 pF§,	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS			TLV2354I			UNIT
				MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, See Note 5	C_L = 15 pF§,	100-mV input step with 5-mV overdrive		650		ns
			TTL-level input step		200		

§ C_L includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.

electrical characteristics at specified free-air temperature, T_A = 25°C†

PARAMETER		TEST CONDITIONS		TLV2354Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4		1	5		1	5	mV
I_{IO}	Input offset current				1			1		pA
I_{IB}	Input bias current				5			5		pA
V_{ICR}	Common-mode input voltage range			0 to 2			0 to 4			V
I_{OH}	High-level output current	V_{ID} = 1 V			0.1			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 2 mA		115	300		150	400	mV
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I_{DD}	Supply current	V_{ID} = 1 V,	No load		240	500		290	600	µA

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TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

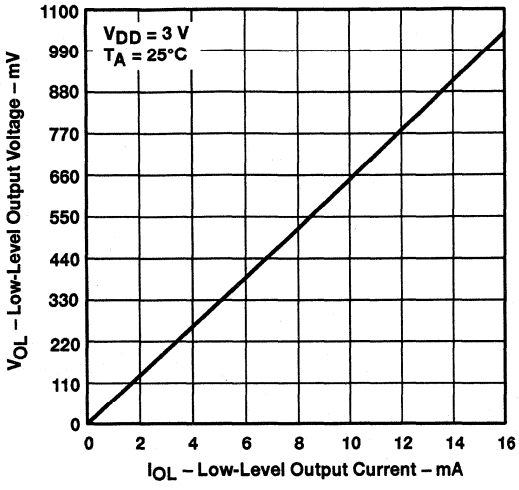

Figure 1

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

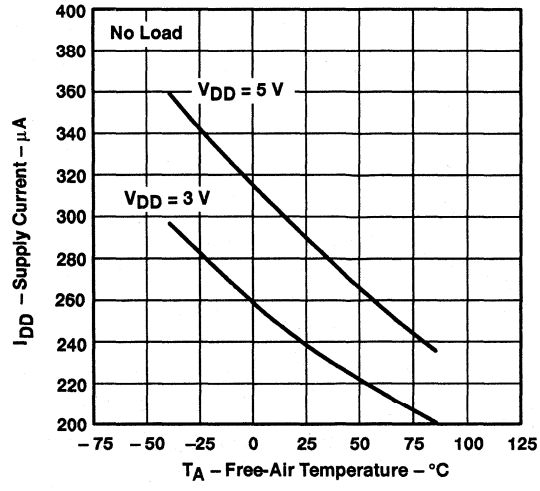

Figure 2

COMMON-MODE INPUT VOLTAGE RANGE vs FREE-AIR TEMPERATURE

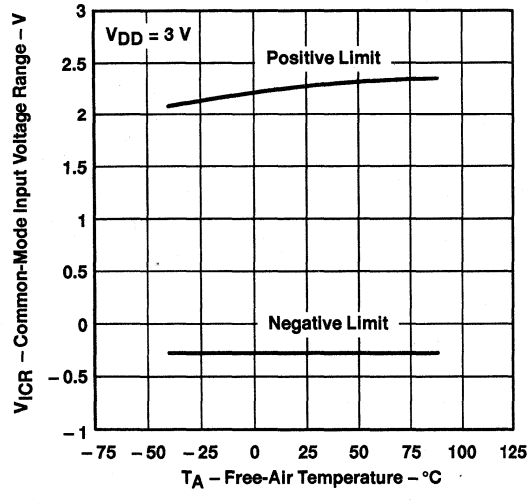

Figure 3

OUTPUT FALL TIME vs CAPACITIVE LOAD

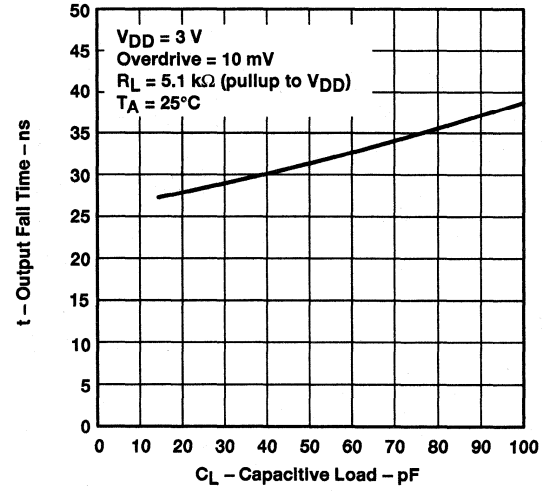

Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

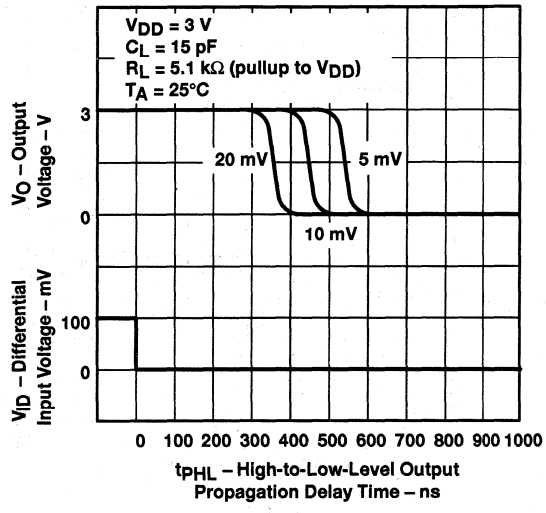

Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

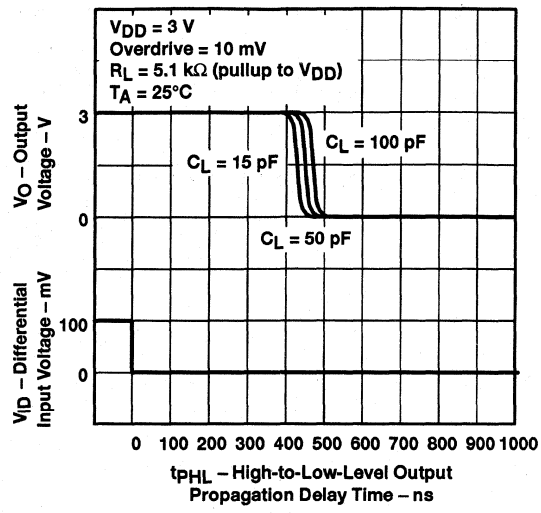

Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

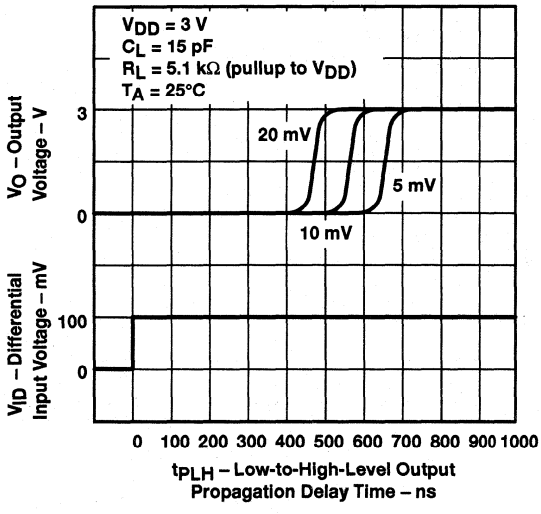

Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

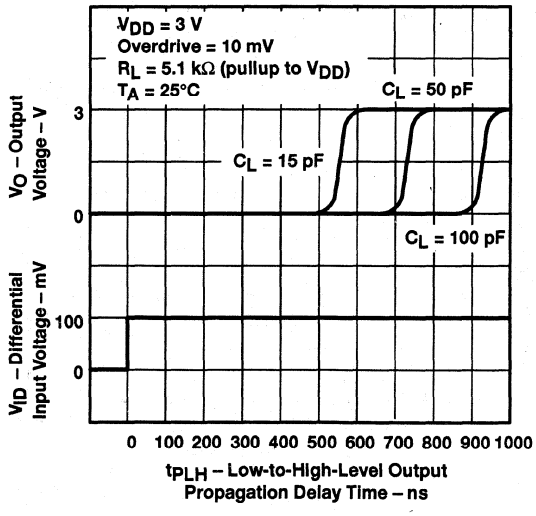

Figure 8

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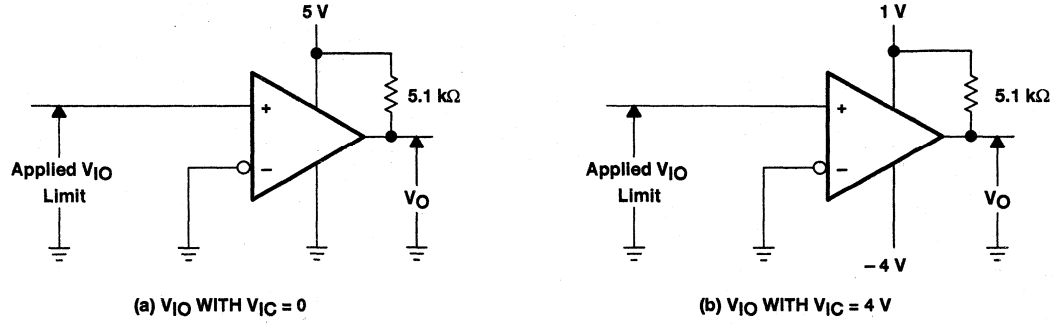
The digital output stage of the TLV2354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test rather than changing the input voltages to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} WITH V_{IC} = 4 V

Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

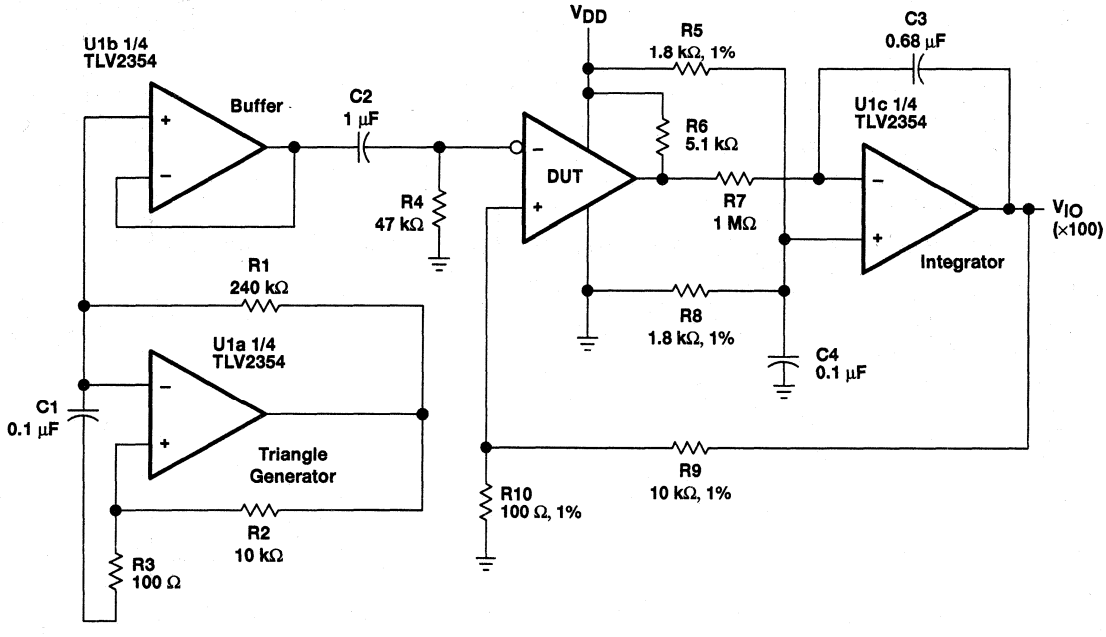
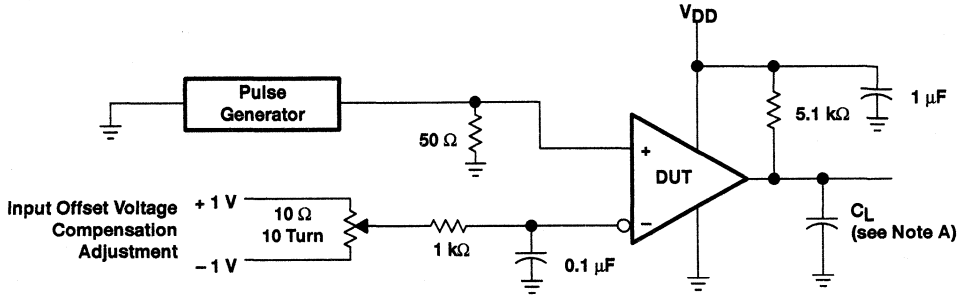


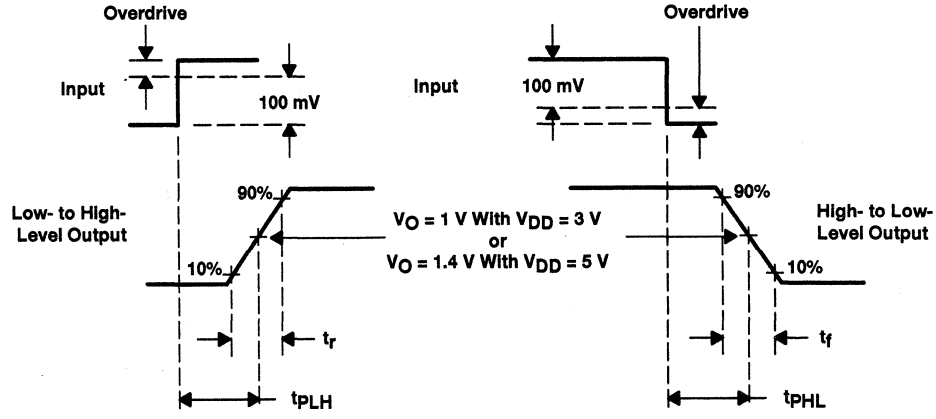
Figure 10. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 V with V_{DD} = 5 V. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

General Information (Volume A) 1
Operational Amplifiers 2
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Operational Amplifiers (continued) 5
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Mechanical Data 7–

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example:	TLE	2022	PW	LE

Prefix

MUST CONTAIN TWO OR THREE LETTERS

SN ..... TI Special Functions or Interface Products
TL, TLE ..... TI Linear Products
TLC ..... TI Linear Silicon-Gate CMOS Products

STANDARD SECOND-SOURCE PREFIXES

AD ..... Analog Devices
ADC, LF, LM, LP, or MP ..... National
LT or LTC ..... Linear Technology
MC ..... Motorola
NE, SA, or SE ..... Signetics
OP ..... PMI
RC, RM, or RV ..... Raytheon
uA ..... Fairchild/National
UC ..... Unitrode

Unique Circuit Description Including Temperature Range

MUST CONTAIN TWO OR MORE CHARACTERS
(from individual data sheets)

Examples: 10, 592, 7757, 34070, 1451AC, 2217-285

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DB, DW, FK, FN, J, JD, JG, KC, KV, LP, LPF, N, NE, NS, NT, NW, P, PK, PW, U, W
(from pin-connection diagrams on individual data sheet)

Available Taped and Reeled or Left-Ended Taped and Reeled

R – Available Taped and Reeled
LE – Available Only Left-Ended Taped and Reeled

ORDERING INSTRUCTIONS

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (J, JD, JG, N, NT, NS, NW, P)
- A-Channel Antistatic or Conductive Plastic Tubing

Small Outline (D, DW)
- Tape and Reel
- Antistatic or Conductive Plastic Tubing

Shrink Small Outline (DB)
- Tape and Reel

Thin Shrink Small Outline (PW)
- Tape and Reel

Chip Carriers (FK, FN)
- Antistatic or Conductive Plastic Tubing

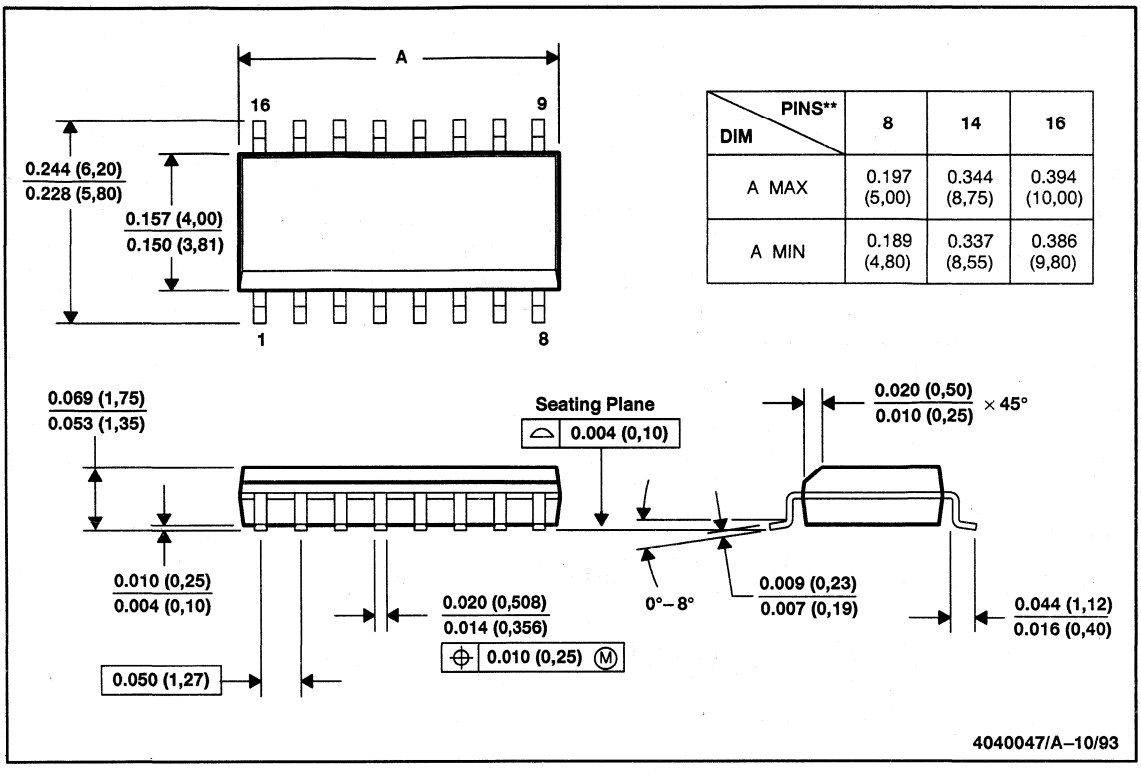
Flat (U, W)
- Milton Ross Carriers

Plug-In (LP)
- Plastic Bag
- Tape and Reel

D/R-PDSO-G**

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16 PIN SHOWN

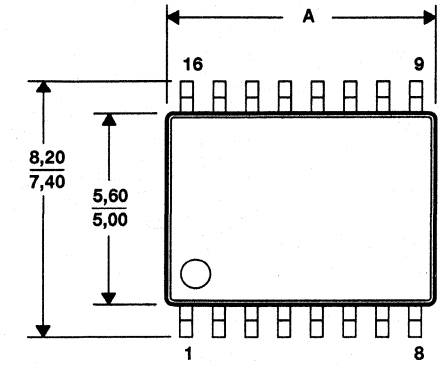


DIM \ PINS**	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

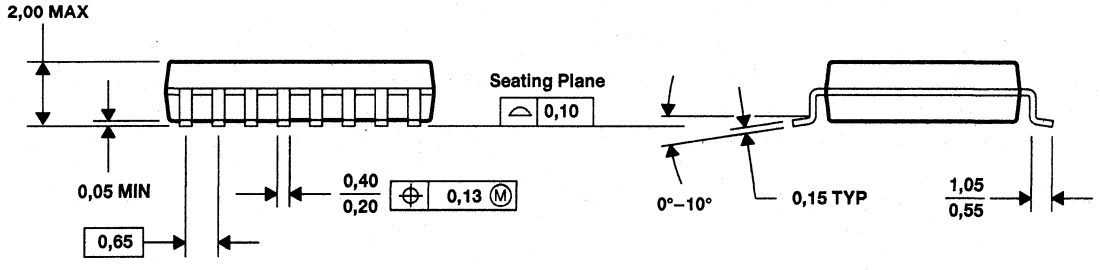
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Mold protrusion shall not exceed 0.006 (0,15).

DB/R-PDSO-G** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS**	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30



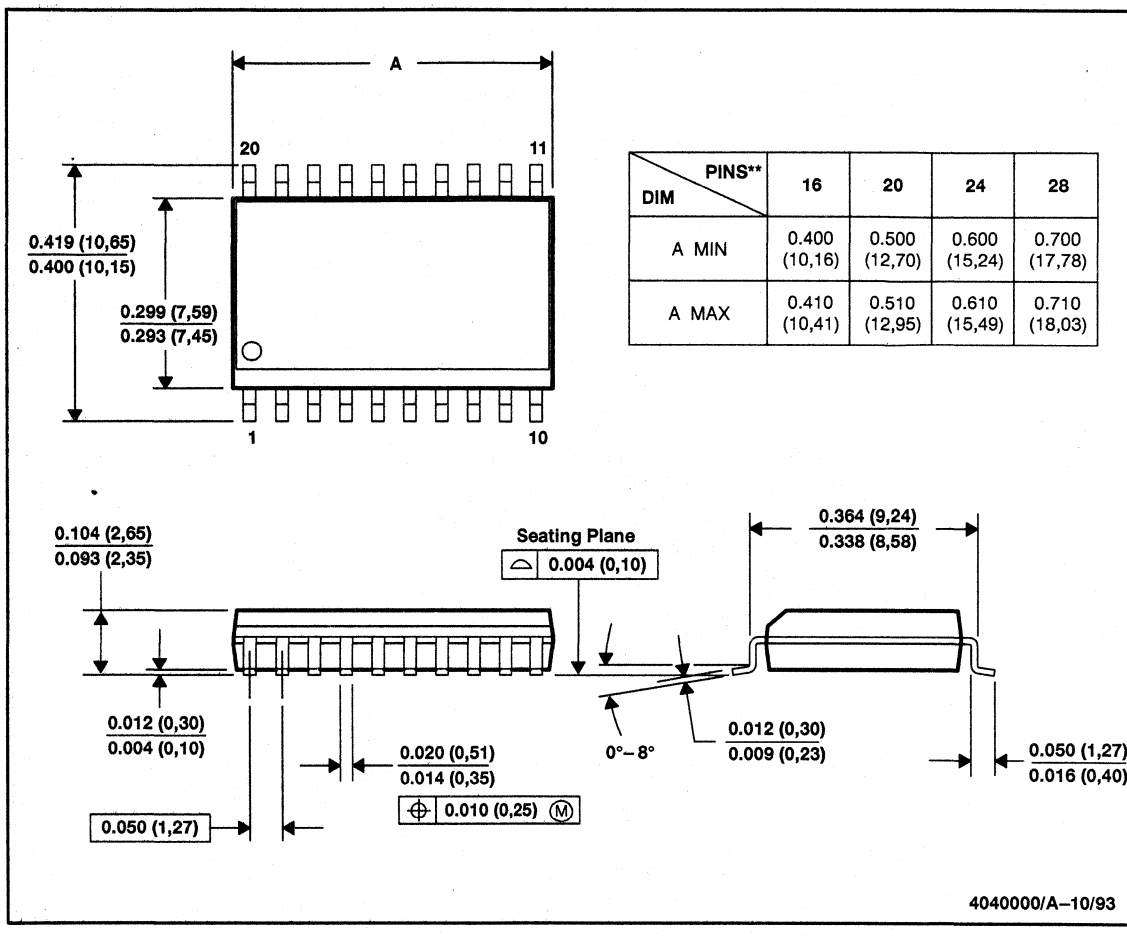
4040065/A–10/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

DW/R-PDSO-G**

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

20 PIN SHOWN



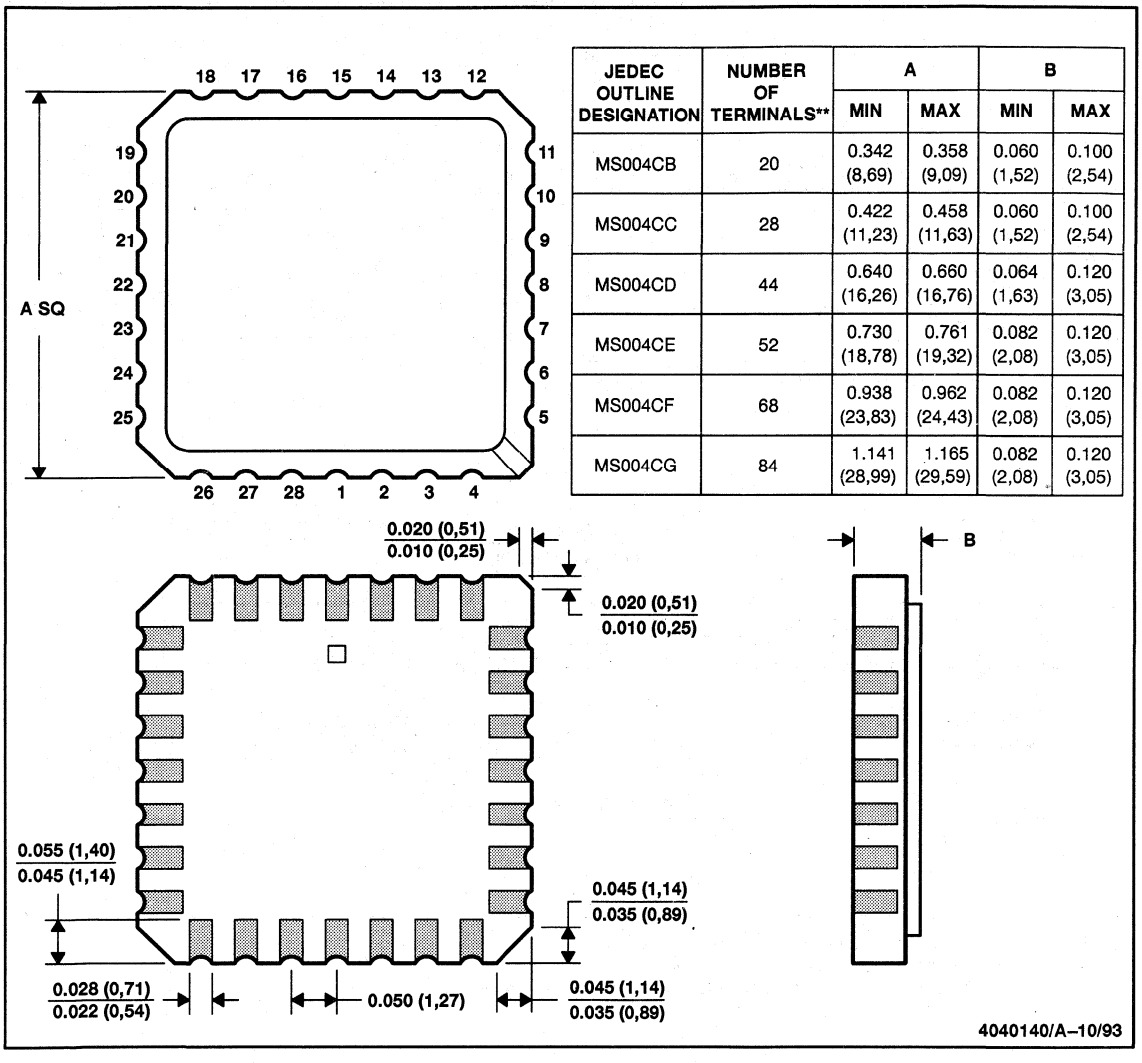
DIM \ PINS**	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

FK/S-CQCC-N**

LEADLESS CERAMIC CHIP CARRIER PACKAGE

28-TERMINAL PACKAGE SHOWN



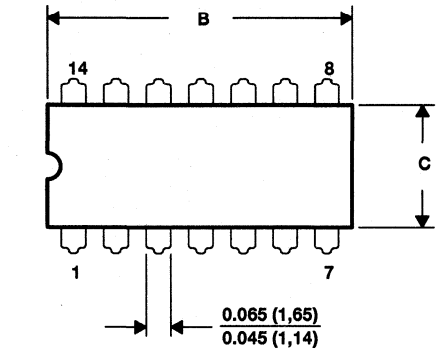
JEDEC OUTLINE DESIGNATION	NUMBER OF TERMINALS**	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	0.342 (8,69)	0.358 (9,09)	0.060 (1,52)	0.100 (2,54)
MS004CC	28	0.422 (11,23)	0.458 (11,63)	0.060 (1,52)	0.100 (2,54)
MS004CD	44	0.640 (16,26)	0.660 (16,76)	0.064 (1,63)	0.120 (3,05)
MS004CE	52	0.730 (18,78)	0.761 (19,32)	0.082 (2,08)	0.120 (3,05)
MS004CF	68	0.938 (23,83)	0.962 (24,43)	0.082 (2,08)	0.120 (3,05)
MS004CG	84	1.141 (28,99)	1.165 (29,59)	0.082 (2,08)	0.120 (3,05)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

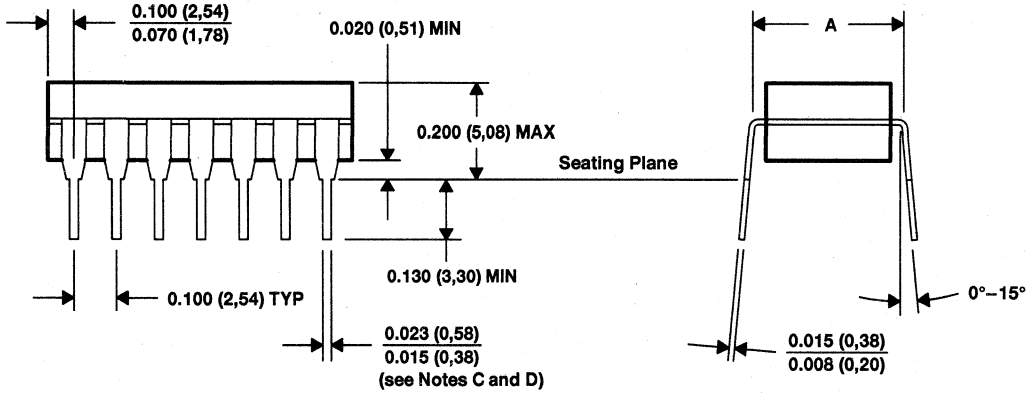
J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



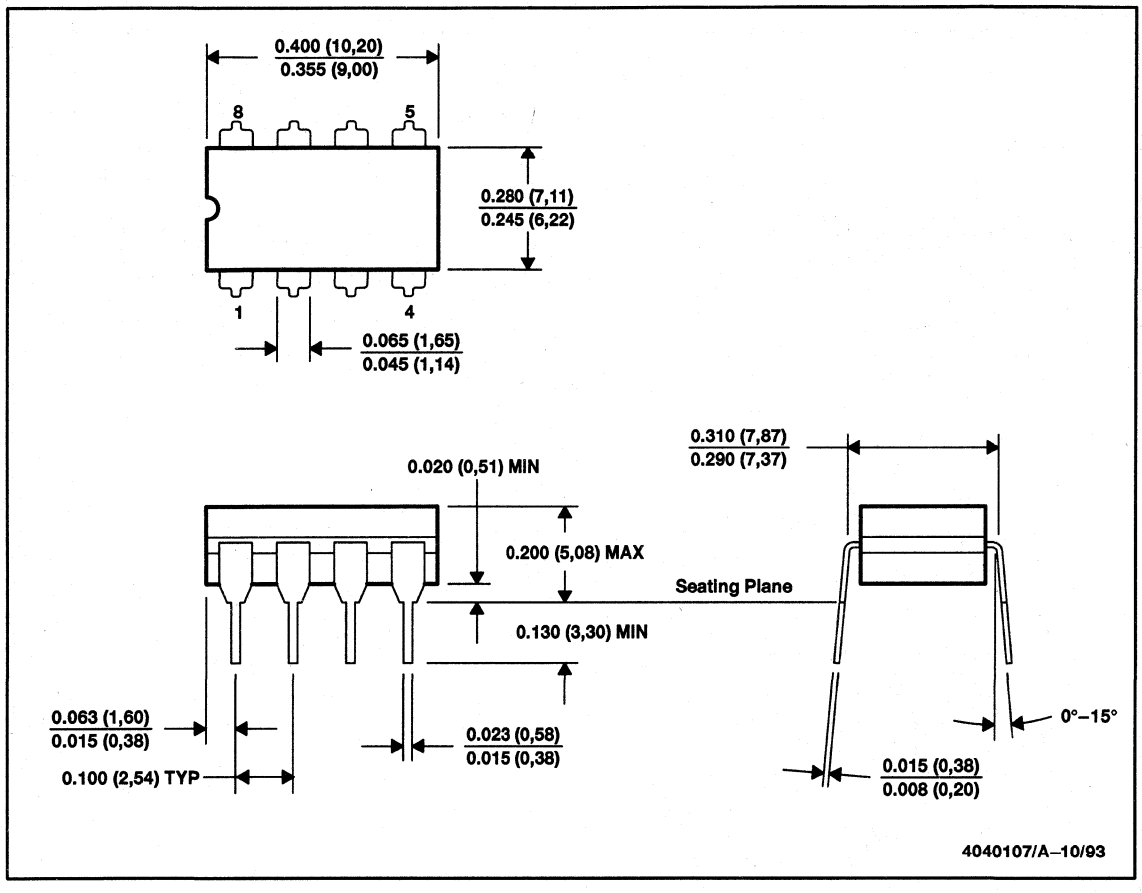
DIM \ PINS**	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



4040083/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

JG/R-GDIP-T8 **CERAMIC DUAL-IN-LINE PACKAGE**

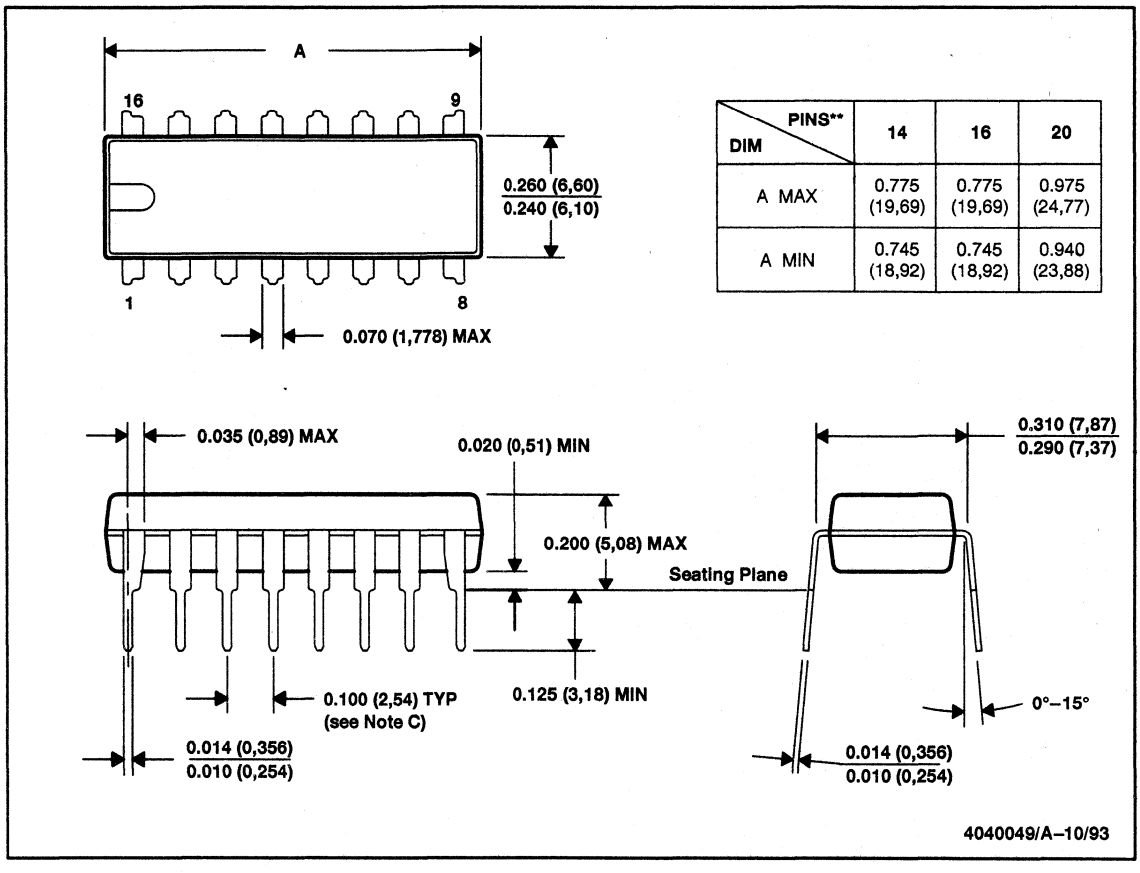


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



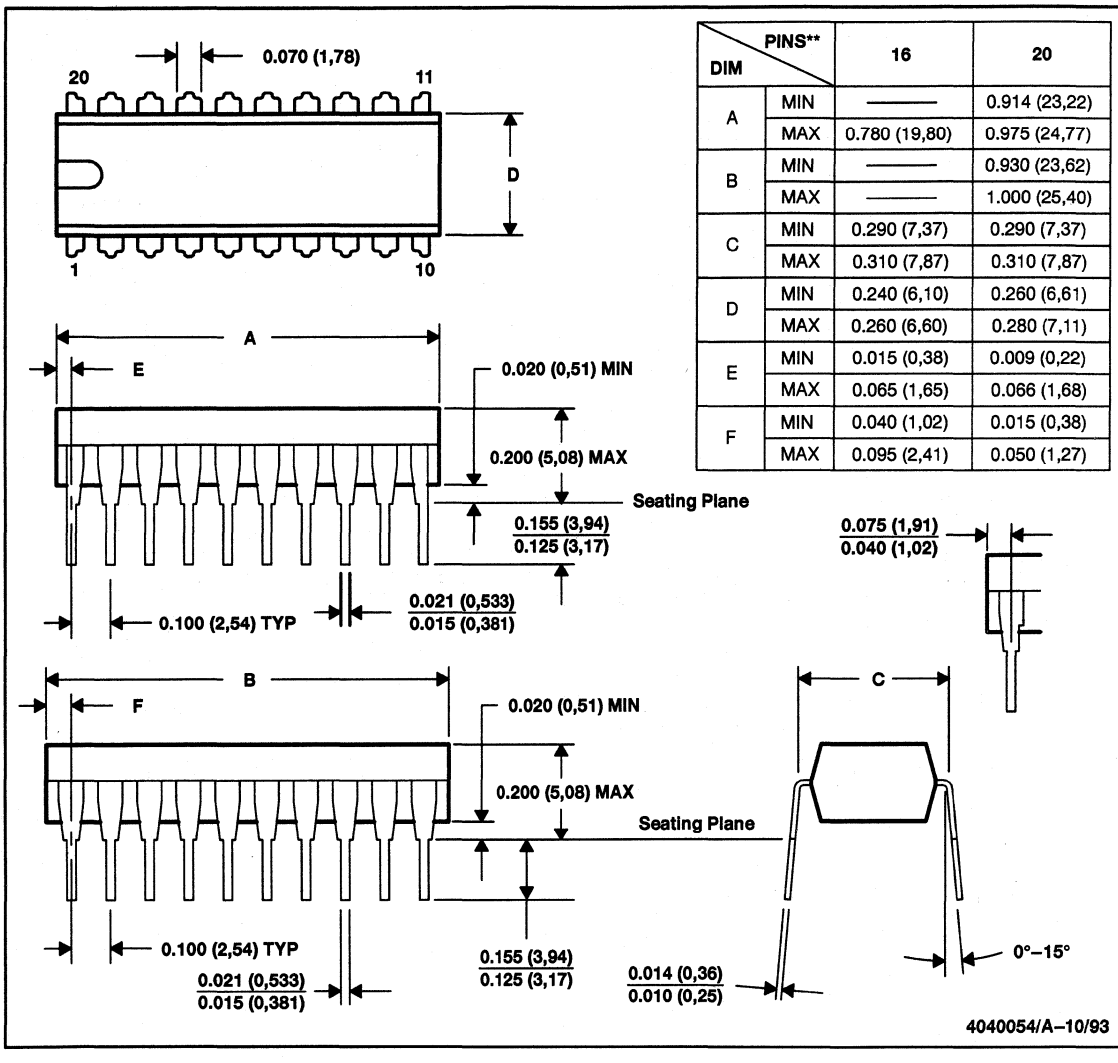
DIM \ PINS**	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each lead centerline is located within 0.010 (0,254) of its true longitudinal position.

NE/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

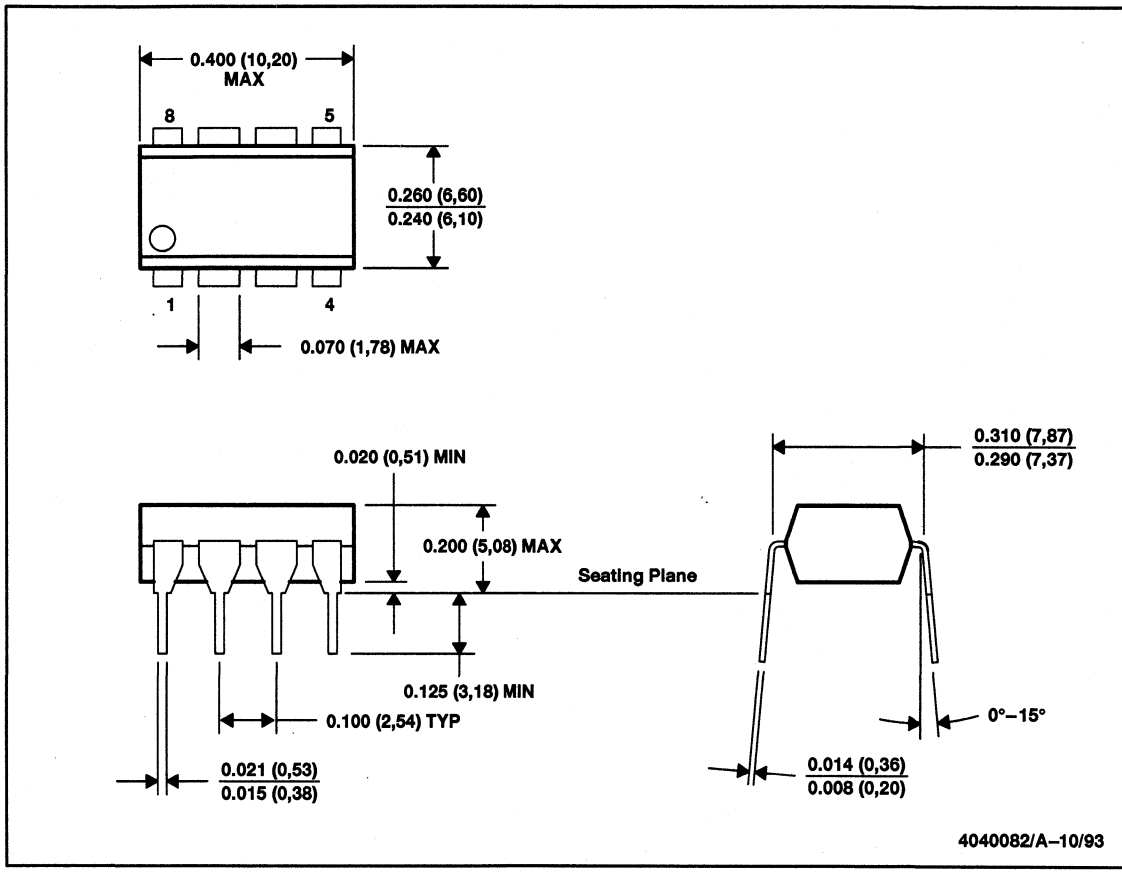
20 PIN SHOWN



DIM \ PINS**		16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.290 (7,37)	0.290 (7,37)
	MAX	0.310 (7,87)	0.310 (7,87)
D	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)
E	MIN	0.015 (0,38)	0.009 (0,22)
	MAX	0.065 (1,65)	0.066 (1,68)
F	MIN	0.040 (1,02)	0.015 (0,38)
	MAX	0.095 (2,41)	0.050 (1,27)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

P/R-PDIP-T8 **PLASTIC DUAL-IN-LINE PACKAGE**

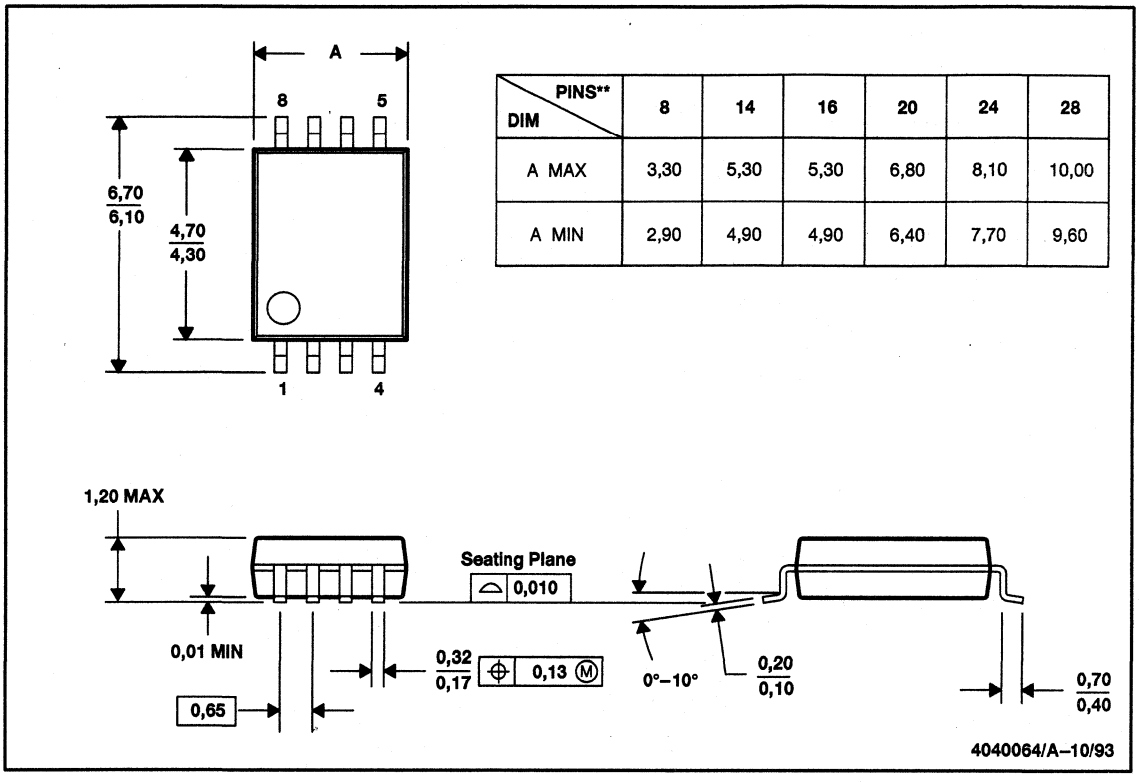


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

PW/R-PDSO-G**

PLASTIC THIN SHRINK SMALL-OUTLINE PACKAGE

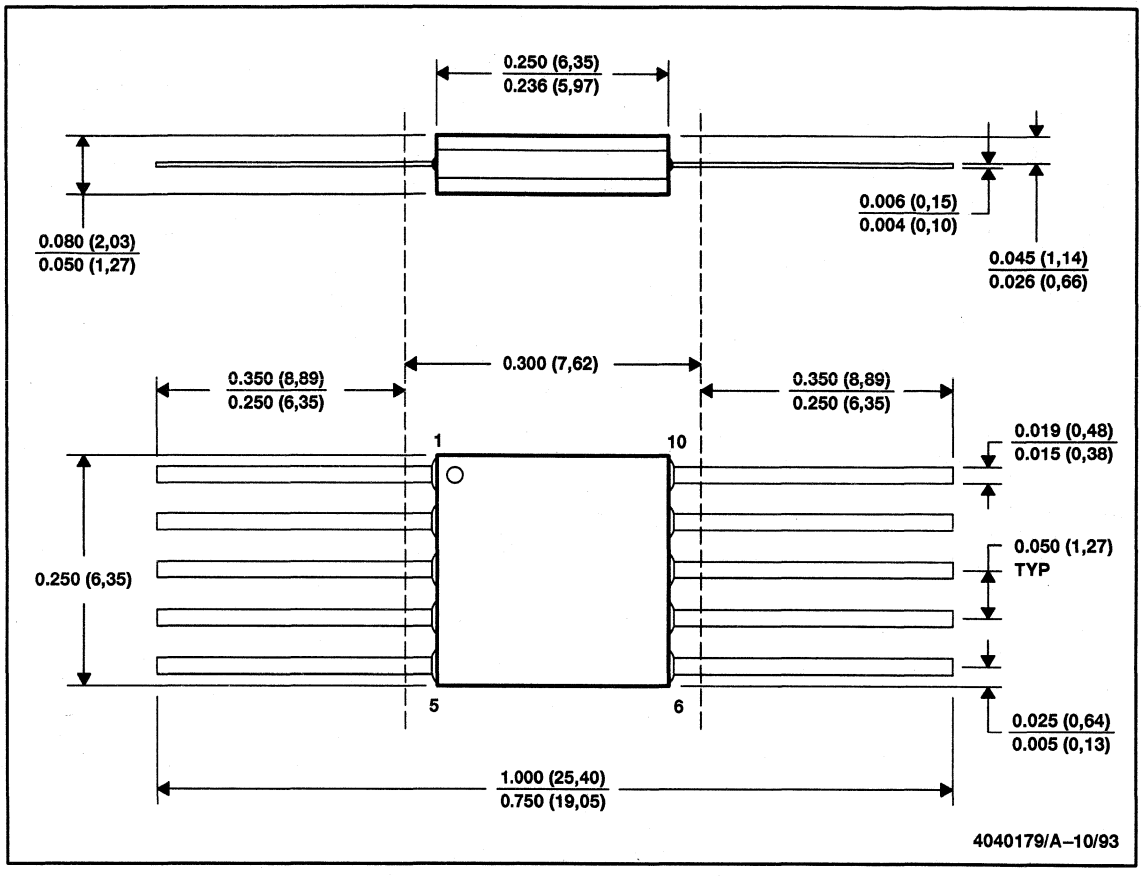
8 PIN SHOWN



DIM \ PINS**	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

U/S-GDFP-F10 **CERAMIC FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within JEDEC MO-004AE

NOTES

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BRAZIL: Texas Instrumentos Electronicos do Brasil Ltda., Av. Eng. Luiz Carlos Berrini, 1461, 11 andar, 04571-903, Sao Paulo, SP, Brazil, 11-535-5133.

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